RZ-EasyFPGA A2.2 - Altera Cyclone IV - EP4CE6E22C8N

Tensão Lógica: 3,3V LVTTL
Corrente GPIO: 8mA

FPGA_RESET	25
FPGA_CLK	23

Keys	Pino
KEY[0]	88
KEY[1]	89
KEY[2]	90
KEY[3]	91

Os botões e os DIP estão ligados juntos!

Botões/DIP são acionados com "0" (LOW ou BAIXO)

Dial Switch	Pino
ckey1	88
ckey2	89
ckey3	90
ckey4	91

LED	Pino
LED[0]	87
LED[1]	86
LED[2]	85
LED[3]	84

UART	Pino
UART_TXD	114
UART_RXD	115

I²C	Pino
FPGA_SCL	112
FPGA_SDA	113
I2C_SCL	99
I2C_SDA	98

Receptor IR	Pino
IR	100

SDRAM	Pino
SDRAM_DQ[0]	28
SDRAM_DQ[1]	30
SDRAM_DQ[2]	31
SDRAM_DQ[3]	32
SDRAM_DQ[4]	33
SDRAM_DQ[5]	34
SDRAM_DQ[6]	38
SDRAM_DQ[7]	39
SDRAM_DQ[8]	54
SDRAM_DQ[9]	53
SDRAM_DQ[10]	52
SDRAM_DQ[11]	51
SDRAM_DQ[12]	50
SDRAM_DQ[13]	49
SDRAM_DQ[14]	46
SDRAM_DQ[15]	44
SDRAM_A[0]	76
SDRAM_A[1]	77
SDRAM_A[2]	80
SDRAM_A[3]	83
SDRAM_A[4]	68
SDRAM_A[5]	67
SDRAM_A[6]	66
SDRAM_A[7]	65
SDRAM_A[8]	64
SDRAM_A[9]	60
SDRAM_A[10]	75
SDRAM_A[11]	59
SDRAM_BS[0]	73
SDRAM_BS[1/	74
SDRAM_DQM[0] / LDQM	42
SDRAM_DQM[1] / UDQM	55
SDRAM_CKE	58
SDRAM_CLK	43
SDRAM_CS	72
SDRAM_RAS	71
SDRAM_CAS	70
SDRAM_WE	69

VGA	Pino
VGA_HSYNC	101
VGA_VSYNC	103
VGA_B	104
VGA_G	105
VGA_R	106

LCD 1602/12864	Pino
LCD_RS	141
LCD_RW	138
LCD_E	143
LCD_D[0]	142
LCD_D[1]	1
LCD_D[2]	144
LCD_D[3]	3
LCD_D[4]	2
LCD_D[5]	10
LCD_D[6]	7
LCD_D[7]	11

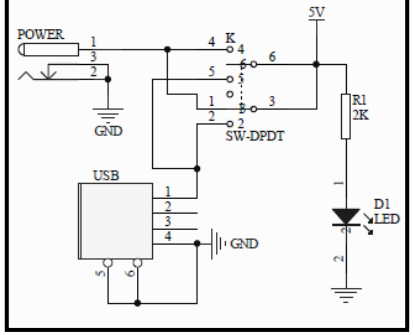
Displ. 7 Segs	Pino
DIG[0]	133
DIG[1]	135
DIG[2]	136
DIG[3]	137
SEG[0]	128
SEG[1]	121
SEG[2]	125
SEG[3]	129
SEG[4]	132
SEG[5]	126
SEG[6]	124
SEG[7]	127

PS2	Pino
PS_CLOCK	119
PS_DATA	120

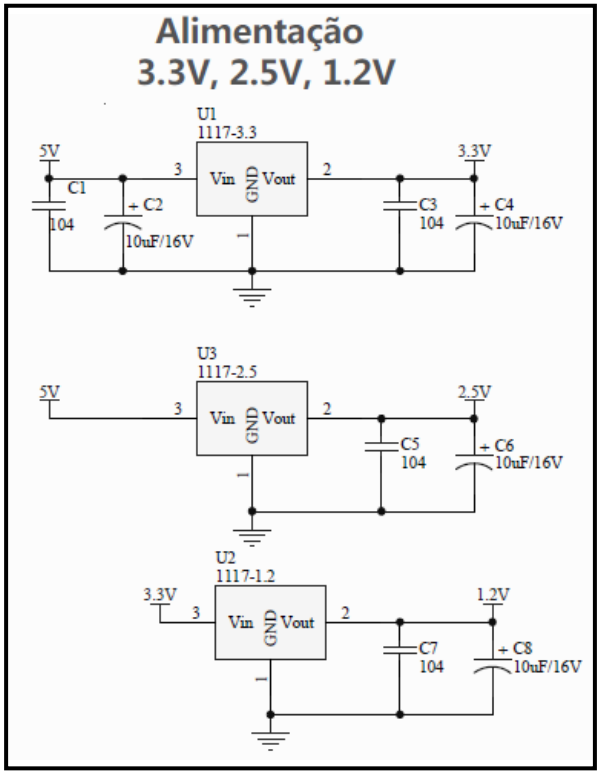
Buzzer	Pino
FPGA_BUZZER	110

Esquemas Elétricos – Kit RZ-EasyFPGA A2.2

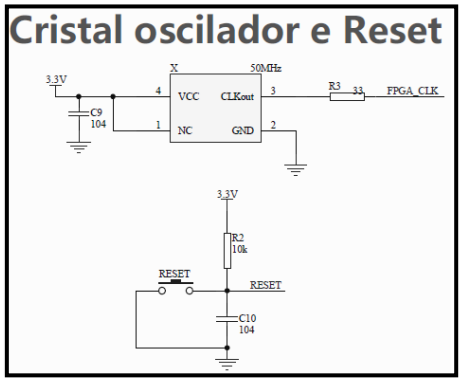
Alimentação



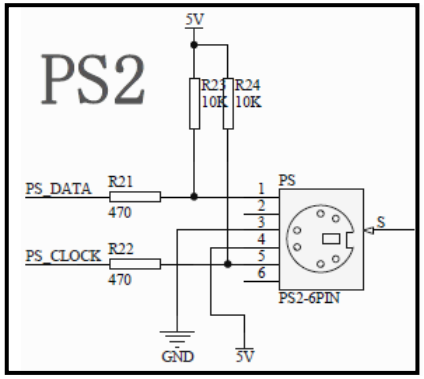
Alimentação
3.3V, 2.5V, 1.2V



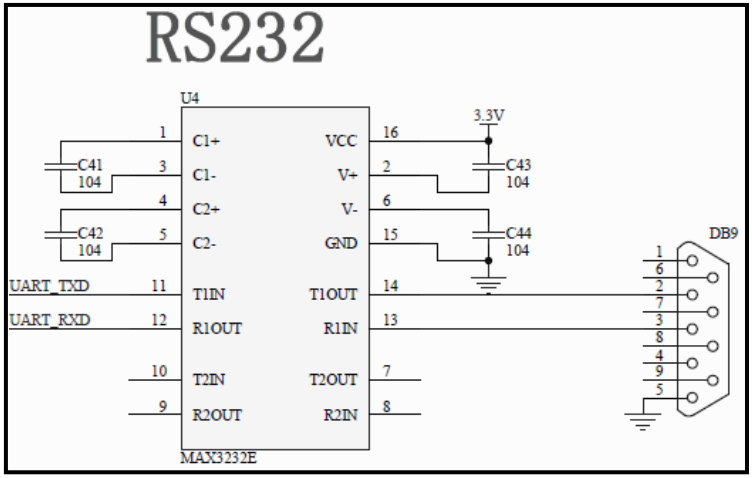
Cristal oscilador e Reset



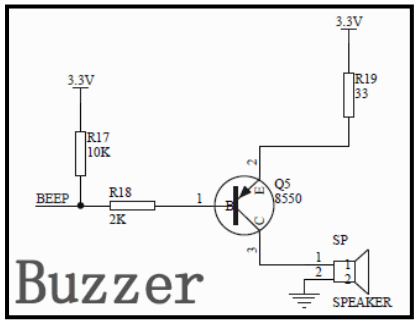
PS2



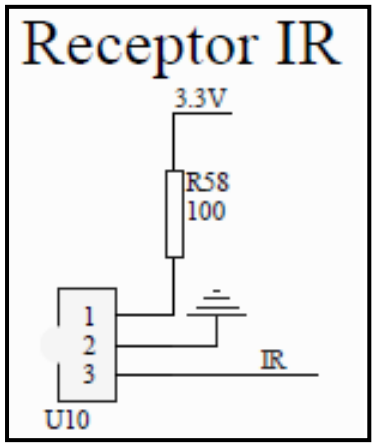
RS232



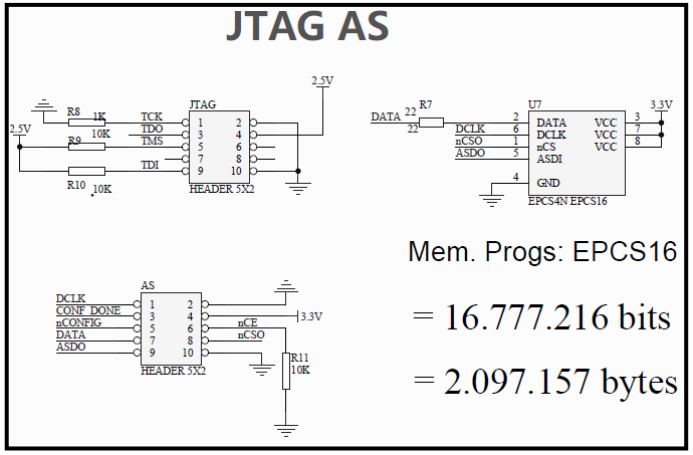
Buzzer



Receptor IR



JTAG AS

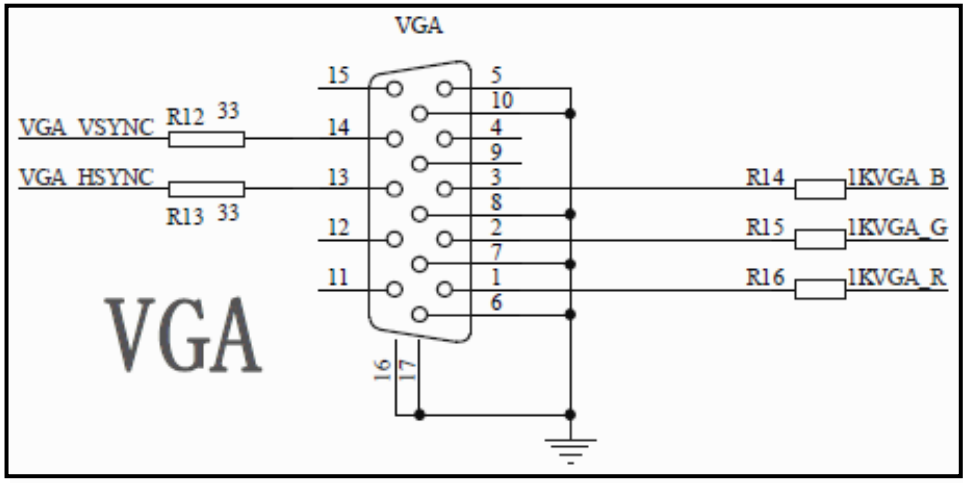


Mem. Progs: EPCS16

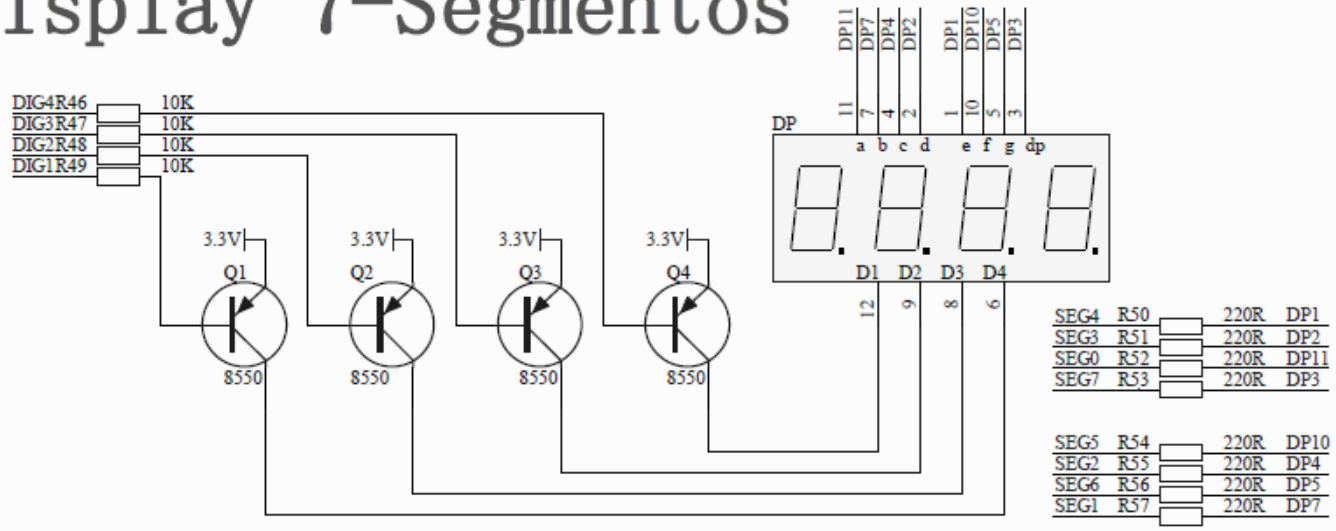
= 16.777.216 bits

= 2.097.157 bytes

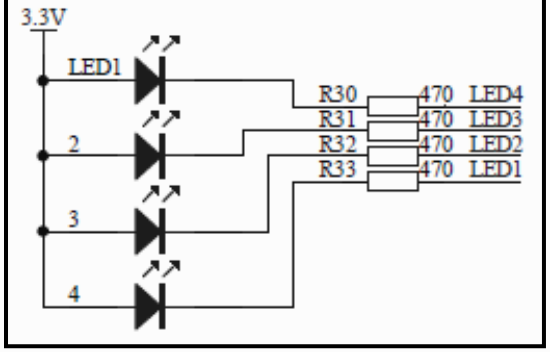
VGA



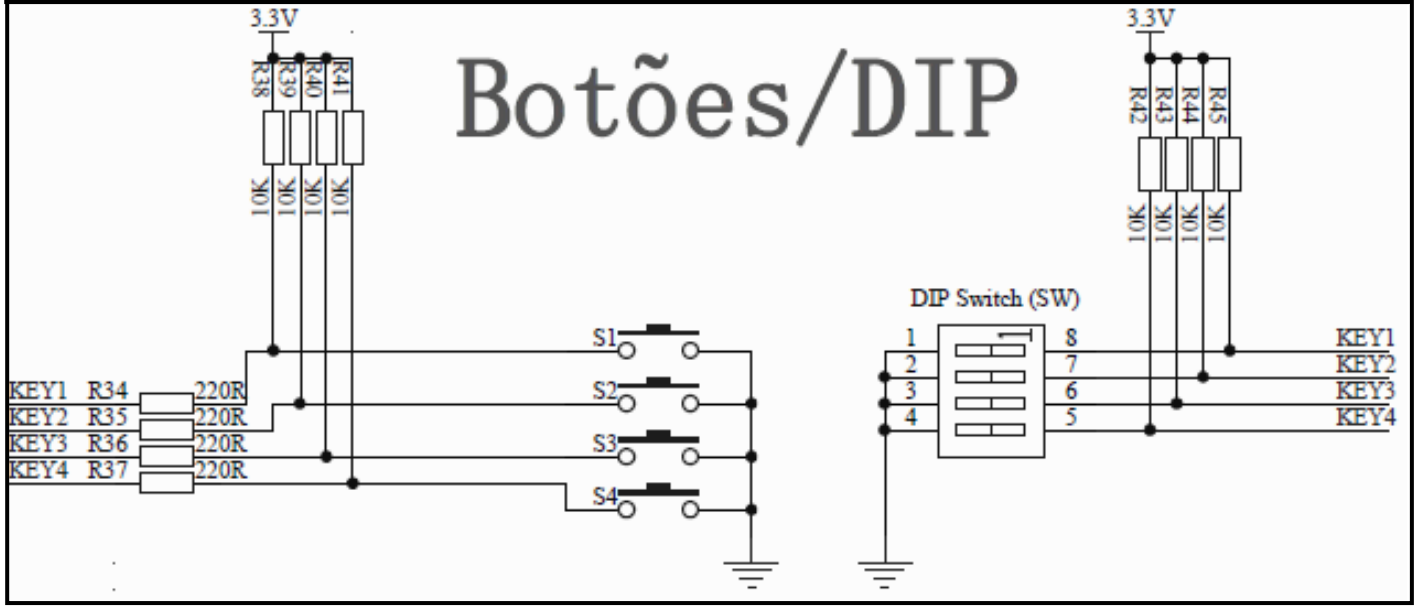
Display 7-Segmentos



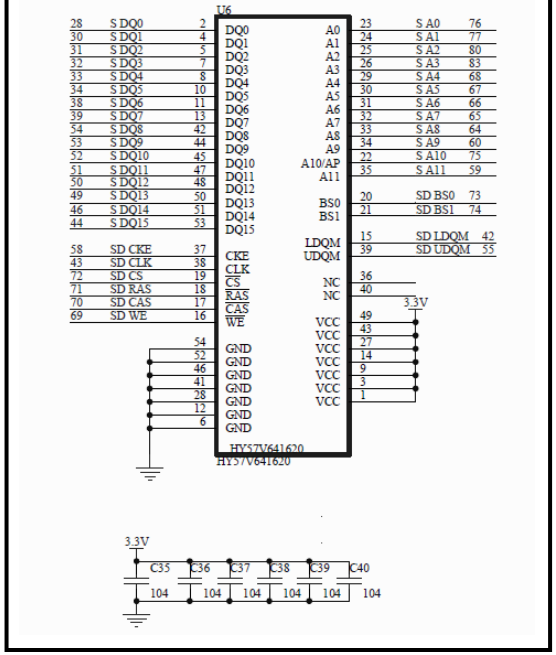
LEDs

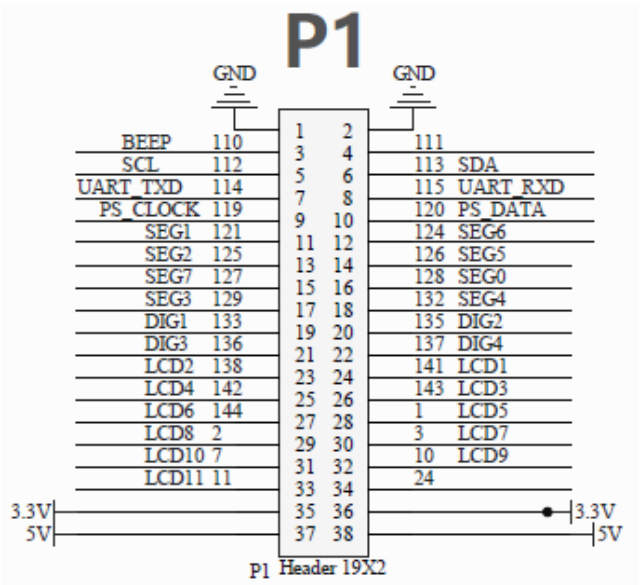


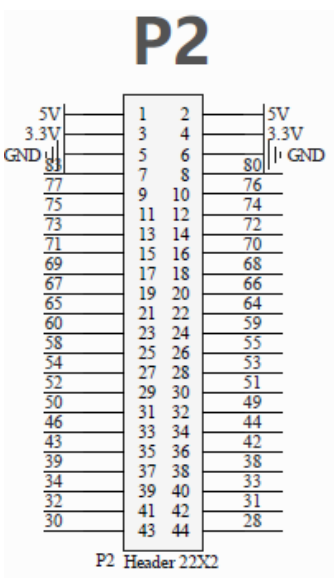
Botões/DIP

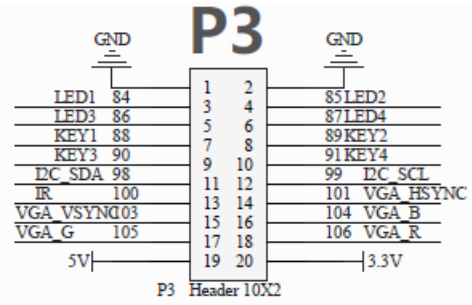


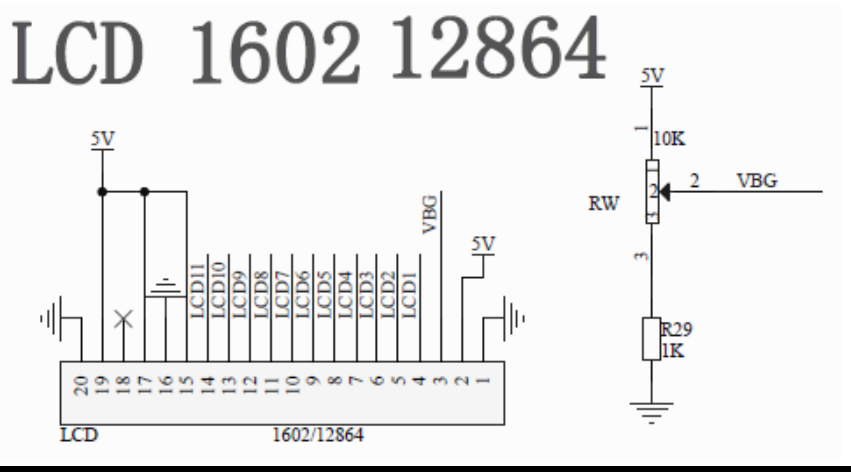
SDRAM (HY57V641620)

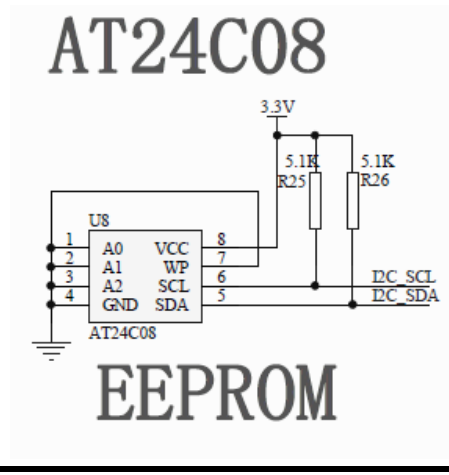


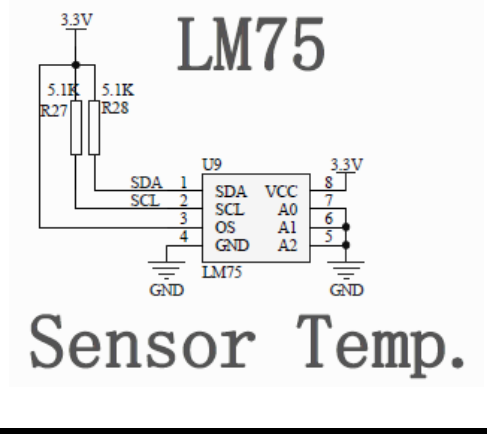

P1
GND
GND
BEEP 110
SCL 112
UART_TXD 114
PS_CLOCK 119
SEG1 121
SEG2 125
SEG7 127
SEG3 129
DIG1 133
DIG3 136
LCD2 138
LCD4 142
LCD6 144
LCD8 2
LCD10 7
LCD11 11
111
113 SDA
115 UART_RXD
120 PS_DATA
124 SEG6
126 SEG5
128 SEG0
132 SEG4
135 DIG2
137 DIG4
141 LCD1
143 LCD3
1 LCD5
3 LCD7
10 LCD9
24
3.3V
5V
3.3V
5V
P1 Header 19X2


P2
5V
3.3V
GND
5V
3.3V
GND
P2 Header 22X2

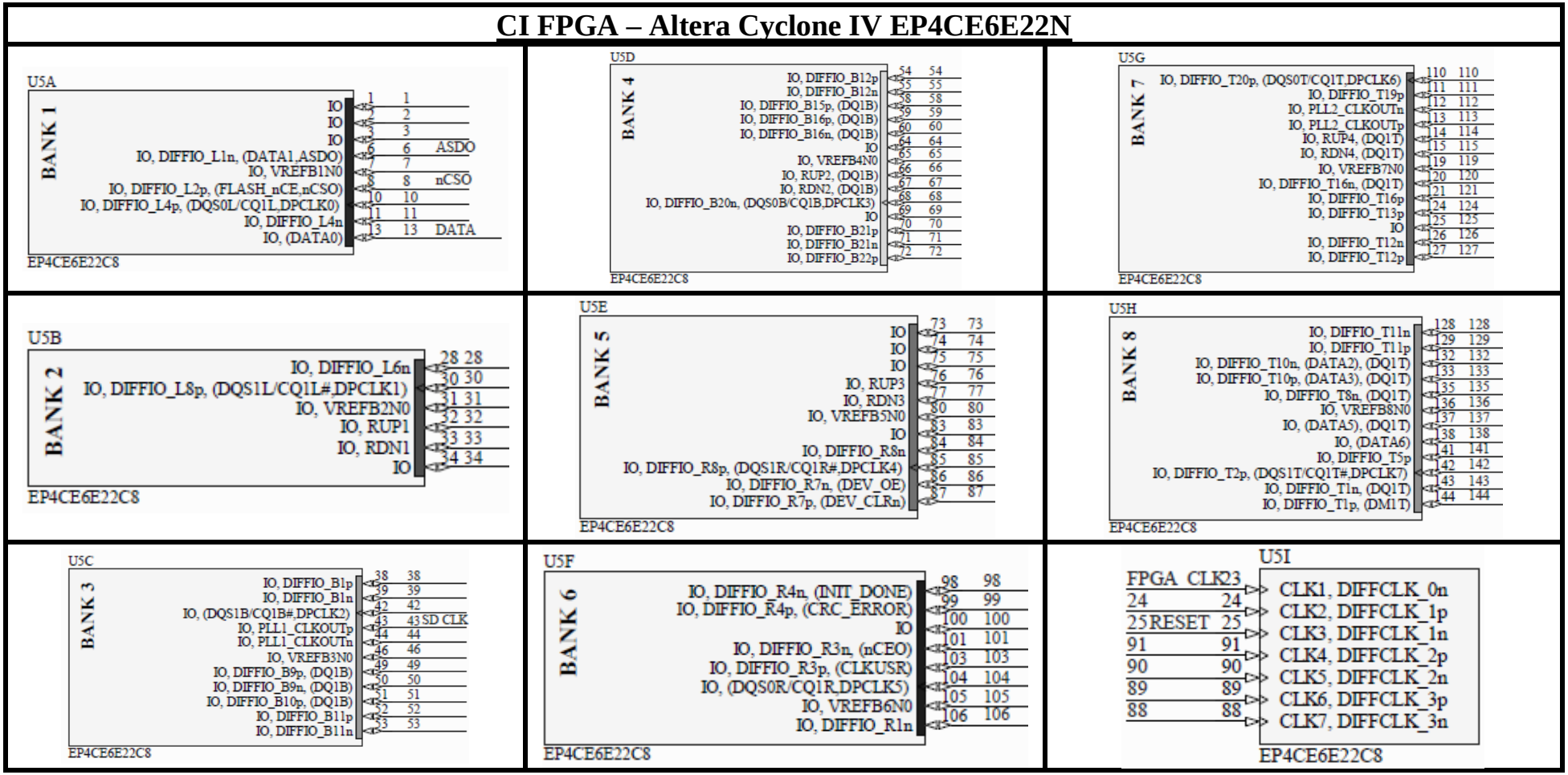

P3
GND
GND
LED1 84
LED3 86
KEY1 88
KEY3 90
I2C_SDA 98
IR 100
VGA_VSYNC 103
VGA_G 105
85 LED2
87 LED4
89 KEY2
91 KEY4
99 I2C_SCL
101 VGA_HSYNC
104 VGA_B
106 VGA_R
5V
3.3V
P3 Header 10X2


LCD 1602 12864
5V
VBG
5V
LCD11
LCD10
LCD9
LCD8
LCD7
LCD6
LCD5
LCD4
LCD3
LCD2
LCD1
LCD
1602/12864
5V
10K
RW
2 VBG
R29
1K


AT24C08
3.3V
5.1K
R25
5.1K
R26
U8
A0 VCC
A1 WP
A2 SCL
GND SDA
I2C_SCL
I2C_SDA
AT24C08
EEPROM


3.3V
LM75
5.1K
R27
5.1K
R28
U9
SDA
SCL
OS
GND
SDA VCC
SCL A0
OS A1
GND A2
3.3V
LM75
GND
GND
Sensor Temp.

CI FPGA – Altera Cyclone IV EP4CE6E22N



CI FPGA – Altera Cyclone IV EP4CE6E22N (Cont.)