Salvar um programa na memória flash do kit RZ-EasyFPGA A2.2:

- Ao enviar o programa compilado para a memória flash, quando a placa FPGA for desligada e religada novamente, o programa será mantido na memória da placa.

- Se houver um programa sdalvo nessa memória, então assim que a placa FPGA for ligada, o programa salvo nela começará a ser executado.

1 - Criar o arquivo `.jic`

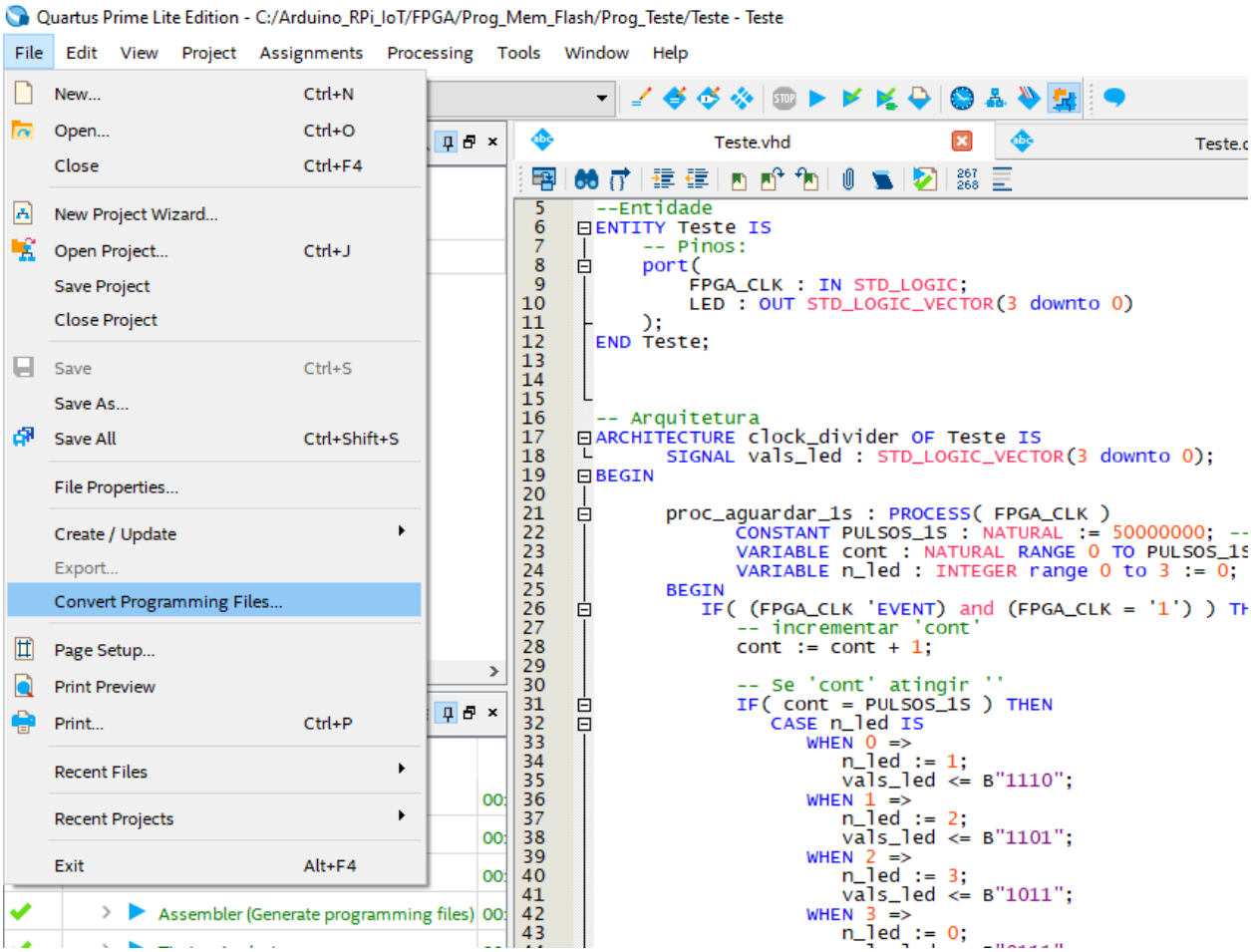

Figure 1: 1.1 - `File/Convert Programming Files...`

2 - Enviar o programa para a memória compilada

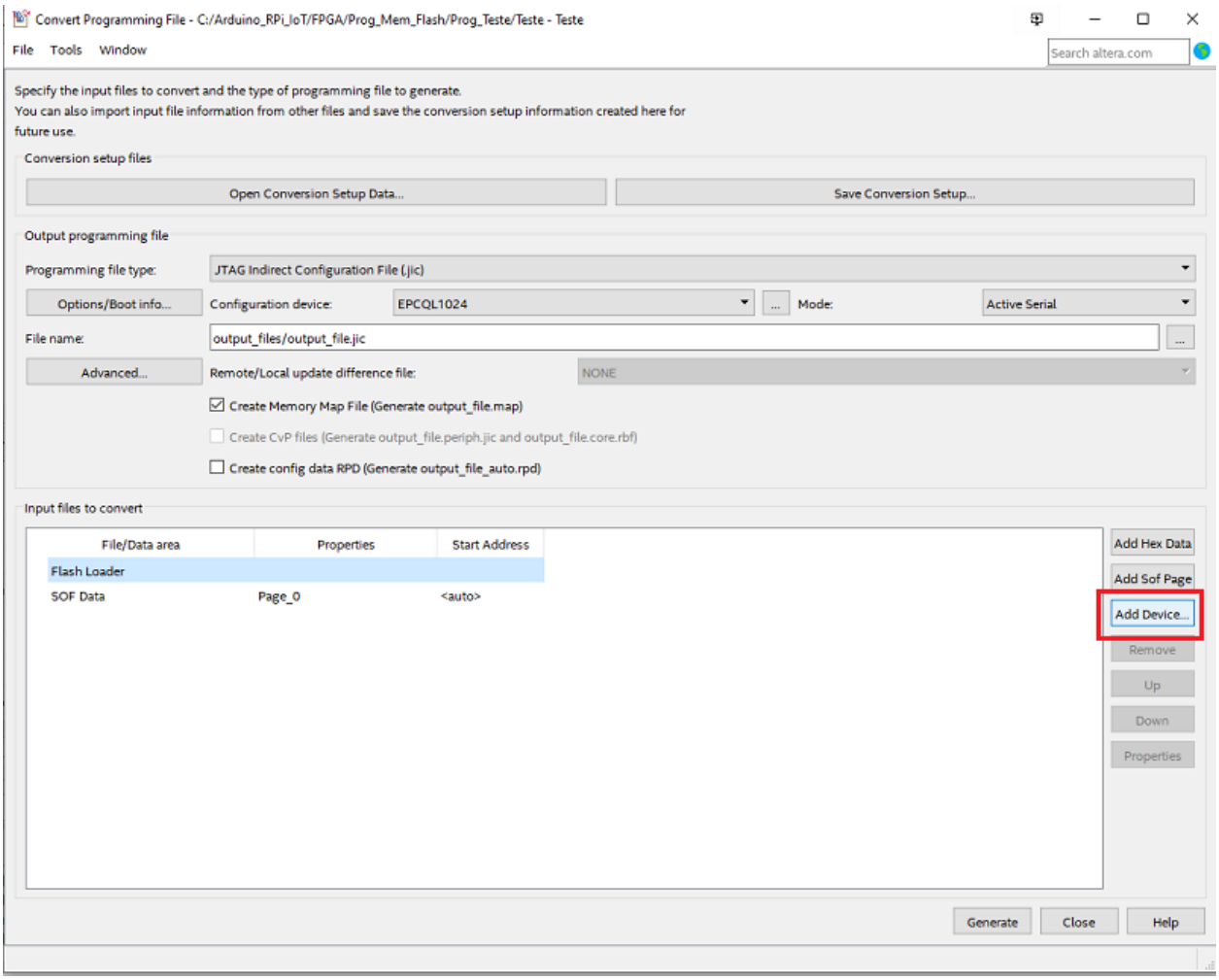

Figure 2: 1.2 - Adicionar dispositivo

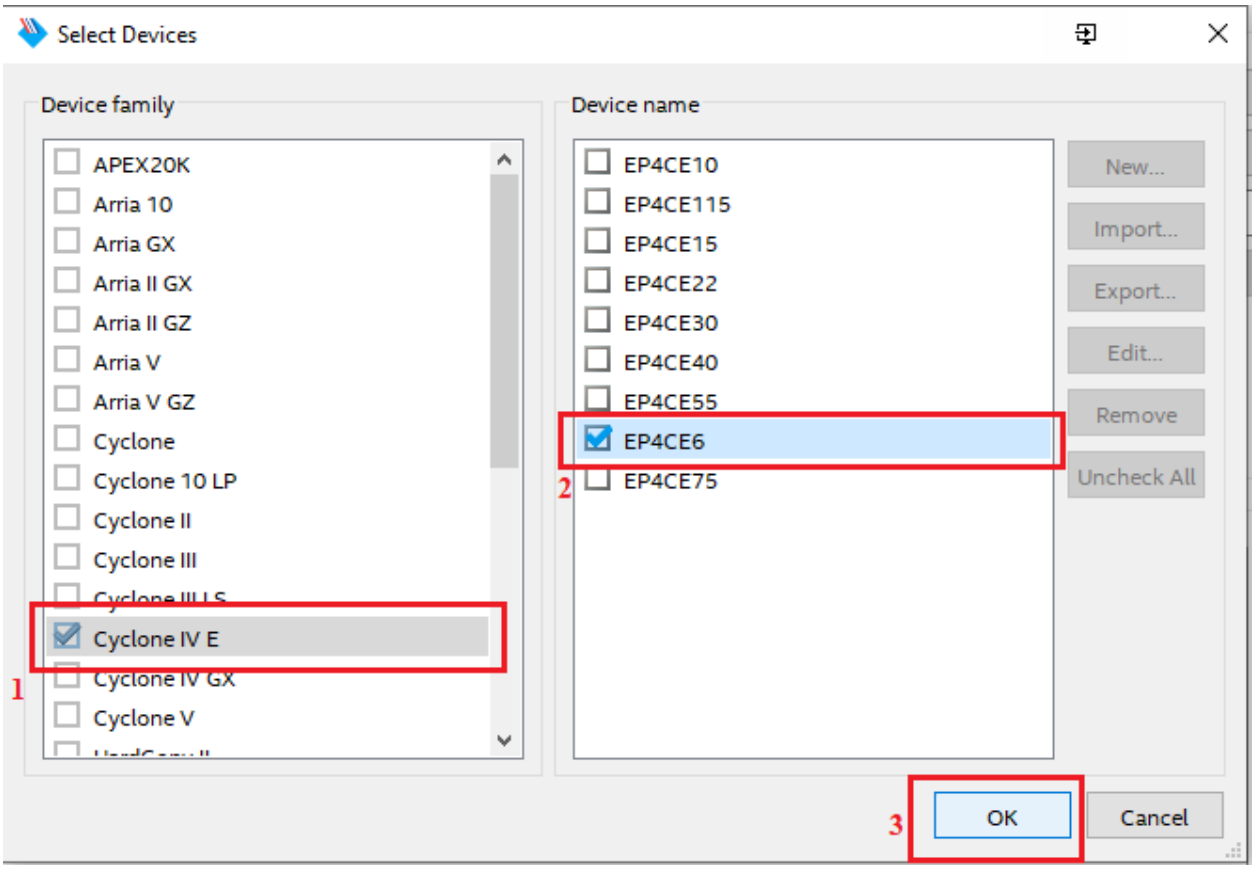

Figure 3: 1.3 - Selecionar o dispositivo Cyclone IV

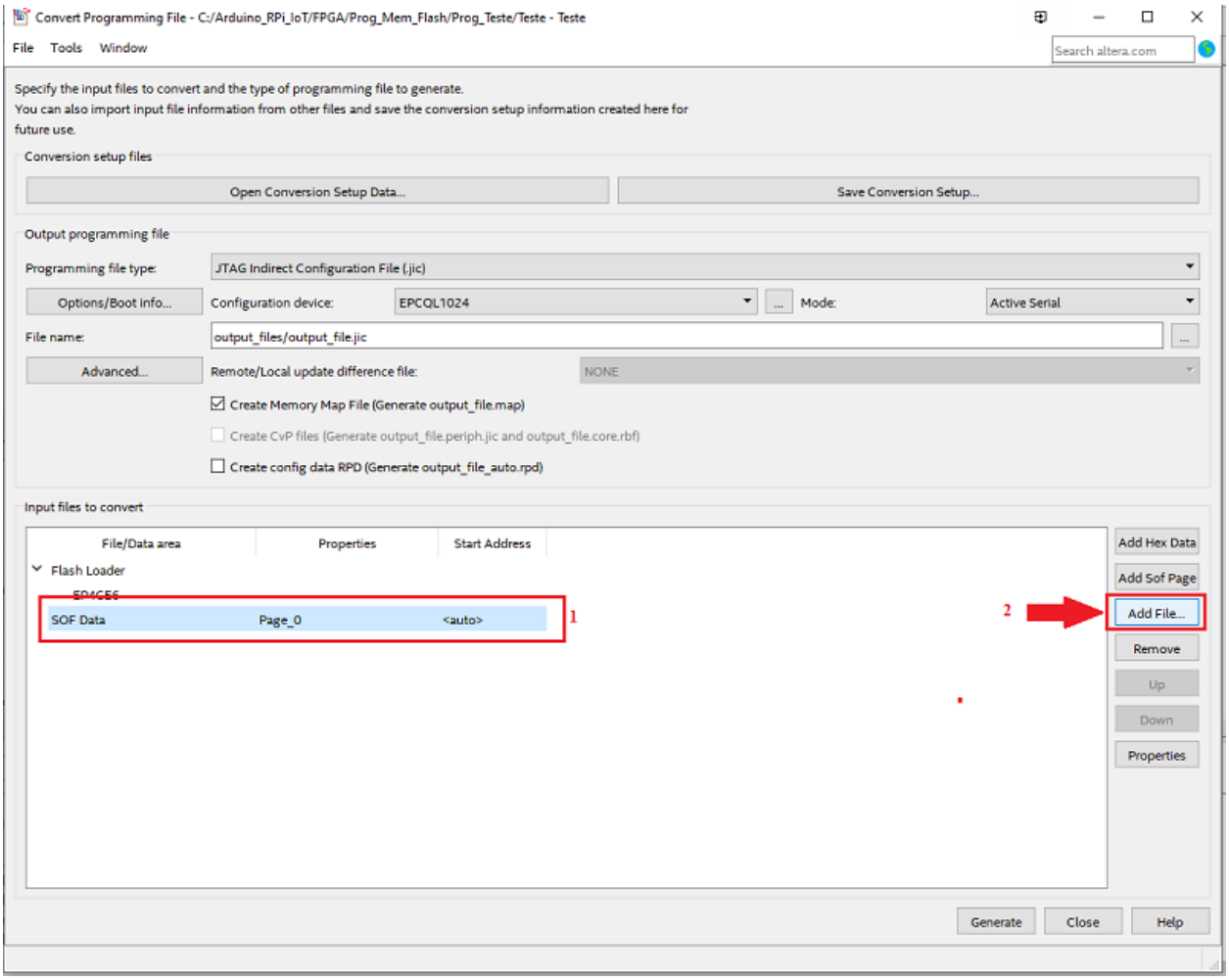

Figure 4: 1.4 - Adicionar o arquivo `.sof`

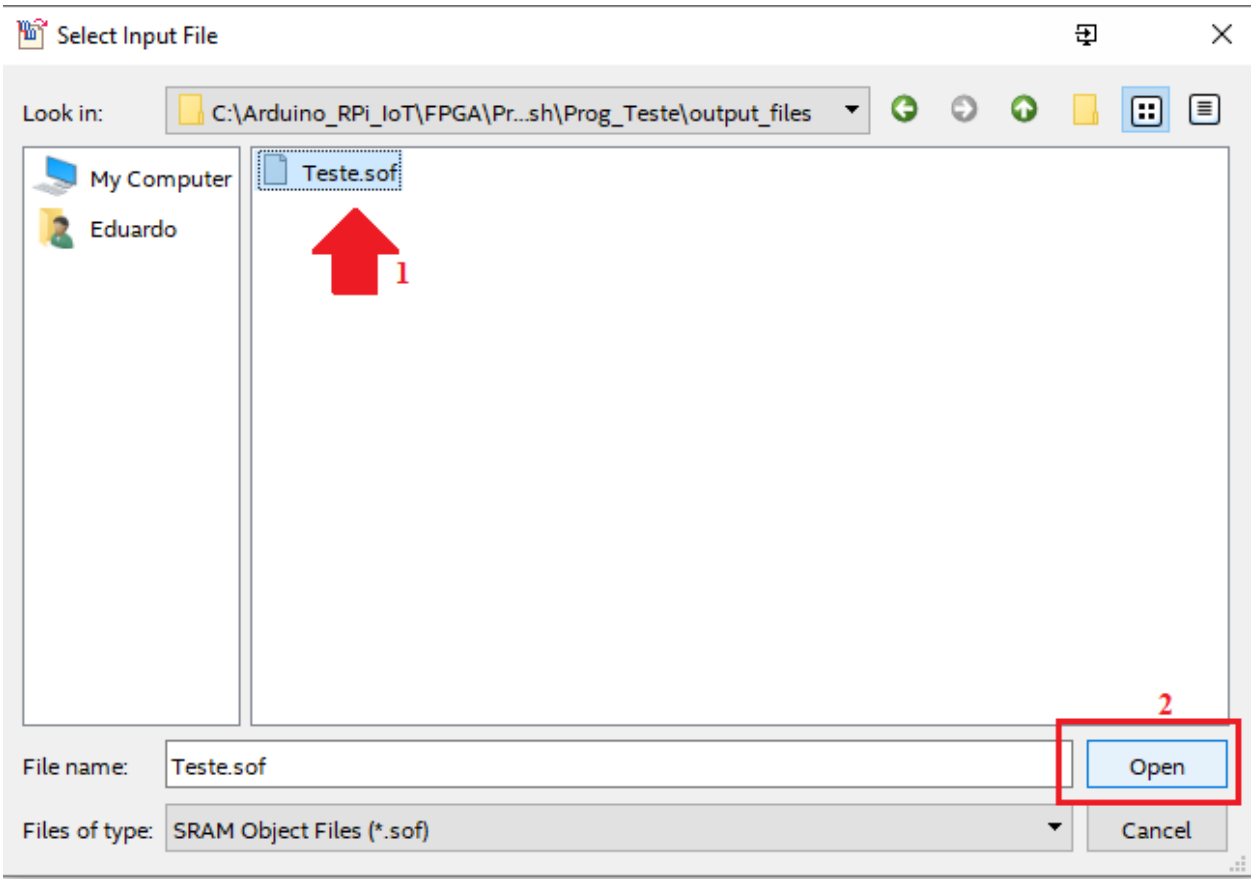

Figure 5: 1.5 - Adicionar o arquivo `.sof`

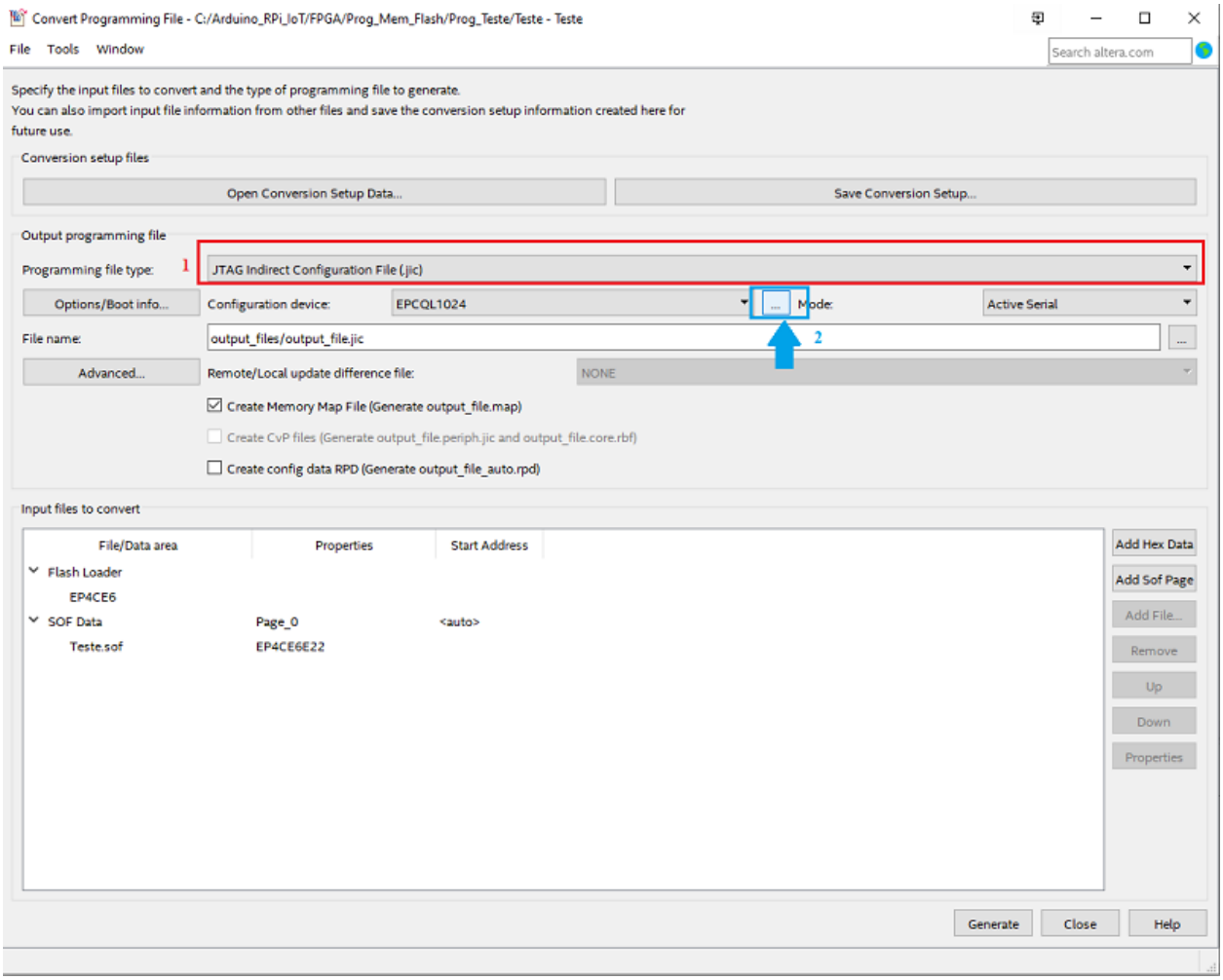

Figure 6: 1.6 - Selecionar a saída para `.jic`

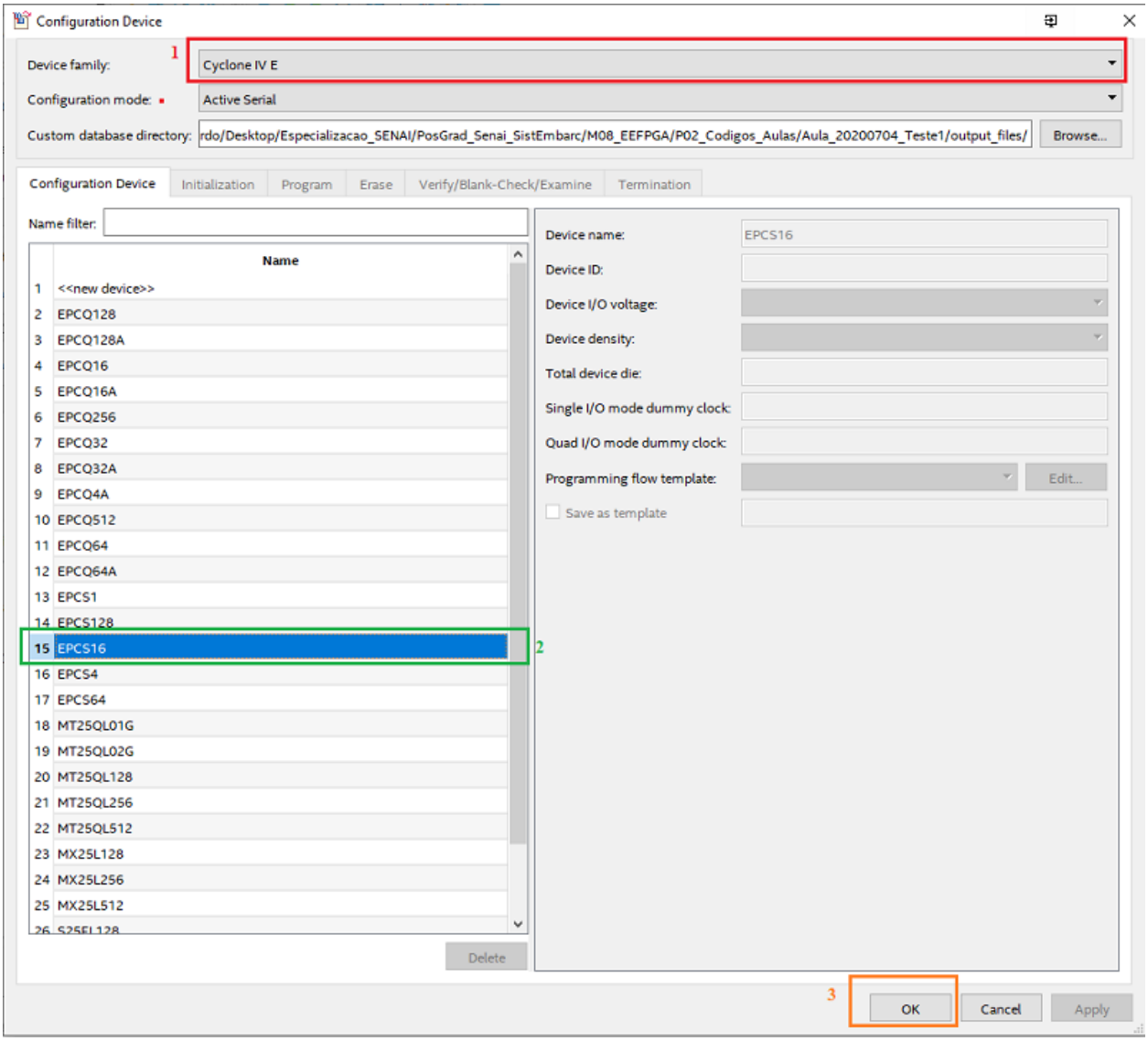

Figure 7: 1.7 - Selecionar o dispositivo de memória da placa FPGA

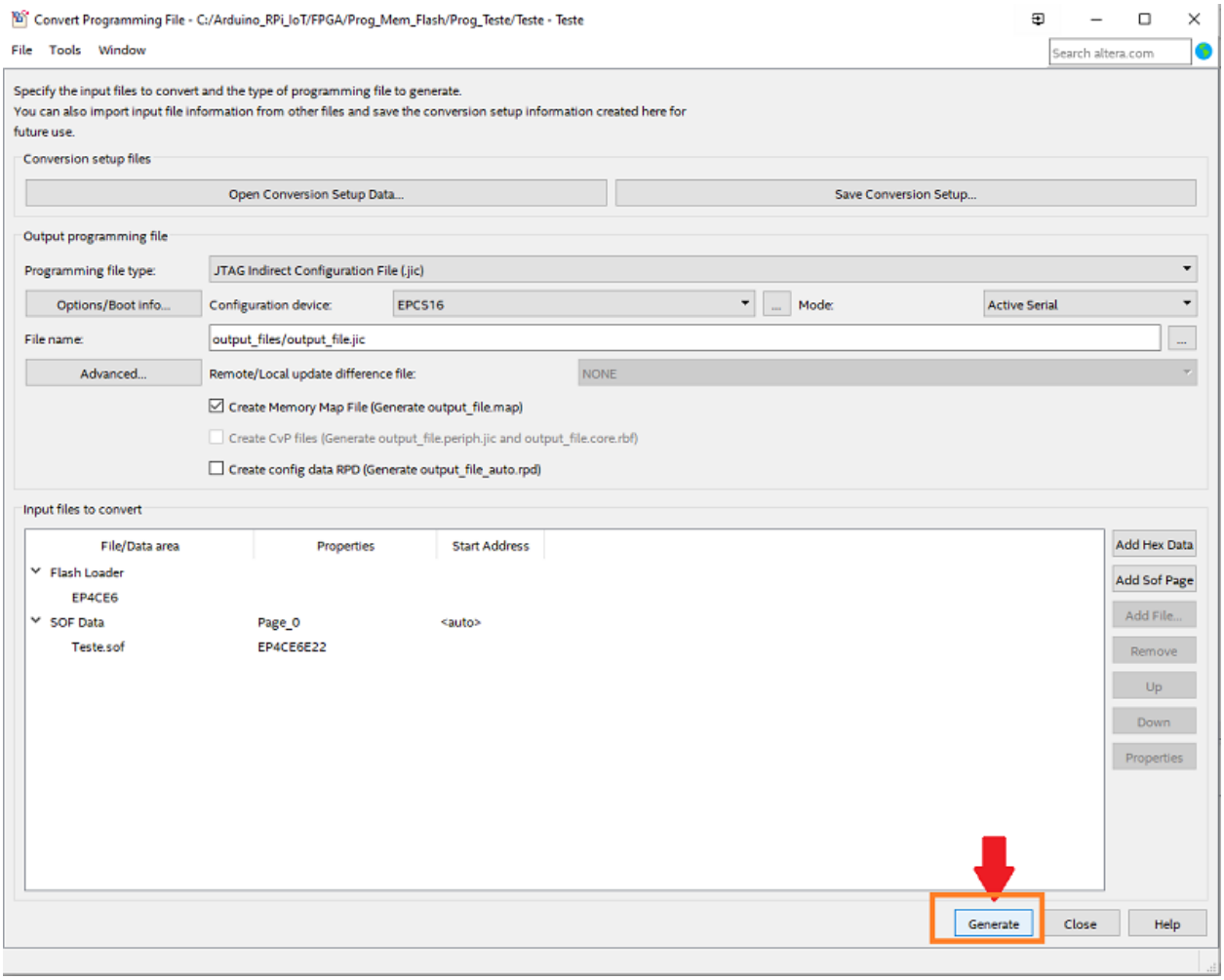

Figure 8: 1.8 - Gerar o arquivo `.jic`

Figure 9: 2.1 - Selecionar a janela de programação

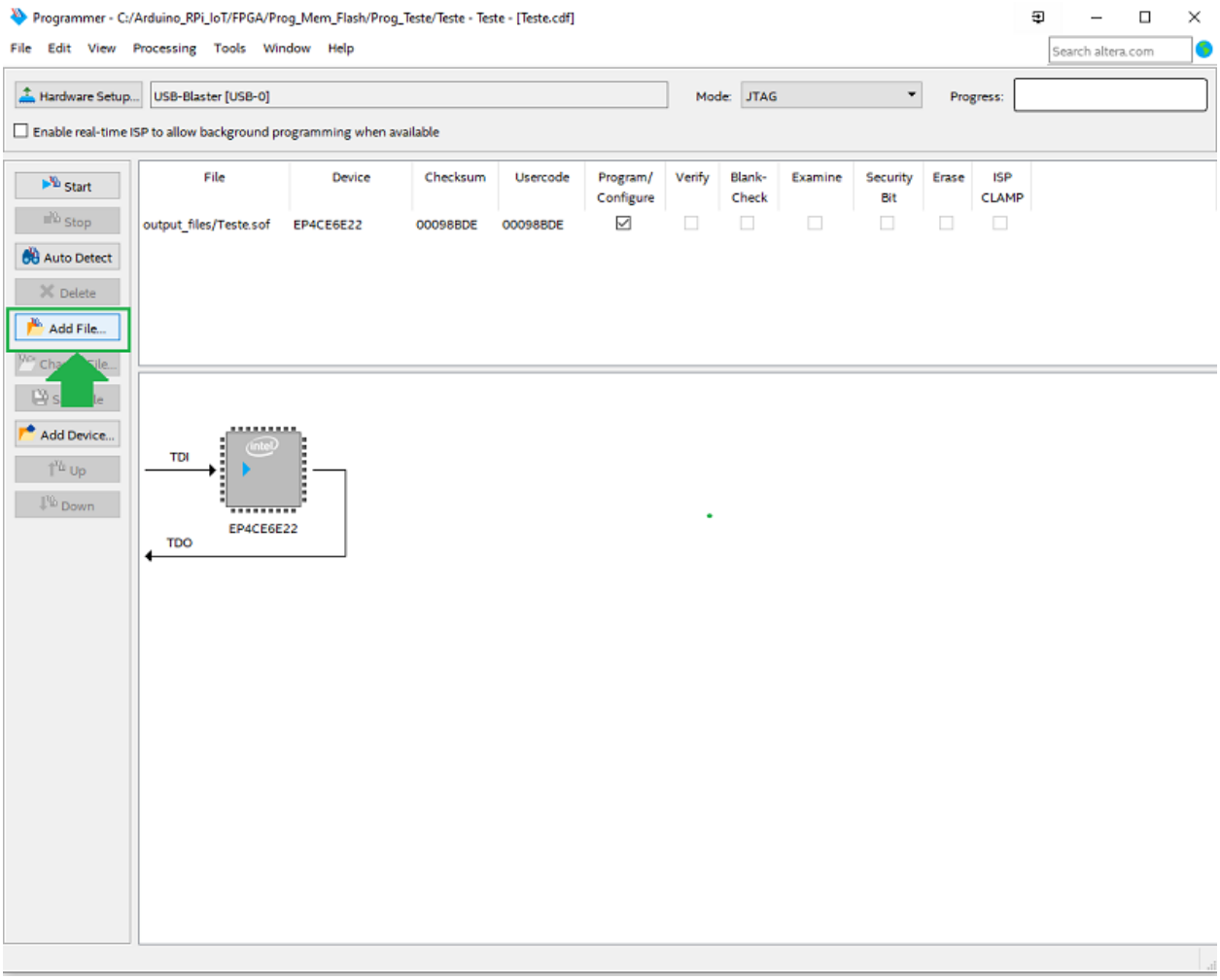

Figure 10: 2.2 - Selecionar o arquivo `.jic`

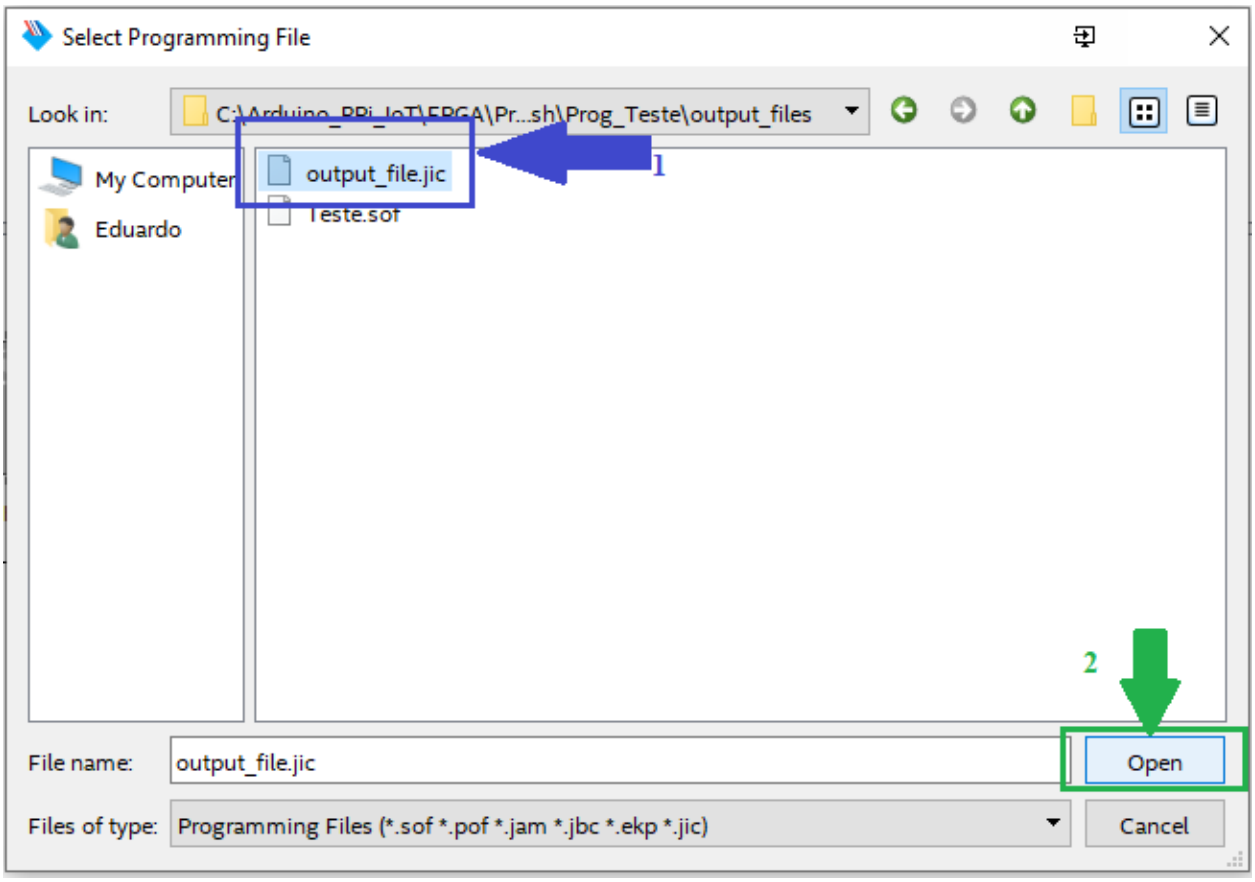

Figure 11: 2.3 - Selecionar o arquivo `.jic`

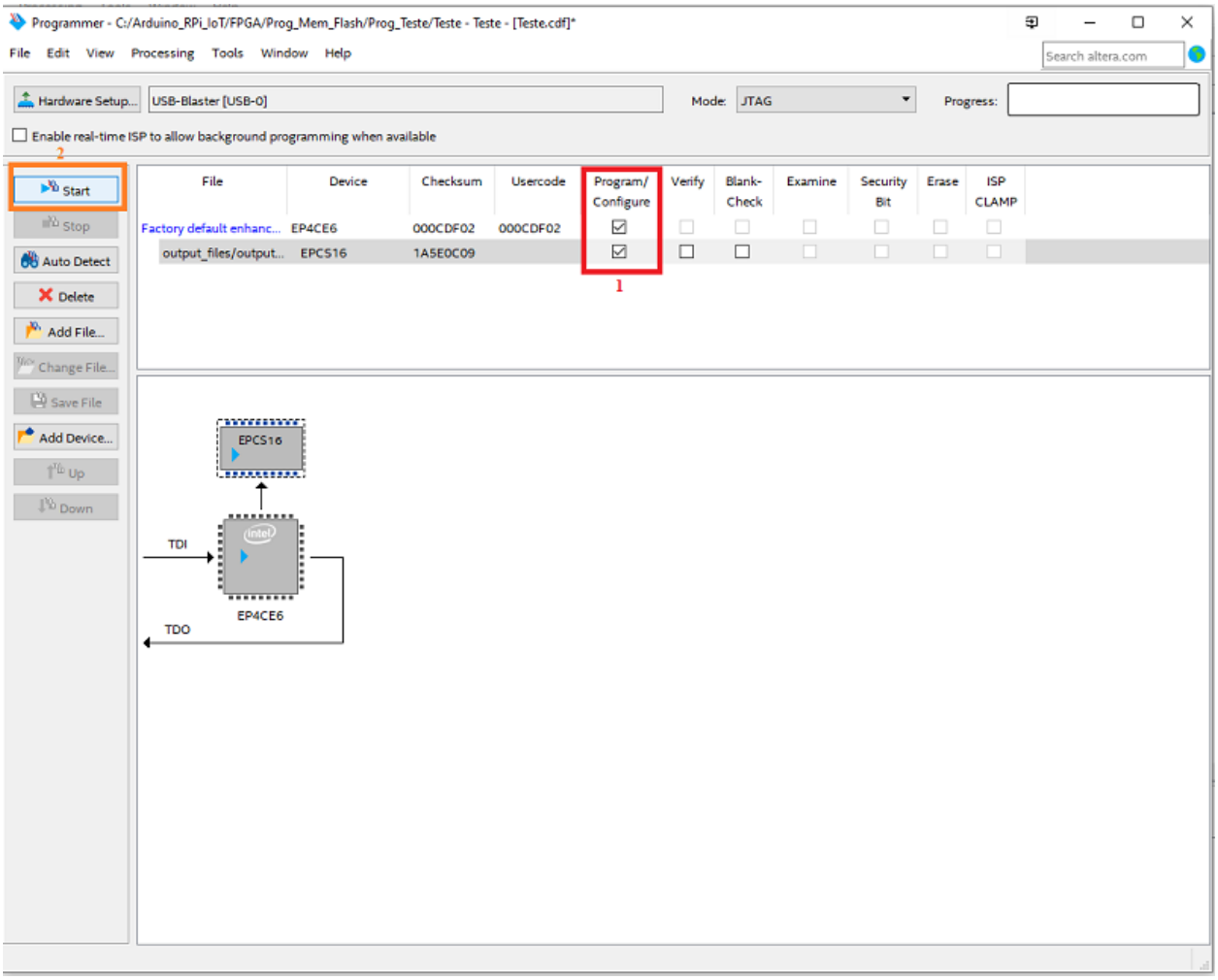

Figure 12: 2.4 - Enviar o programa para a memória do dispositivo FPGA

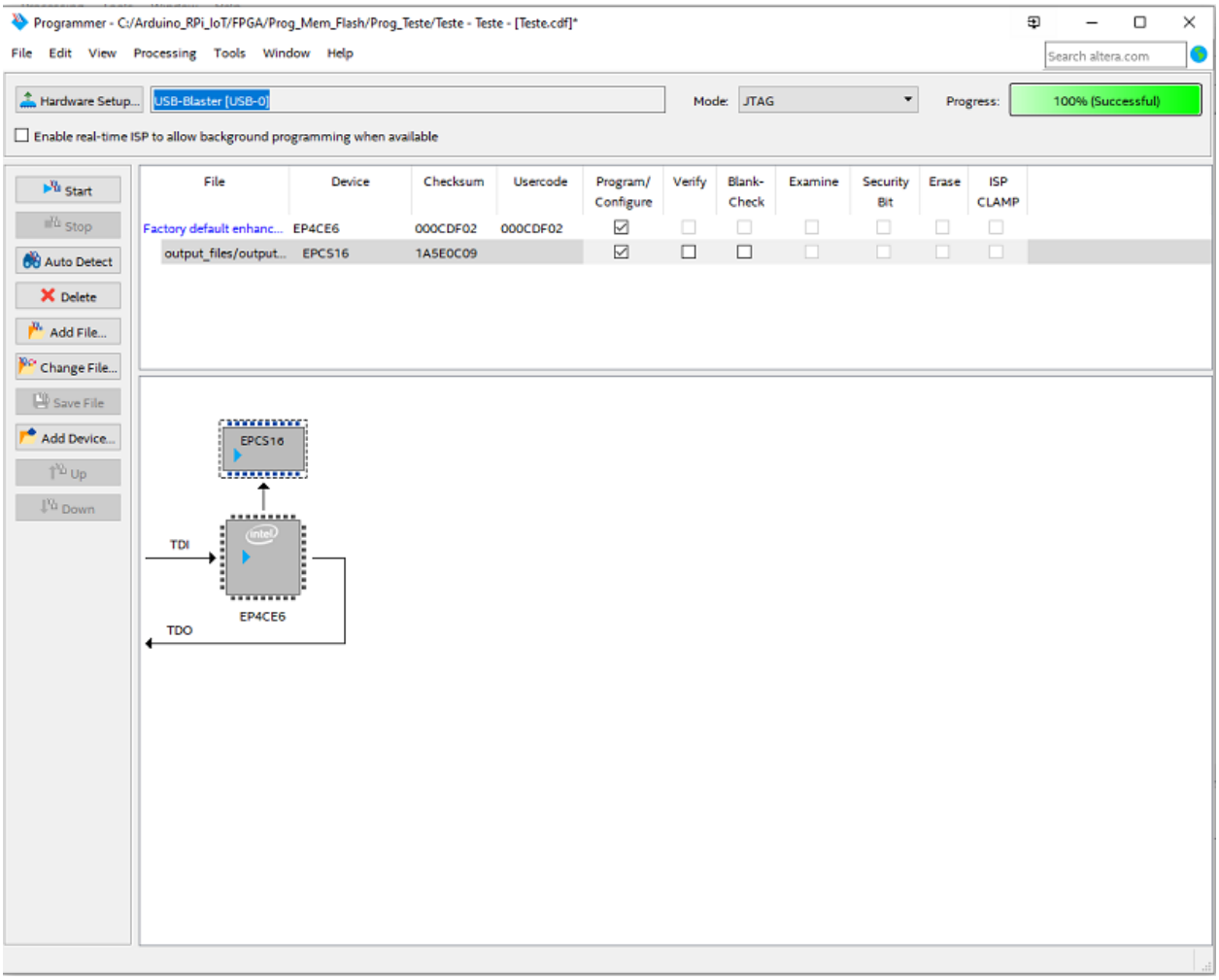

Figure 13: 2.5 - Pronto!