CUSTOMER PRODUCT SPECIFICATION (CPS)

LightView™ 201k Digital Display Module

Model LDM-0201-E3A

Revision 1

Displaytech, Inc.

2602 Clover Basin Drive

Longmont, Colorado 80503-7604 USA

303-772-2191

303-772-2193 fax

800-397-8121 USA toll free

LV201support@displaytech.com

www.displaytech.com

DisplayTECH®

Table of Contents

List of Tables

List of Figures

Introduction

This specification provides a detailed technical description of the Displaytech LightView™ 201k Digital Display Module, Model LDM-0201-E3A and offers the basic information needed to integrate the Display Module into viewfinder and other display applications. The document is divided into seven primary sections: introduction, display module overview, optical specification, mechanical specification, electrical specification, product quality, and applicable standards.

Product Description

The Displaytech LightView™ 201k Digital Display Module is a compact, low power offering primarily designed for color digital still camera and video camcorder electronic viewfinders. The module provides an integrated display solution, incorporating the display panel, illumination, polarization optics, and control circuitry in a compact opto-mechanical package. This product takes advantage of the fast switching speeds and superior optical qualities of Displaytech's patented Ferroelectric Liquid Crystal (FLC) materials, delivering high quality images free of motion smearing. The product is capable of showing up to 4.2 Million colors, obtained through color sequential mode of operation. With a power target of 90 mW at 120 Hz frame rate, this high brightness display module delivers 250 cd/m^2. Industry standard digital interfaces are supported to provide an easily integrated, high performance solution for camcorder and digital still camera customers, as well as for other high-tech display applications.

Table 1 summarizes the key parameters that describe the LDM-0201-E3A Display Module. In the sections following, details behind each of the parameters will be provided as well as additional information on the proper application of the Display Module.

Block Diagram

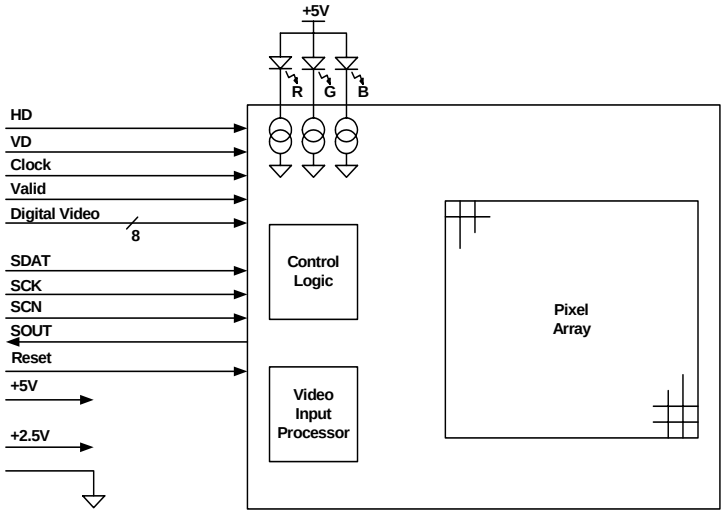

Figure 1: Block Diagram of LV201k Display Module

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Display Module Overview

The LV201k Display Module provides a compact solution for converting electronic video data into full color and high-quality live images. The main component of the LV201k Display Module is the low power Ferroelectric Liquid Crystal (FLC) reflective microdisplay panel. Light from a tri-color LED is directed towards the panel, and the light being reflected from the panel makes up images that can be viewed through a compact viewfinder lens system. A schematic drawing of how the display module works can be seen in Figure 2 below. The red, green and blue light from the LED is polarized and reflected by a polarizing beam splitter (PBS) onto the display panel. The light also passes through a pre-polarizer and diffuser to avoid stray light of unwanted polarization and to create an even illumination of the panel. The panel assembly consists of a reflective silicon backplane, a layer of ferroelectric liquid crystal, and a glass cover. The video data is fed to the silicon backplane controlling the voltage applied to its top reflective and pixelated surface. The voltage determines the orientation of the liquid crystal molecules, which in turn determines the polarization state of the light reflected from the panel. The polarizing beam splitter will only transmit one type of polarization, thereby creating bright or dark pixels according to the voltage that was applied to the pixels (P-polarized light is transmitted in and S-polarized light is reflected, as shown in Figure 2). The light transmitted through the polarizing beam splitter is typically captured by a lens system magnifying the image before it reaches the observer.

The display module works in a color sequential mode, which means that the image data for the colors red, green and blue are shown as three separate image fields in time. The human eye then integrates the three color images to produce the intended image and final color. To achieve this, the LED only emits one color at a time, and during that time the corresponding image data is shown on the display panel. This is done at a very high frequency in the LV201k Display Module, typically at a frequency of 120 Hz (360 Hz RGB field rate).

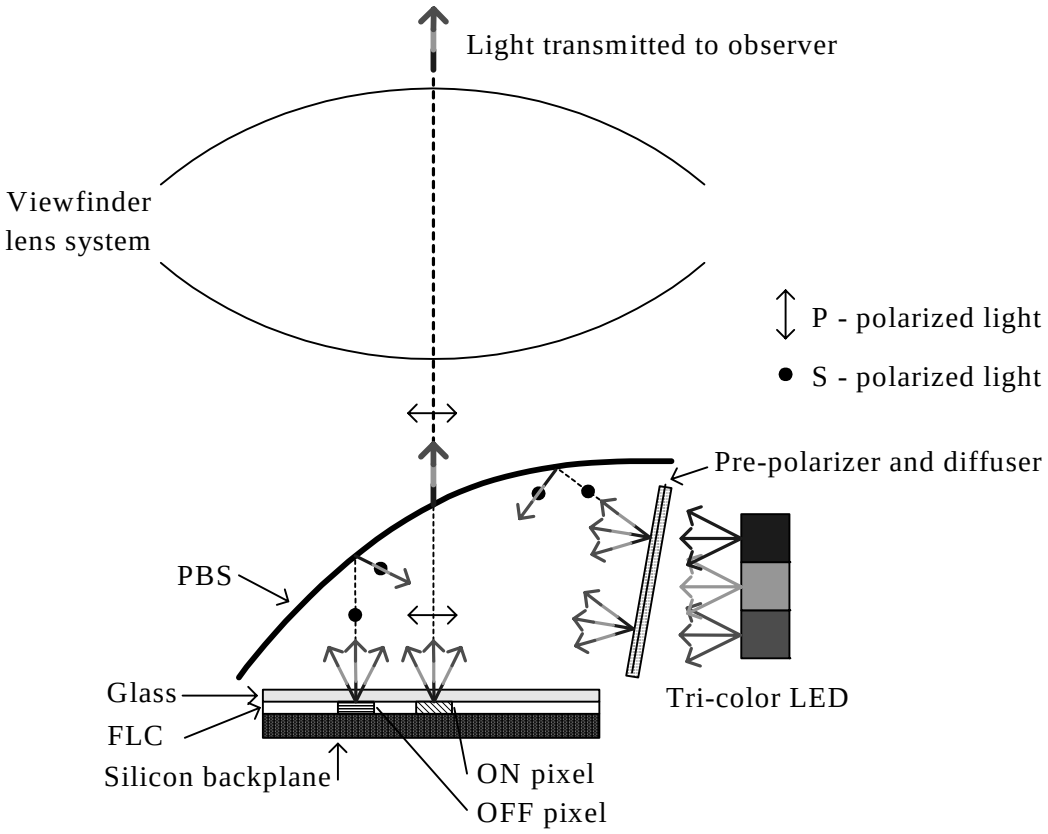

Figure 2: Pictorial of LV201k Display Module

(Note: Viewfinder lens system is not included as part of the LV201k Display Module assembly.)

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Specification Summary

Parameter	Specification
Display technology	Ferroelectric Liquid Crystal (FLC) on reflective CMOS
Display mode	Field sequential color
Display format	300 (H) x 224 (V)
Display panel active area	4.05 x 3.02 mm (4:3 aspect ratio)
Display panel diagonal	5.0 mm (0.20”)
Input Grayscale	256 levels
Display pixel pitch	13.5 μm
Pixel fill factor	94%
Color depth	4.2Million unique colors (YCrCb video interface)
Display frame rate	120 Hz (NTSC), 100 Hz (PAL)
Data clock rate	27 MHz
Display Module luminance[1]	250 cd/m^2 maximum, adjustable to 1/64th of full scale
Contrast ratio[1]	80:1
White point[1]	Color temperature target is 6500 K
Display Module exit pupil location	60 mm behind the microdisplay
Display Module exit pupil dimensions	Square, 18.75 x 18.75 mm
Digital display interface	CCIR 601 CCIR 656 RGB-serial (8 data, H_d, V_d, Valid, Clock)
Control interface	4 wire serial
Operating supply voltages	2.5 V (core), 5.0 V (LED), Analog
Power consumption[1]	90 mW
Dimensions (L x W x H)[2]	15.2 x 11.3 x 9.2 mm
Weight	1.0 g approximately
Operating temperature	-10 °C to 70 °C
Storage temperature	-30 °C to 83 °C

[1]Typical values at 60 Hz NTSC (gamma correction of 2.1), CCIR-601 operation with flat field video pattern at room temperature

[2]Dimensions shown do not include flex circuit. Refer to Figure 4 for details.

Table 1: Specifications for LDM-0201-E3A Digital Display Module

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Optical Specification

The Display Module optical system consists of a low power tri-color LED package, the FLC reflective microdisplay panel, and the illuminator. The passive optical components of the illuminator control the microdisplay illumination and observation. A viewing lens is not supplied as part of the Display Module assembly.

In comparison to conventional backlighting systems, the integral, low power LED package of the Display Module reduces manufacturing costs and prolongs the life of the battery. The individual LEDs are turned on in a sequence. Sequential control of the FLC ON and OFF states relative to the LED's ON and OFF states defines the microdisplay color at individual pixels of the FLC microdisplay panel. A PBS in the illuminator assembly separates the illumination optical path from the imaging optical path. The PBS reflects one polarization while transmitting the other. Diffused linearly polarized light from a pre-polarizing diffuser reflects off the PBS to the FLC microdisplay panel. The state of each pixel controls the state of the FLC polarization. When the pixel is in the ON state, the FLC rotates the linear polarization of the incident beam maximizing the light transmitted by the PBS toward a viewer. When the pixel is in the OFF state, the FLC does not rotate the linear polarization of the incident beam which in turn, minimizes the light transmitted.

Individual LED white point calibrations are programmed into the EEPROM of each Display Module. These calibrations are read at each power up sequence of the Display Module to ensure proper color balancing during operation. The values for the LED calibration points depend not only on the individual LEDs but also on other Display module optical components. The individual red, green, and blue LED currents are determined algorithmically to produce the best white image during final test calibration in the manufacturing process. Following the setting of these calibration points, the maximum luminance white and minimum luminance dark fields are measured and the Display Module contrast is determined as the ratio of the white state luminance level over the dark state luminance level.

The Display Module parameters important for the viewing lens design are specified in the section, "Optical Interface".

Photometric Test Methods

A spectrophotometer is used to photometrically evaluate the white and dark images produced by the Display Module. To assess the white state luminous level the Display Module is driven to the full white state by applying a 60 Hz, NTSC (gamma correction of 2.1), CCIR-601, flat field white video pattern at room temperature, where Y=EBh, Cr=80h, and Cb=80h. Similarly, to assess the dark state luminous level the Display Module is driven to the full dark state by applying a 60 Hz, NTSC, CCIR-601, flat field black video pattern at room temperature, where Y=10h, Cr=80h, and Cb=80h. A pulse width modulation of the LED drive is used to set the overall brightness of the Display Module. See Appendix B: Registers. In both of the previous cases the pulse width modulation was set to 100%. The contrast is determined as the ratio of the measured white state luminance level over the dark state luminance level. (Note: Both display brightness and contrast is to some extent dependent on the gamma correction settings, and all specifications listed are valid with a gamma of 2.1). The color temperature is determined by the spectrophotometer while sampling the white state luminance. Table 2 below specifies the Display Module photometric values:

Test	Minimum	Typical	Maximum	Unit
"Full On" White State Level[1]	100	250	300	cd/m^2
Contrast Ratio[1]	30:1	80:1	-	-
Color Temperature[1]	6000	6500	9000	K

Table 2: Optical Parameters and Test Methods

[1]Typical Values at 60 Hz NTSC (gamma correction of 2.1), CCIR-601 operation with flat field video pattern at room temperature

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Optical Interface

The viewing lens needs to image a color rectangular microdisplay of 4.05 by 3.02 mm adjacent to the bottom surface of a cover glass plate behind the curved PBS film. The lens also needs to mask the bright pre-polarizing diffuser inside the Display Module that illuminates the microdisplay. The pre-polarizing diffuser is located in the lens object space periphery between the microdisplay and the lens. The cross-sectional view of the lens object space is illustrated in Figure 3. The masking aperture shown in Figure 3 is not part of the Display Module. It must be supplied as part of the viewing lens.

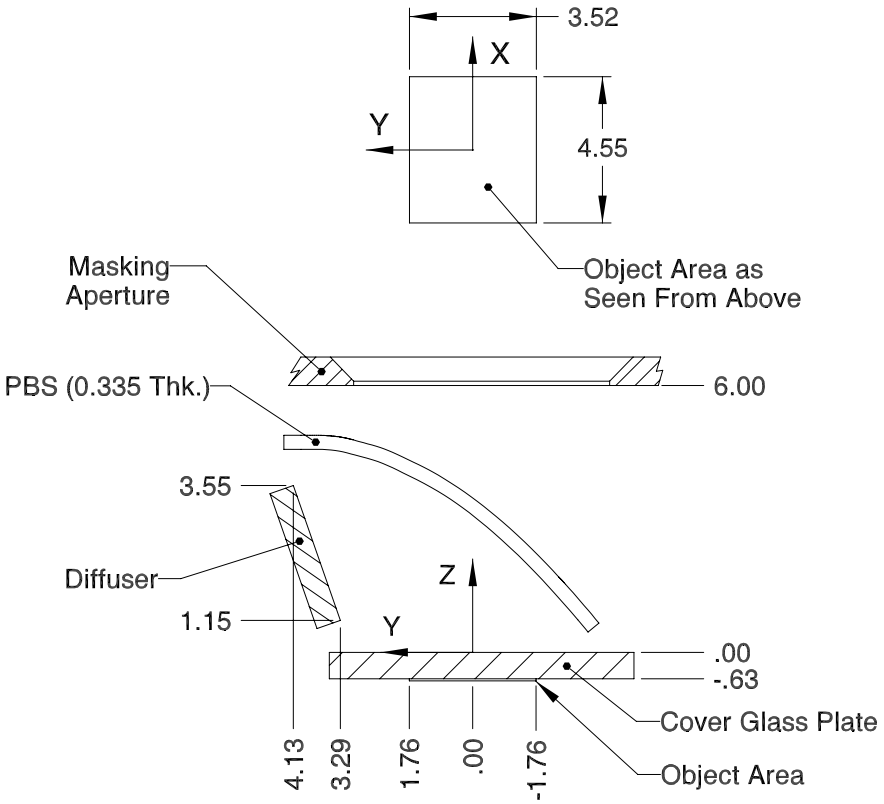

Figure 3: Optical Components In the Viewing Lens Object Space

(All dimensions in millimeters)

	surface facing to cover plate	*surface facing to lens*
Y-Z plane radius	-5.3743 mm	-5.7020 mm
Y-Z plane conic constant	-1.2169	-1.1749
Z distance (before decenter and tilt)	4.8070 mm	5.1413 mm
Y decenter (before tilt)	3.6927 mm	3.6701 mm
Tilt about X-axis (rotate surface toward cover plate)	3.8567 deg	3.8567 deg

Table 3: Specifications for PBS Shape and Location

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

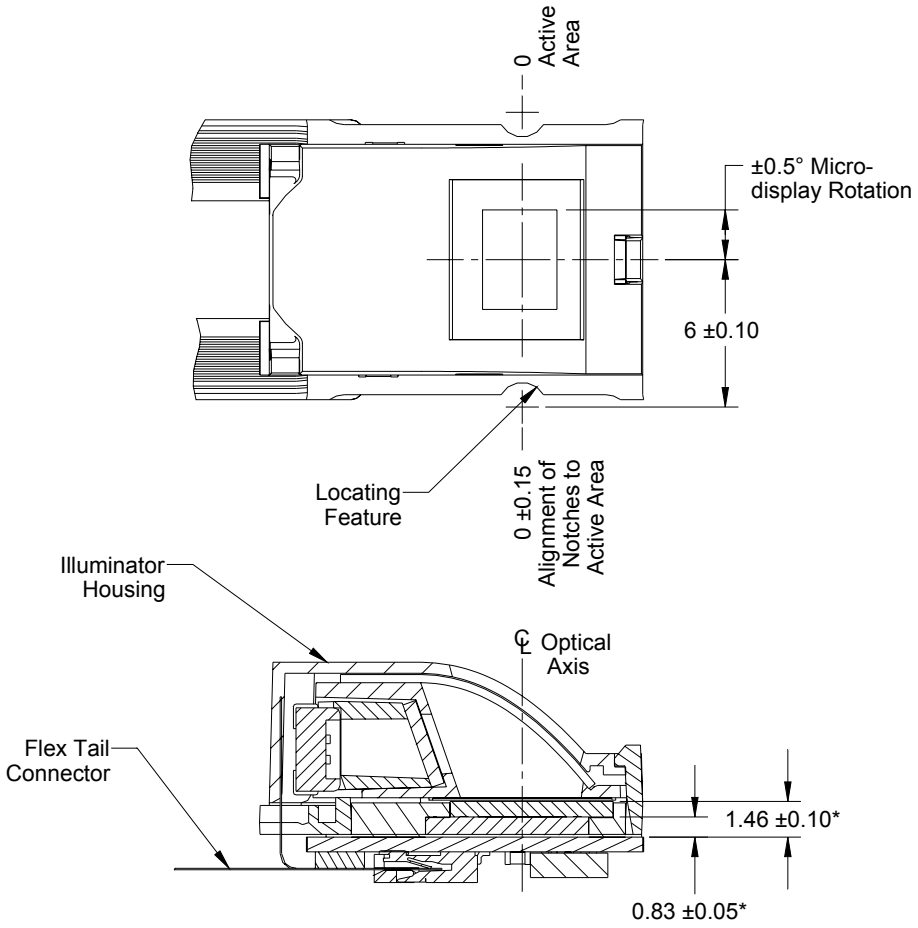

Figure 4: Display Module Location Features

(Dimensions with asterisks are referenced to the top surface of the PCB assembly)

(All dimensions in millimeters)

Light Spectra

The microdisplay uses a tri-color LED to create truly vivid colors. The LED spectra peak at 465, 523 and 628 nm and have FWHMs (Full Width Half Maximum) of 25, 33 and 16 nm, respectively.

Microdisplay Resolution

The rectangular microdisplay of 4.05 by 3.02 mm consists of 300 by 224 pixels of 0.0135 mm (pixel dimensions include a 0.0005 mm interpixel gap). This means that the viewing lens cutoff frequency should be above 37 lines/mm. The individual pixels have a hexagon shape, with each row being offset from the previous row. Figure 5 shows details of the pixel layout, including corner and edge pixel shape.

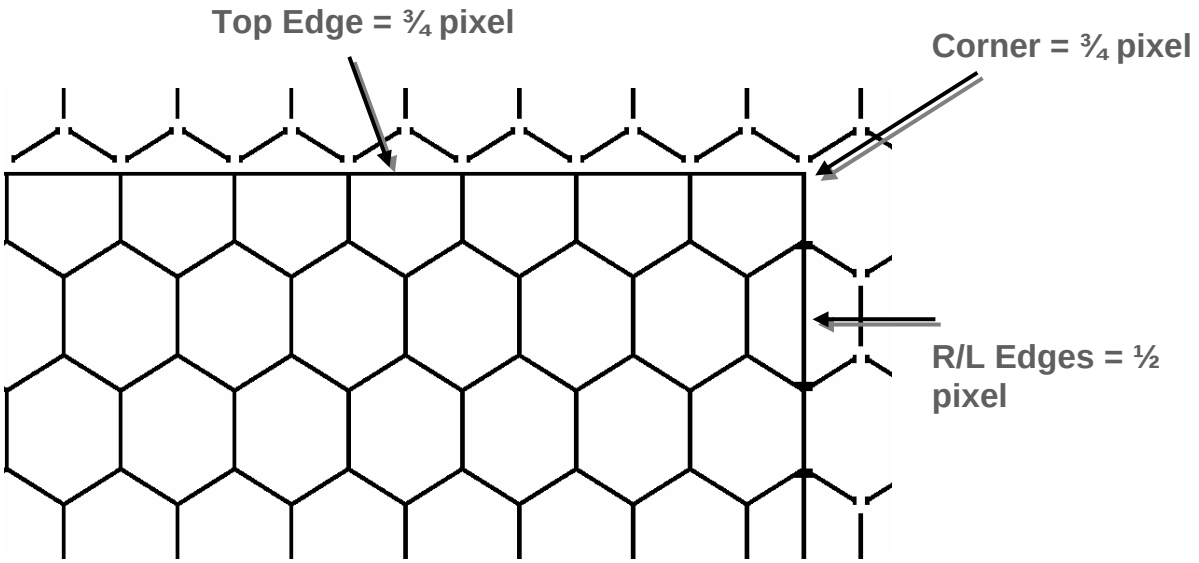

Figure 5: Display Module Pixel Layout

Microdisplay Location

The microdisplay axial position is referenced to the top surface of the Display Module FPCA with an accuracy of +/-0.15 mm. The lateral position of the microdisplay is referenced to locating features on the FPCA as shown in Figure 3. It's controlled with an accuracy of +/-0.15 mm. The position of the lens housing should be restrained by using the locating features. When considering the overall lateral performance required of the lens, the lens designer must take into account the lateral tolerance of the microdisplay relative to the FPCA and the lateral tolerance of the lens housing relative to the location of the lens optical axis. Combining these two tolerances will yield an increase in the lens object area from 4.05 by 3.02 mm to 4.35+2*T by 3.32+2*T mm, where +/-T mm is the lens housing tolerance. The Display Module illuminator will accommodate an object area of up to 4.55 by 3.52 mm as shown in Figure 3. This would require the optical axis to be centered within the lens housing with an accuracy of not worse than T = +/-0.10 mm.

The cover plate is made of Corning EAGLE 2000 glass. The plate thickness is 0.63+/-0.05 mm. The curved PBS film is 0.335 mm thick and its effective refractive index is 1.60. The dispersion is unspecified. The position and shape of the PBS film is specified in Table 3 with reference to the cross sectional view in Figure 3. Note that the Z-axis coincides with the optical axis, the plane Z=0 coincides with the cover plate top surface and the object (microdisplay) plane coincides with the cover plate bottom surface at Z=-0.63 mm.

Display Module Exit Pupil and Masking Aperture

The Display Module exit pupil is a square of 18.75 by 18.75 mm that is 60 mm away from the microdisplay, on the side opposite to the viewing lens. Each point of the rectangular object area of 4.55 by 3.52 mm sends a divergent beam toward the viewing lens. The beam shape is defined by its apex at the object area point and by its rectangular base coinciding with the square exit pupil of the Display Module. If the lens entrance pupil is located at the Display Module exit pupil plane and the whole lens pupil is within the Display Module exit pupil area then there will be absolutely no beam vignetting due to the Display Module illuminator. Otherwise, there could be some partial beam obscuration attributed to the Display Module illuminator dependent on the location and the size of the viewing lens entrance pupil.

Knowing the locations and the sizes of the object and the Display Module exit pupil, the lens designer can unambiguously determine the magnitude of the obstruction of the individual object beams at the desired exit pupil of the viewing lens of a chosen design and magnification. If, for instance, the desired exit pupil diameter of the viewing lens is 5 mm, then the Display Module illuminator could support the imaging without vignetting for fairly large eye relief and the viewing lens magnification up to 16X giving a field of view of about 18 degrees. If for the same size exit pupil a reasonable partial beam obscuration is allowed (including a partial obscuration of the beam from the on-axis point), then we expect that the illuminator could support viewing lens magnifications up to 22X giving the field of view of about 25 degrees.

The function of the masking aperture, which has to be supplied with the viewing lens, is to mask the bright illuminator diffuser without significantly increasing vignetting. The coordinates of the top and bottom edges of the rectangular diffuser are defined in Figure 3. The masking aperture should preferably be centered relative to the rectangular object area in a plane parallel to the microdisplay that is 7.48 mm above the Display Module FPCA and in front of the viewing lens (nominally 6.00 mm above the cover plate). The proper size of the masking aperture depends on the Display Module exit pupil, the object size, and on the viewing lens entrance pupil. For example, to avoid vignetting, the circular masking aperture that is located 6.00 mm above the cover plate and centered with respect to the optical axis should have a diameter of at least 5.94 mm. This assumes that the beams emerging from points located within the object area and limited by the Display Module exit pupil are not partially obstructed by the viewing lens. However, if the viewing lens itself would obscure beams, then the masking aperture diameter could be smaller without causing vignetting. To ensure that the diffuser won't be visible through the viewing lens exit pupil, all the diffuser points must be outside the surface one would get by connecting the masking aperture edge with the edge of the viewing lens entrance pupil. If the above requirement to mask the whole diffuser can not be satisfied because the entrance pupil is too large then the masking aperture has to be reduced and some vignetting by the masking aperture allowed. If the whole viewing lens entrance pupil will be inside the Display Module exit pupil area then the masking aperture 6.00 mm above the cover plate and of the diameter 5.94 mm will fully mask the diffuser and won't introduce any vignetting.

It is not necessary to use a circular masking aperture. A square aperture or, since the pre-polarizer diffuser is only on one side of the object, just a straight edge screen can work as well.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Mechanical Specification

The LV201k Display Module is a flexible printed circuit board based package, with detachable flex connection. Envelope dimensions of the Display Module package are shown in Figure 6.

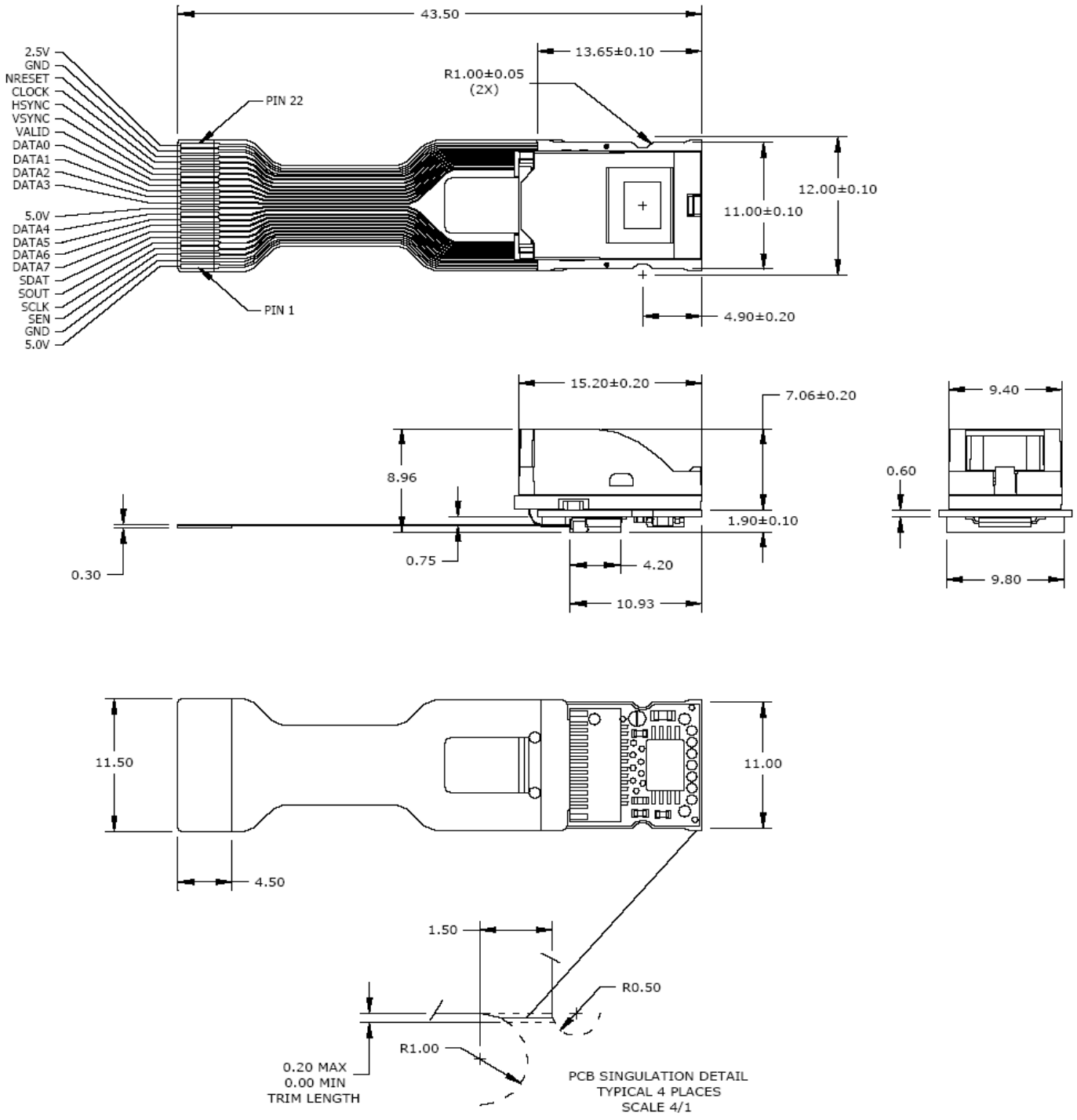

Figure 6: Envelope Dimensions

(**All dimensions in millimeters**)

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Mounting Recommendations

The LV201k Display Module is designed to mount into camera viewfinder systems with minimal effort. Location of the lens elements for optical viewing of the Display Module should be referenced to the top surface of the PCB assembly for minimal tolerance stack relative to the object plane. Electrical connection is made by means of an attached flex circuit. Mounting and electrical connection of the LV201k Display Module is designed for easy assembly reducing manufacturing time and complexity. Refer to Figure 7 for detail of mounting dimensions for the LV201k Display Module.

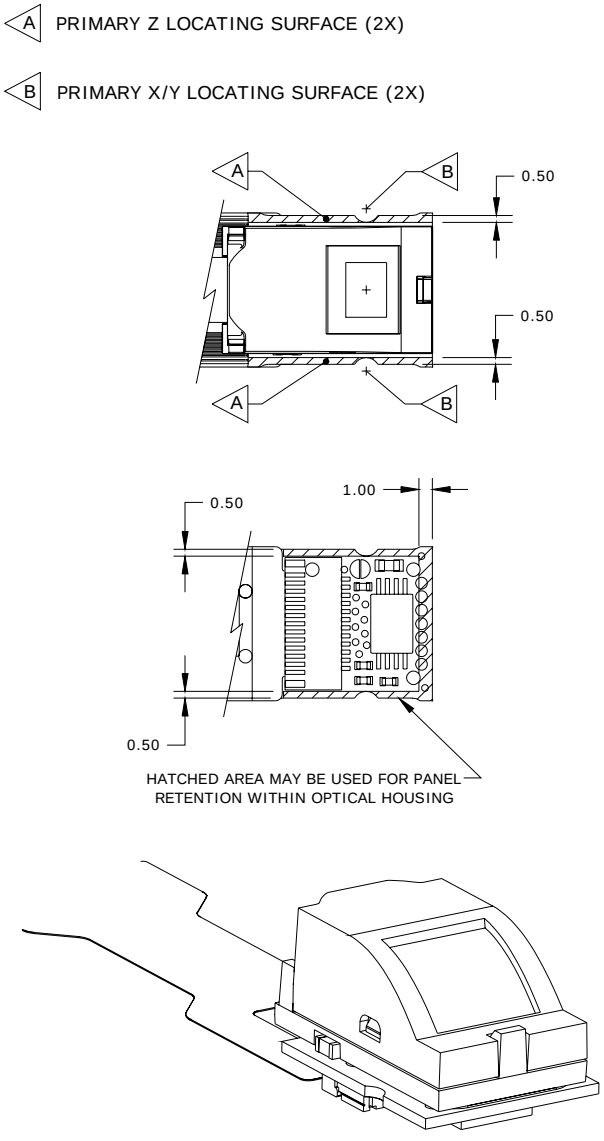

Figure 7: Mounting Dimensions

(All dimensions in millimeters)

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Connector Recommendation

The type of connector chosen by the system designer is highly dependent on the application. The LV201k Display Module provides 22 signals via pins at the end of the flex cable. The pins are spaced on a 0.5 mm pitch. See Table 4 for a detailed listing of signal assignments for each pin.

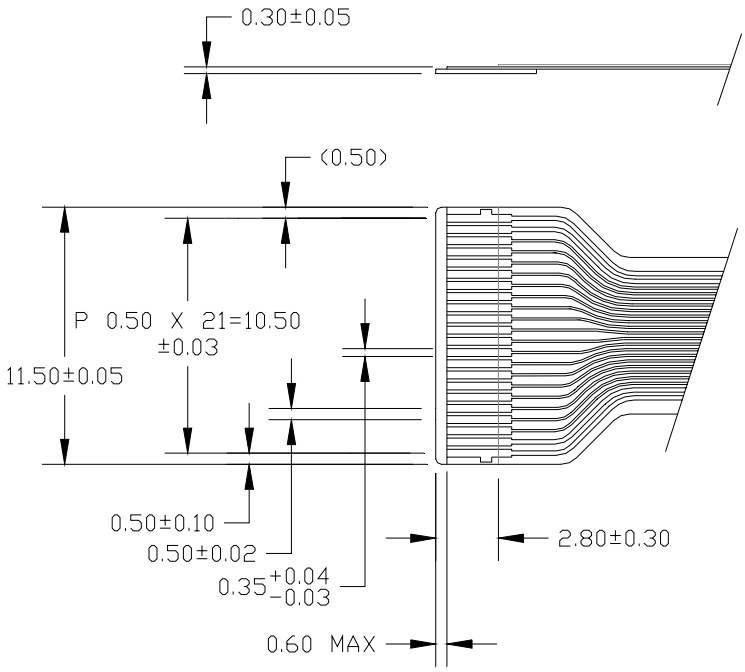

Figure 8: Connector Tab Details

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Electrical Specification

The Display Module accepts standard video formats requiring no additional interface hardware, providing the camera system designer a plug and play electronic viewfinder solution. The backplane is based on standard CMOS electronics for proven functionality and reliability.

Electrical Interface Specification

The LDM-0201-E3A Digital Display Module converts digital video signals to displayed images. Acceptable video input formats are CCIR-601, CCIR-656, and 8-bit RGB Serial.

Video input data is gamma corrected and stored in a frame buffer and video data from the frame buffer is used to create a sequence of red, green, and blue video fields. These color fields will be displayed at a rate of 6 times the video input's vertical frequency. Only 60Hz and 50Hz vertical input frequencies are supported. The default gamma correction value can be found in the Configuration Register section. A gamma correction is applied on the output side of the display. The gamma correction table can be programmed to correct for any incoming gamma value between and including 1.0 to 3.0.

The Display Module is controlled by a four wire serial interface. Through this interface, various display attributes can be controlled. Display attributes are set by writing to registers inside the Display Module. The serial interface is designed to be compatible with common three wire serial interfaces. However, an additional fourth wire is provided to allow the register's values to be read. This addition to the three wire serial interface is provided as a convenience. No reading of registers is required for proper operation of the Display Module.

At power-up or following a hardware reset, the LDM-0201-E3A Display Module is in a sleep mode. The host must then program the Display Module through the serial interface to set which video format the host will provide. If desired, other display attributes may also be programmed at this time. Lastly, the host must program the Display Module to enable the display. To power down the display after it has been enabled, the Display Module must be returned to sleep mode by programming the Display Module to disable the display.

The Display Module is reset with the NRESET pin. For general usage, NRESET should be tied to system reset. The LDM-0201-E3A Display Module requires 5V and 2.5V power.

The Display Module's electrical inputs are compatible with either 3.3V or 2.5V CMOS signaling. The Display Module's electrical output is an open-drain output. All pins have ESD protective diodes, and no pull-up or pull-down resistor. One may tie a pull-up resistor, provided by the user, to either 3.3V or 2.5V so as to create an output with the desired voltage range.

The Display Module contains minimal decoupling capacitance. The user is therefore required to provide de-coupling capacitors for the 2.5V and 5V power supplies to limit supply voltage variations due to peak current sinks from the Display Module.

Table 4 shows the pin assignments for the 22 pin connector and Tables 5 and 6 show the voltage and current requirements of the LDM-0201-E3A Display Module.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Pin Num.	Pin Name	Pin Direction	Pin Function		
22	2.5V	Power	Core power supply (VDD)		
21	GND	Ground	Power and signal return		
20	NRESET	Input	System reset		
			CCIR –601	**CCIR-656**	**8-Bit RGB Serial**
19	CLOCK	Input	CLOCK	CLOCK	CLOCK
18	HSYNC	Input	HSYNC	GND	HSYNC
17	VSYNC	Input	VSYNC	GND	VSYNC
16	VALID	Input	VALID*1	GND	VALID*1
15	DATA 0	Input	Y/Cr/Cb 0	Y/Cr/Cb 0	R/G/B 0
14	DATA 1	Input	Y/Cr/Cb 1	Y/Cr/Cb 1	R/G/B 1
13	DATA 2	Input	Y/Cr/Cb 2	Y/Cr/Cb 2	R/G/B 2
12	DATA 3	Input	Y/Cr/Cb 3	Y/Cr/Cb 3	R/G/B 3
11	L5.0V	Power	Illumination power supply (VCC)		
10	DATA 4	Input	Y/Cr/Cb 4	Y/Cr/Cb 4	R/G/B 4
9	DATA 5	Input	Y/Cr/Cb 5	Y/Cr/Cb 5	R/G/B 5
8	DATA 6	Input	Y/Cr/Cb 6	Y/Cr/Cb 6	R/G/B 6
7	DATA 7 (MSB)	Input	Y/Cr/Cb 7	Y/Cr/Cb 7	R/G/B 7
6	SDAT	Input	Serial interface data input		
5	SOUT	Output (Open Drain)	Serial interface data output (not required for operation)		
4	SCLK	Input	Serial interface clock input		
3	SEN	Input	Serial interface chip select		
2	GND	Ground	Power and signal return		
1	A5.0V	Power	Analog power supply (VCC)		

***1** Use of the VALID signal to indicate when data should be sampled is not required. See CCIR 601 Video Format description or RGB Serial Video Format description for details.

Table 4: Pin Descriptions

(Pin 1 location shown in Figure 4)

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Item	Symbol	Measurement Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	For all inputs		2.3			V
Input Low Voltage	V_{IL}	For all inputs				0.5	V
Input Capacitance	I_C	For all inputs, 3.3V Sqr @ 27Mhz			8	16	pF
Input Leakage Current	I_{IL}	$V_I = V_{IL}$		-10			µA
	I_{IH}	$V_I = V_{IH}$				10	µA
Output Low Current Sink	I_{OL}			50			mA
Supply Voltage	VDD			2.3	2.5	2.7	V
Supply Voltage	VCC			4.5	5.0	5.5	V
Average Supply Current	I_{VDD}	2.3V<VDD<2.7V	Normal Mode	15	22	28	mA
			Sleep Mode	0.5	1.44	3.0	mA
Average Supply Current	I_{VCC}	4.5V < VCC < 5.5V	Normal Mode	2	7	12	mA
			Sleep Mode	0.13	0.26	0.9	mA

Table 5: DC Characteristics

Item	Min	Max	Unit
VDD to GND		3	V
VCC to GND		6	V
Voltage on any Input Pin to GND	GND-0.4	VDD+1.4	V

Table 6: Absolute Maximum Ratings

Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each input pin, except for Vdd, Vcc and GND (Vss) inputs. The equivalent circuit of the input pins is shown below (Resistance values shown typical):

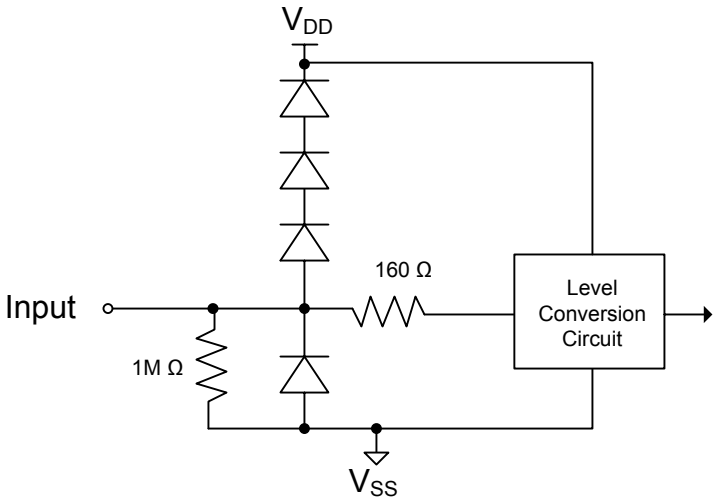

Figure 9: Input Equivalent Circuit

Video Input Interface

Supported Video Formats

The LDM-0201-E3A supports three video formats: CCIR-601, CCIR-656, and 8-bit RGB Serial.

For CCIR-601 and RGB Serial video sources, separate HSync and VSync signals must be provided. The sampling of video data can be configured to use either the VALID signal to indicate valid image data, or a configurable delay after the assertion of HSync or VSync including adjustment of delay between odd and even fields. The odd and even video fields must be correctly indicated by the relation of the VSsync and HSync pulses per the CCIR-601 specification.

For the CCIR-656 video sources, the odd and even field must be correctly indicated by the 'F' bit of the SAV and EAV codes per the CCIR-656 specification.

Video input sources can be at either 50Hz or 60Hz vertical frequency and can be displayed with or without overscan.

Video Scaling and Cropping

Video data for the CCIR video formats must be either 720 by 242, 720 by 240, or 720 by 288 resolution. Since the LDM-0201-E3A has a native resolution of 300 by 224, the LDM-0201-E3A will scale the video data prior to its display. Video data for the RGB Serial input format is expected to be in the LDM-0201-E3A native resolution of 300 by 224. The LDM-0201-E3A uses horizontal and vertical interpolation to fit the input video data on to the LDM-0201-E3A's 300 by 224 pixel array. This interpolation function is configured by programming the Scaling Coefficient Upper Register, the Horizontal Scaling Coefficient Register, the Horizontal Scaling Cycle Register, the Vertical Scaling Coefficient Register, and the Vertical Scaling Cycle Register, before the display is enabled. Cropping to produce overscan is achieved by delaying the sampling of video data in both the horizontal and vertical directions. The HVldDelay and VVldDelay fields of the Vertical Field Offset Register, the Horizontal Valid Delay Register and the Vertical Valid Delay Register control the cropping function. Table 7 details the supported settings.

Input Resolution		**Overscan**	**Valid Delay** *1		**Post-Crop Resolution**		**Interpolation Register Settings**			
H	**V**		**H**	**V**	**H**	**V**	**H Coef.**	**H Cycle**	**V Coef.**	**V Cycle**
720	240	None	0	0	720	240	214	5	478	14
720	240	7.0%	48	8	672	224	229	25	512	1
720	242	None	0	1	720	240	214	5	478	14
720	242	7.0%	48	9	672	224	229	25	512	1
720	288	None	0	0	720	288	214	5	399	7
720	288	8.3%	60	12	660	264	233	5	435	28
300	224	None	0	0	300	224	512	1	512	1

***1** Valid Delay settings must be adjusted when not using the VALID signal to indicate when data should be sampled. See CCIR 601 Video Format description for details.

Table 7: Scaling and Cropping Options for Supported Video Formats

CCIR-601 Video Format

The LDM-0201-E3A can accept video in the CCIR-601 video format. The LDM-0201-E3A will accept 240/242 or 288 lines per field for the NTSC and PAL video input modes respectively. Data is expected to be in the standard 4:2:2 format with 720 valid Y samples, 360 valid Cr samples, and 360 valid Cb samples, per line.

Figure 10 shows the required vertical timing of the video input signals for CCIR-601. Figure 11 shows the required horizontal timing signals. Tables 8 and 9 provide the required timing specifications for the 240/242-line and 288-line modes respectively.

Note that with regards to the timing specifications given in Tables 8 and 9, all specifications must be met simultaneously. For example it would not be satisfactory to have the maximum vertical back porch, front porch, and pulse width as 7 + 7 + 20 = 34 lines which violate the maximum vertical blanking specification of 26 lines.

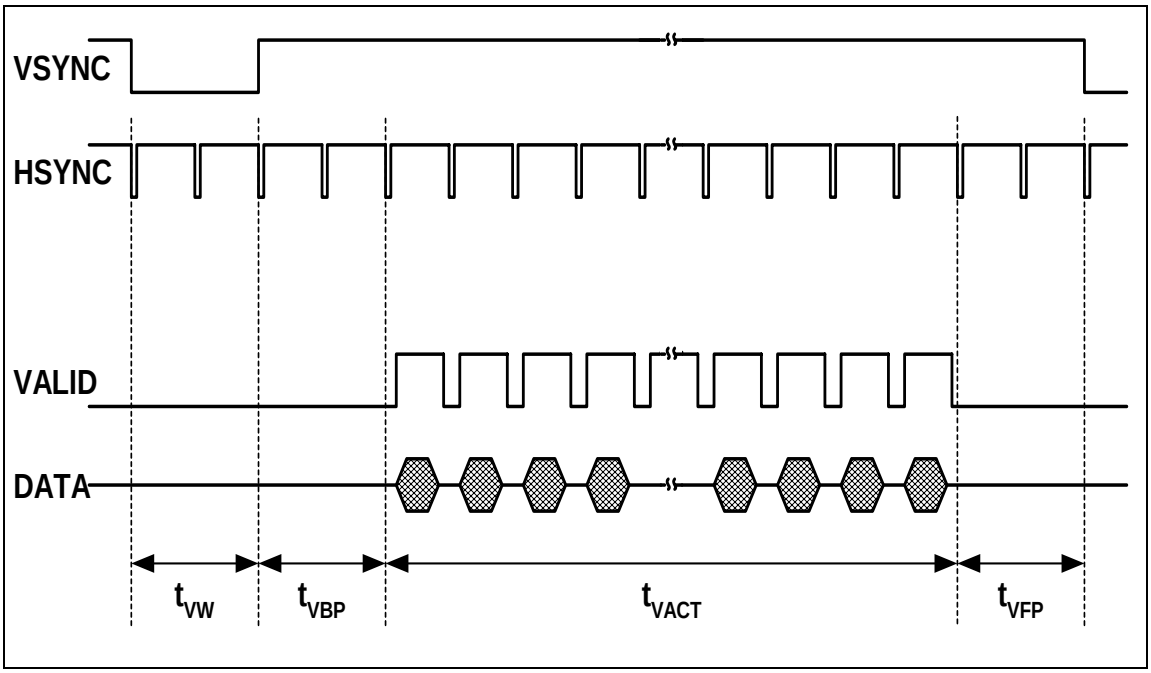

Figure 10: Video Input Vertical Timing, CCIR-601 Video Formats

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

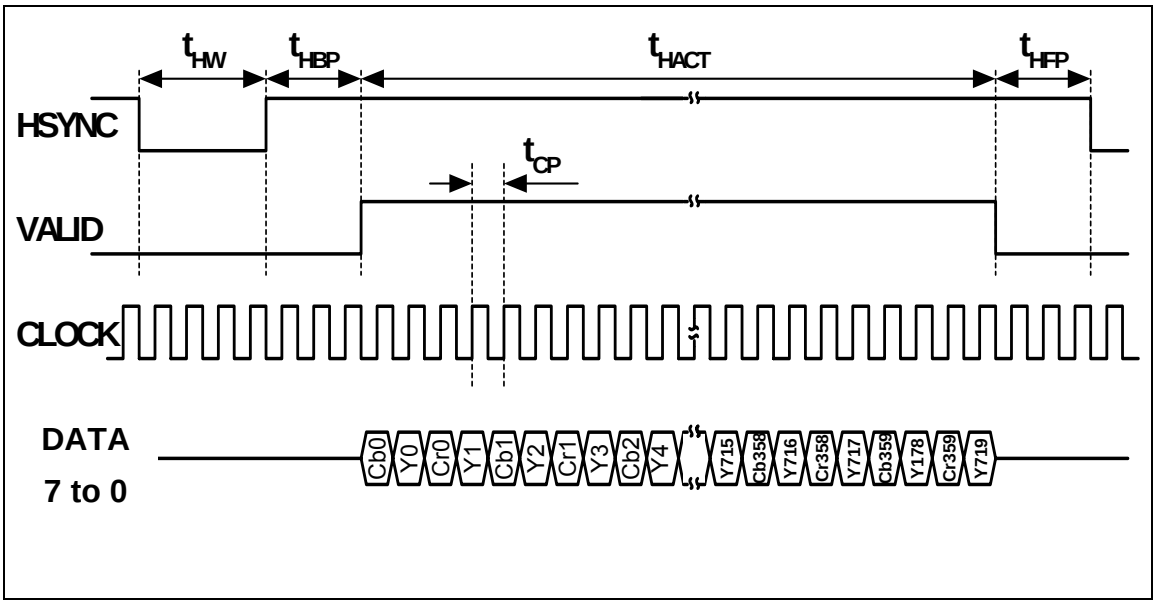

Figure 11: Video Input Horizontal Timing, CCIR-601 Video Format

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	59	60	61	Hz
VSYNC, total lines	$t_{VTOT=}$ t_{VBLK+} t_{VACT}	260	262	266	Lines
VSYNC, active lines	t_{VACT}	240	242	242	Lines
VSYNC, blanking	$t_{VBLK=}$ t_{VFP+} t_{VW+} t_{VBP}	18	22	26	Lines
VSYNC, front porch	t_{VFP}	3	3	7	Lines
VSYNC, pulse width	t_{VW}	3	3	7	Lines
VSYNC, back porch	t_{VBP}	12	16	20	Lines
HSYNC, total clocks	t_{HTOT}	1690	1716	1746	Clocks
HSYNC, active clocks	t_{HACT}	1440	1440	1440	Clocks
HSYNC, blanking	t_{HBLK}	250	276	306	Clocks
HSYNC, front porch	t_{HFP}	15	32	62	Clocks
HSYNC, pulse width	t_{HW}	100	126	156	Clocks
HSYNC, back porch	t_{HBP}	92	118	148	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	¼ t_{HTOT}	½ t_{HTOT}	¾ t_{HTOT}	Clocks

Table 8: AC Characteristics, CCIR-601 240/242-line, 60Hz Video Format Timing

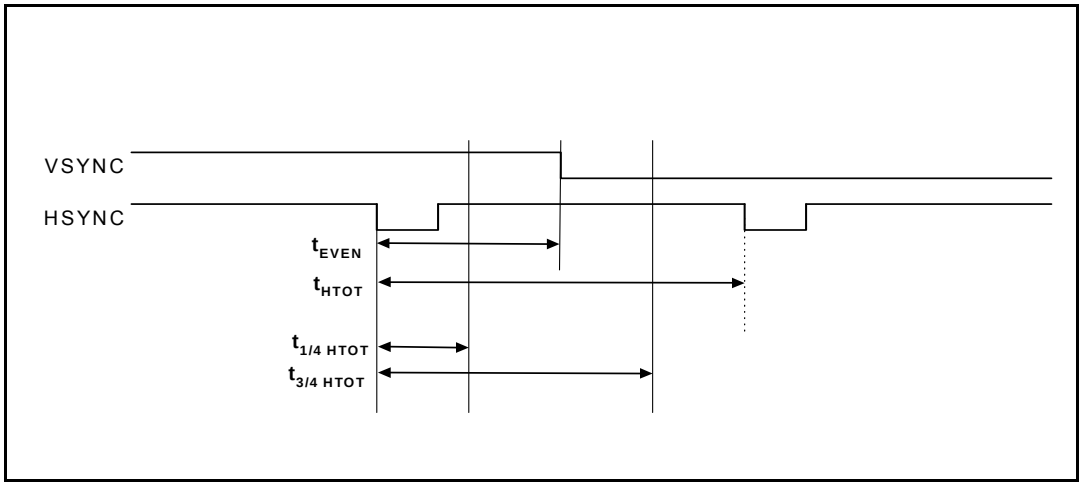

Figure 12: Video Input Field Detection

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	49	50	51	Hz
VSYNC, total lines	t_{VTOT}	306	312	318	Lines
VSYNC, active lines	t_{VACT}	288	288	288	Lines
VSYNC, blanking	t_{VBLK}= t_{VFP+} t_{VW+} t_{VBP}	18	24	30	Lines
VSYNC, front porch	t_{VFP}	3	3	9	Lines
VSYNC, pulse width	t_{VW}	3	3	9	Lines
VSYNC, back porch	t_{VBP}	12	18	24	Lines
HSYNC, total clocks	t_{HTOT}= t_{HBLK+} t_{HACT}	1698	1728	1766	Clocks
HSYNC, active clocks	t_{HACT}	1440	1440	1440	Clocks
HSYNC, blanking	t_{HBLK}= t_{HFP+} t_{HW+} t_{HBP}	258	288	326	Clocks
HSYNC, front porch	t_{HFP}	15	24	62	Clocks
HSYNC, pulse width	t_{HW}	96	126	164	Clocks
HSYNC, back porch	t_{HBP}	108	138	176	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	¼ t_{HTOT}	½ t_{HTOT}	¾ t_{HTOT}	Clocks

Table 9: AC Characteristics, CCIR-601 288-line, 50Hz Video Format Timing

CCIR 601 Without VALID

The LDM-0201-E3A is configured by default to require an external VALID to indicate when video data should be sampled. Alternatively, when the SyncMode bits of the Video Configuration Register0 are programmed to “01”, the LDM-0201-E3A will ignore the VALID input pin and begin sampling video data after a specified delay from the assertion of HSYNC and VSYNC. The Vertical Field Offset Register, the Horizontal Valid Delay Register, and the Vertical Valid Delay Register are used to specify these delays. The values to program these register fields are as follows:

Register Field	Calculation	Unit
HVldDelay	$t_{HW +} t_{HBP}$ + (horizontal overscan delay) - 2	Clocks
VVldDelay	$t_{VW +} t_{VBP}$+ (vertical overscan delay)	Lines
VldDelOffset	$(t_{VW +} t_{VBP})_{\text{even field}} - (t_{VW +} t_{VBP})_{\text{odd field}}$	Lines

Table 10: Register Values Enabling CCIR 601 Without Valid

CCIR-656 Video Format

The LDM-0201-E3A can accept video in the CCIR-656 video format. The LDM-0201-E3A will accept either 240/242 or 288 lines per field for the NTSC and PAL video input modes respectively. Data is expected to be in the standard 4:2:2 format with 720 Y samples, 360 Cr samples, and 360 Cb samples per line. Use of the SAV and EAV codes according to the CCIR-656 specification is required.

The CCIR-656 interface of the LDM-0201-E3A complies with the ITU-R BT.656-4 version of the specification. The LDM-0201-E3A expects that when the V bit of the SAV code transitions from a 1 to a 0, that the following line will be valid and is to be sampled. CCIR-656 video interfaces complying to older versions of the CCIR-656 specification may not cause the V bit of the SAV code to transition concurrently with the data being valid, which may result in the unintentional sampling of blanking lines. To address these older interfaces, the VldDelOffset field of the Vertical Field Offset Register and the Vertical Valid Delay Register may be programmed to skip an additional number of blanking lines after the transition of the V bit. Sampling of data will begin the programmed number of lines after the transition of the V bit. The number of blanking lines to skip can be independently programmed for the two video fields. To disable line skipping, the number of lines to skip must be programmed to zero.

Figure 13 shows the required horizontal timing of the video input signals for CCIR-656. Tables 11 and 12 provide the required timing for 240/242-line and 288-line modes, respectively. Table 13 specifies the arrangement of the bits in the SAV and EAV codes.

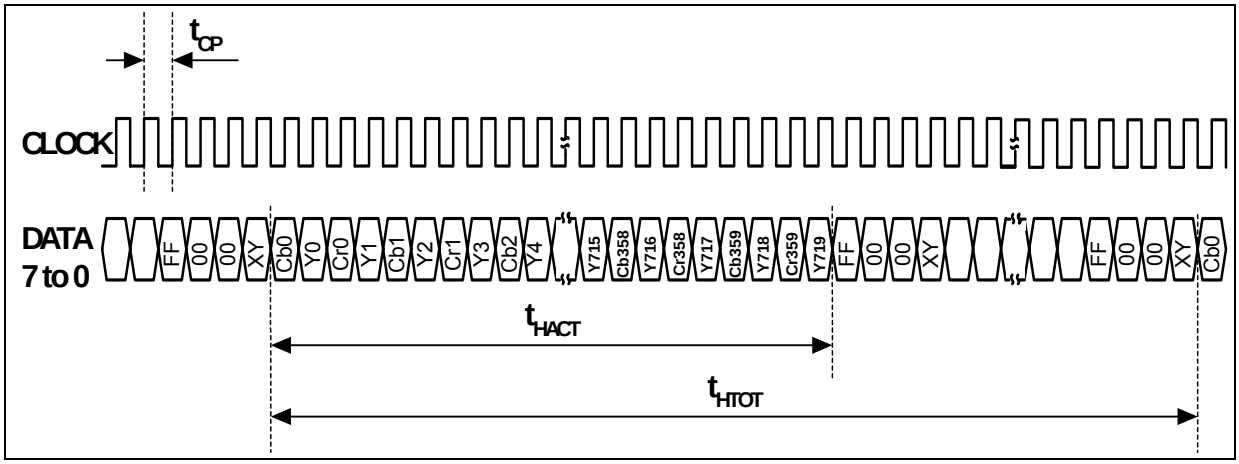

Figure 13: Video Input Timing, CCIR-656 Video Format

Item	Symbol	Min	Typ	Max	Unit
Vertical frequency	t_{VF}	59	60	61	Hz
Total lines per field	t_{VTOT}	258	262	266	Lines
Active lines per field	t_{VACT}	240	242	242	Lines
Total clocks per line	t_{HTOT}	1690	1716	1746	Clocks
Active clocks per line	t_{HACT}	1440	1440	1440	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz

Table 11: AC Characteristics, CCIR-656 240/242-line, 60Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
Vertical frequency	t_{VF}	49	50	51	Hz
Total lines per field	t_{VTOT}	306	312	318	Lines
Active lines per field	t_{VACT}	288	288	288	Lines
Total clocks per line	t_{HTOT}	1698	1728	1766	Clocks
Active clocks per line	t_{HACT}	1440	1440	1440	Clocks
CLOCK, rate	$1/t_C$	26.5	27	27.5	MHz

Table 12: AC Characteristics, CCIR-656 288-line, 50Hz Video Format Timing

CCIR-656 Data Information	Pin Name	First Word	Second Word	Third Word	Fourth Word
Data 7 (MSB)	Data 7 (MSB)	1	0	0	1
Data 6	Data 6	1	0	0	F
Data 5	Data 5	1	0	0	V
Data 4	Data 4	1	0	0	H
Data 3	Data 3	1	0	0	P3
Data 2	Data 2	1	0	0	P2
Data 1	Data 1	1	0	0	P1
Data 0 (LSB)	Data 0	1	0	0	P0

Table 13: Bit Arrangement for CCIR-656 SAV and EAV Codes

Note 1: Bit codes F, V, and H are defined as
F = 0 during field 1 and 1 during field 2
V = 1 during field blanking and 0 elsewhere
H = 0 in SAV and 1 in EAV

Note 2: Protection bits P3-P0 are ignored by the LDM-0201-E3A.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

RGB Serial Video Format

The LDM-0201-E3A can accept video in a 8-bit RGB serial format. When the DataMode field of the VideoConfiguration0 register is programmed to "000", the LDM-0201-E3A will expect RGB serial data in the following sequence: Red, Green, then Blue.

The LDM-0201-E3A will accept 300 valid samples per line and 224 valid lines per field when using the values from Table 7. Additional resolutions may be possible with appropriate values for the HScaleStep, HScaleCycle, VScaleStep, and VScaleCycle registers.

Figure 14 shows the required vertical timing of the video input signals and Figure 15 shows the required horizontal timing signals for the 8-bit RGB Serial format. Tables 14 and 15 provide the required timing for the 8-bit RGB Serial format for 60 Hz and 50 Hz video formats, respectively.

Note: With regards to the timing specifications given in Tables 14 and 15, all specifications must be met simultaneously. For example it would not be satisfactory to have the maximum vertical back porch, front porch, and pulse width as 128 + 128 + 150 = 406 lines which violate the maximum vertical blanking specification of 144 lines.

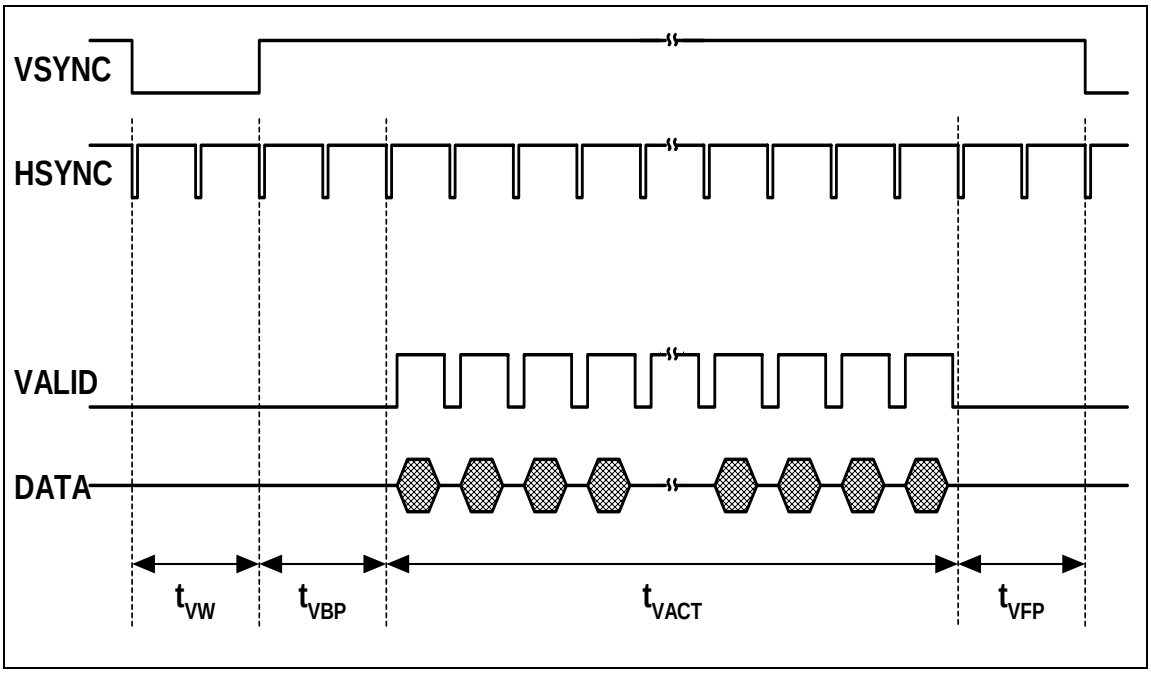

Figure 14: Video Input Vertical Timing, RGB Serial Format

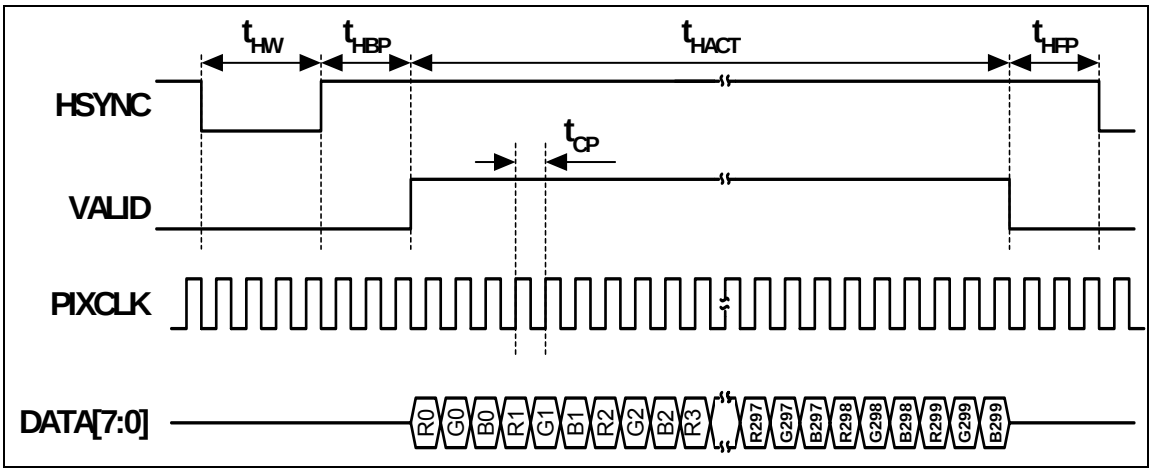

Figure 15: Video Input Horizontal Timing, RGB Serial Video Format

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	59	60	61	Hz
VSYNC, total lines	$t_{VTOT=}$ t_{VBLK+} t_{VACT}	252	262	384	Lines
VSYNC, active lines	t_{VACT}	224	224	224	Lines
VSYNC, blanking	$t_{VBLK=}$ t_{VFP+} t_{VW+} t_{VBP}	12	22	44	Lines
VSYNC, front porch	t_{VFP}	3	3	25	Lines
VSYNC, pulse width	t_{VW}	3	3	25	Lines
VSYNC, back porch	t_{VBP}	6	16	38	Lines
HSYNC, total clocks	$t_{HTOT=}$ t_{HBLK+} t_{HACT}	1690	1716	1746	Clocks
HSYNC, active clocks	t_{HACT}	900	900	900	Clocks
HSYNC, blanking	$t_{HBLK=}$ t_{HFP+} t_{HW+} t_{HBP}	32	816	846	Clocks
HSYNC, front porch	t_{HFP}	14	572	602	Clocks
HSYNC, pulse width	t_{HW}	4	126	156	Clocks
HSYNC, back porch	t_{HBP}	14	118	688	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	¼ t_{HTOT}	½ t_{HTOT}	¾ t_{HTOT}	Clocks

Table 14: AC Characteristics, RGB Serial 60Hz Video Format Timing

Item	Symbol	Min	Typ	Max	Unit
VSYNC, frequency	t_{VF}	49	50	51	Hz
VSYNC, total lines	$t_{VTOT=}$ t_{VBLK+} t_{VACT}	288	312	384	Lines
VSYNC, active lines	t_{VACT}	224	224	224	Lines
VSYNC, blanking	$t_{VBLK=}$ t_{VFP+} t_{VW+} t_{VBP}	48	88	94	Lines
VSYNC, front porch	t_{VFP}	3	19	73	Lines
VSYNC, pulse width	t_{VW}	3	3	73	Lines
VSYNC, back porch	t_{VBP}	6	66	88	Lines
HSYNC, total clocks	$t_{HTOT=}$ t_{HBLK+} t_{HACT}	1698	1728	1766	Clocks
HSYNC, active clocks	t_{HACT}	900	900	900	Clocks
HSYNC, blanking	$t_{HBLK=}$ t_{HFP+} t_{HW+} t_{HBP}	32	828	858	Clocks
HSYNC, front porch	t_{HFP}	14	564	602	Clocks
HSYNC, pulse width	t_{HW}	4	126	164	Clocks
HSYNC, back porch	t_{HBP}	14	138	716	Clocks
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
Even Field Detection, HYSYC edge to VSYNC edge	t_{EVEN}	¼ t_{HTOT}	½ t_{HTOT}	¾ t_{HTOT}	Clocks

Table 15: AC Characteristics, RGB Serial 50Hz Video Format Timing

RGB Serial Without VALID

The LDM-0201-E3A is configured by default to require an external VALID to indicate when video data should be sampled. Alternatively, when the SyncMode bits of the Video Configuration Register 0 are programmed to “01”, the LDM-0201-E3A will ignore the VALID input pin and begin sampling video data after a specified delay from the assertion of HSYNC and VSYNC. The Horizontal Valid Delay Register, and the Vertical Valid Delay Register are used to specify these delays. The values to program these register fields are as follows:

Register Field	Calculation	Unit
HVldDelay	$t_{HW +}$ t_{HBP} - 2	Clocks
VVldDelay	$t_{VW +}$ t_{VBP}+	Lines

Table 16: Register Values Enabling RGB Serial Without Valid

Video Input Signal Timing Requirements

All video input signals must meet the timing requirements shown in Figure 16 and Table 17.

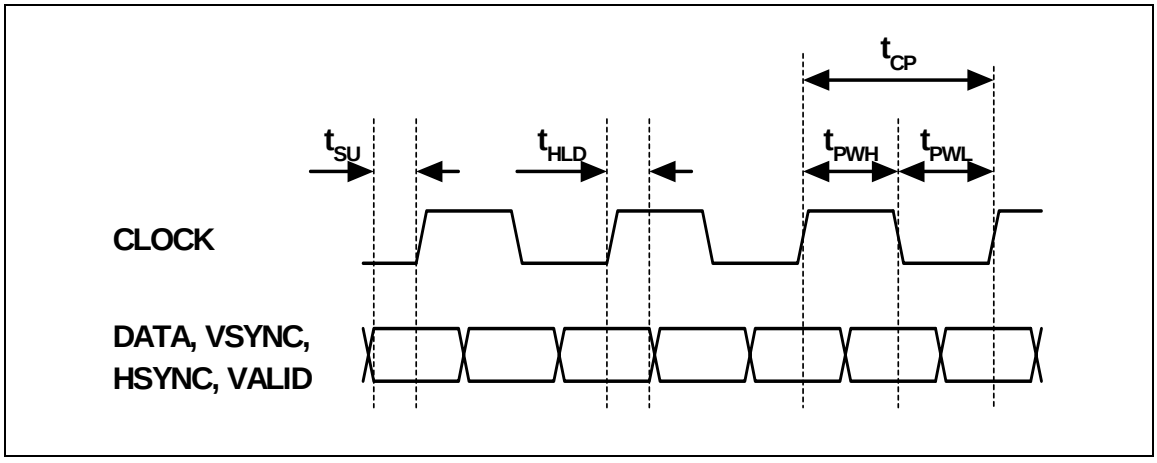

Figure 16: Video Input Signal Timing

Item	Symbol	Min	Typ	Max	Unit
CLOCK, rate	$1/t_{CP}$	26.5	27	27.5	MHz
CLOCK, pulse width high	t_{PWH}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
CLOCK, pulse width low	t_{PWL}	45% t_{CP}	50% t_{CP}	55% t_{CP}	NA
DATA, VSYNC, HSYNC, VALID, setup time	t_{SU}	5			Ns
DATA, VSYNC, HSYNC, VALID, hold time	t_{HLD}	1			Ns

Table 17: AC Characteristics, Video Input Signal Timing

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Serial Interface

The serial interface uses the signals SDAT, SCK, SEN, and SOUT. Through this interface, the LDM-0201-E3A's registers can be both written and read. If desired, the SOUT signal can be ignored and the serial interface can be treated as a common three wire interface. CLOCK must be present, and after a hardware reset a delay of t_{SDLY} must be observed before accessing the serial interface of the LDM-0201-E3A. Although not required, Displaytech recommends using the serial data output to verify the proper programming of the LDM-0201-E3A registers.

The serial interface is activated by pulling the SEN input low. Then the SDAT input is sampled on each rising edge of the SCK input. A transfer is begun with the transfer of a read/write command bit and a 7-bit address. For a write command, this is followed by an 8-bit data word to store to that register address. For a read command, the LDM-0201-E3A will output the addressed register's data to the SOUT output. The data is changed on the falling edge of the SCK input and can be sampled on each rising edge of the SCK input.

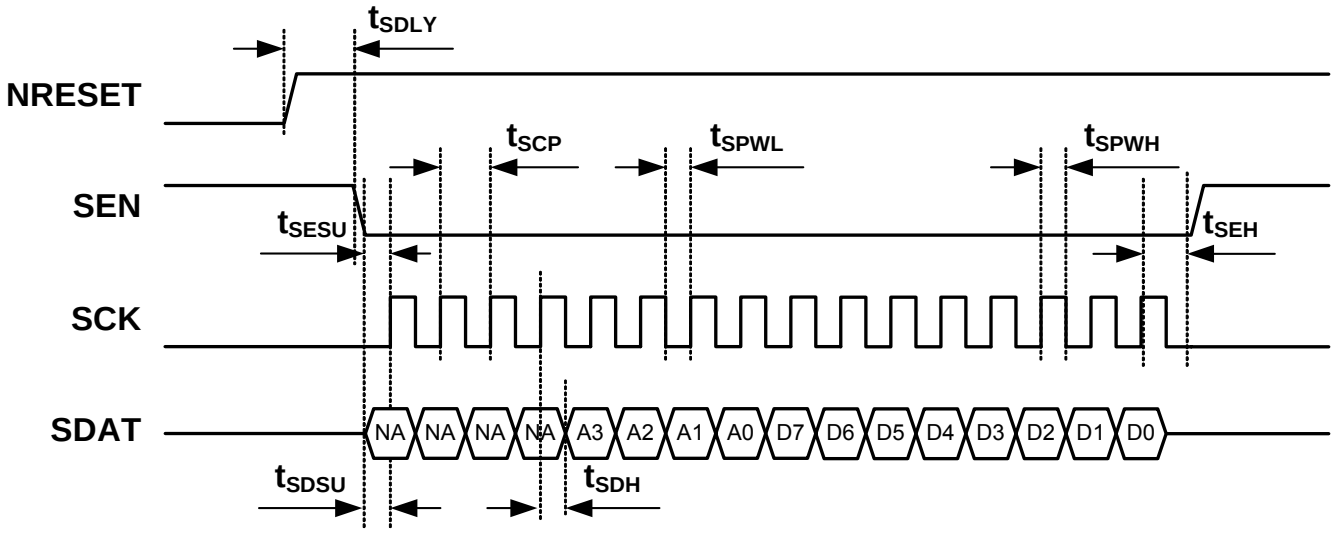

Figure 17: Serial Interface Signal Timing

Item	Symbol	Min	Typ	Max	Unit
Delay from reset to serial transfer	t_{SDLY}	8	-	-	Ms
SCK, rate	$1/t_{SCP}$	100	400	1500	KHz
SCK, pulse width high	t_{SPWH}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
SCK, pulse width low	t_{SPWL}	45% t_{SCP}	50% t_{SCP}	55% t_{SCP}	
SDAT, setup time	t_{SDSU}	150	-	-	Ns
SDAT, hold time	t_{SDH}	150	-	-	Ns
SDO, clock to out time	t_{SCO}	-	-	250	Ns
SEN, setup time	t_{SESU}	150	-	-	Ns
SEN, hold time	t_{SEH}	150	-	-	Ns

Table 18: AC Characteristics, Serial Interface Signal Timing

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

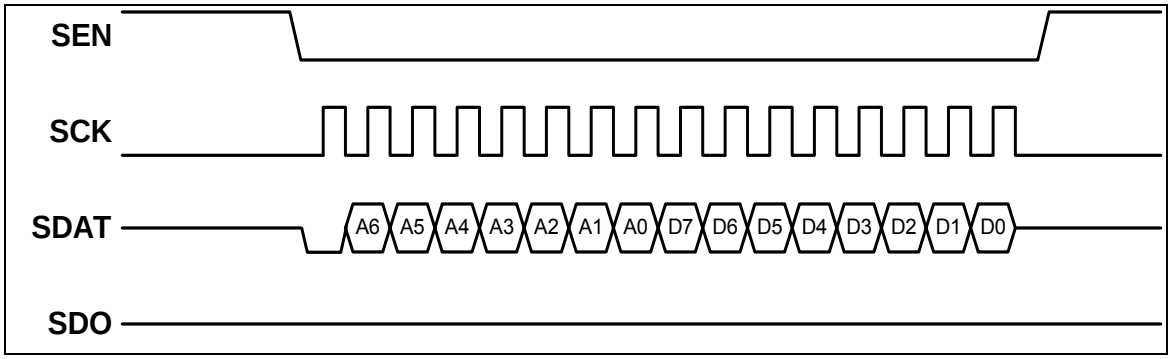

Figure 18: Serial Interface Write Example

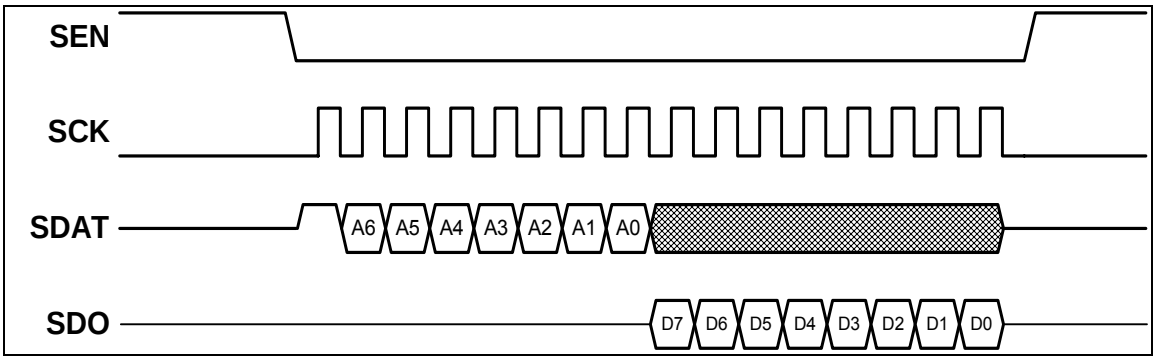

Figure 19: Serial Interface Read Example

Control Sequence Requirements

The LDM-0201-E3A requires particular power-up and shutdown sequences which dictate the application and removal of control signals relative to the power supplies.

As specified in Table 5, no input may exceed the VDD supply by more than 1.4V. It is therefore necessary to apply the VDD supply before any control signal and remove the control signals prior to the removal of the VDD supply. This requirement is due to the ESD protection diodes present on the input pins.

The LDM-0201-E3A will load default register values from EEPROM after the VDD supply is present, the NRESET control signal has been set high, and the CLOCK input is toggling. During this process, the serial interface is ignored as indicated by the timing parameter t_{SDLY} given in Table 18.

The LDM-0201-E3A is enabled by using the serial interface to set the NSleepMode bit of the Video Configuration Register 3. When the NSleepMode bit is cleared the LDM-0201-E3A enters the sleep mode. The LDM-0201-E3A can be repeatedly enabled and disabled as desired. In the sleep mode, all programmed register values are maintained and the Display Module is ready for immediate use

Once the LDM-0201-E3A has been enabled, the LDM-0201-E3A must be disabled using the serial interface, for a time period t_{PWRD} prior to the removal of any power supply, during which time CLOCK and NRESET inputs must be present. The required control sequence of the LDM-0201-E3A is shown in Figure 20. Timing requirements are given in Table 18 and 19.

If it is desired to further reduce sleep mode power, the CLOCK input can be stopped after a time period T_{PWRD} after the LDM-0201-E3A has been disabled. As soon the CLOCK input is restored, the LDM-0201-E3A is ready to begin a serial transfer to be enabled.

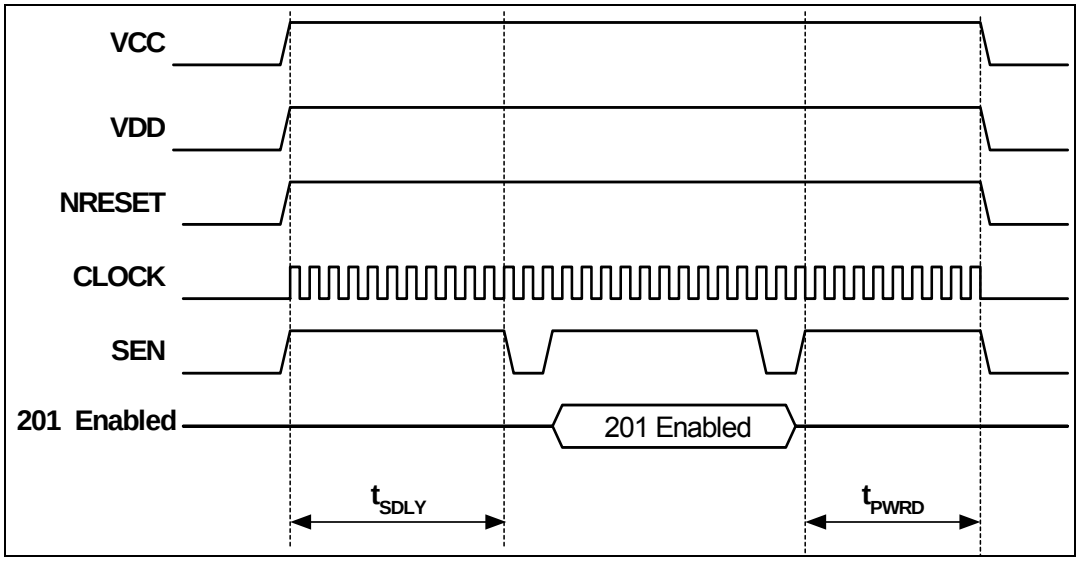

Figure 20: LDM-0201-E3A Control Sequence

Item	Symbol	Min	Typ	Max	Unit
Time from disable of LDM-0201-E3A to removal of first power supply (VCC)	t_{PWRD}	1500	-	-	µs

Table 19: AC Characteristics, Control Sequence Timing

Power Supply Requirements

The LDM-0201-E3A has up to 4µF of bulk capacitance connected to the VDD supply. Inrush current during the application of the VDD supply is determined by the impedance of the source supply.

The LDM-0201-E3A will exhibit large peak current sinks on the VDD power supply relative to the average currents specified in Table 5. To limit these peak currents and ensure that the VDD supply voltage is maintained within specifications, it is required that a minimum of 22µF of bulk capacitance be connected to the VDD power supply and located adjacent to the LV201 connector.

The voltage requirements specified in Table 5 for the VDD and VCC power supplies must be maintained or an internal power-on-reset could result. If an internal reset occurs, power sequencing from the initial start condition, as stated, above is required. If an internal reset occurs after the initial power up sequence any previous data programmed into the LDM-0201-E3A are erased and the display will re-enter sleep mode. After such an occurrence, all configuration registers are set to default values within the display requiring the user to reprogram the display.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Configuration Registers

The LDM-0201-E3A provides a number of registers to allow user customization of the product via the serial interface. For example, the customer can customize the LV201 video-scaler to match a specific input resolution. In order to facilitate factory calibration of the LV201, the same serial interface is also used to program calibration settings to the LV201 EEPROM using a special factory calibration mode. For example, each LV201 LED is individually calibrated to achieve a white point specification. Additionally, during product development, in order to allow easy IC test and characterization, the serial interface is used to actuate a number of test controls in a special test mode. For example, the LV201 can be instructed to perform Built-in-Self-Test (BIST) of the frame buffer memory.

All customer accessible configuration registers, which allow for user configuration of the display parameters, are contained in the upper registers, described in detail below. Figure 21 below gives an overview of the complete register functional block flow.

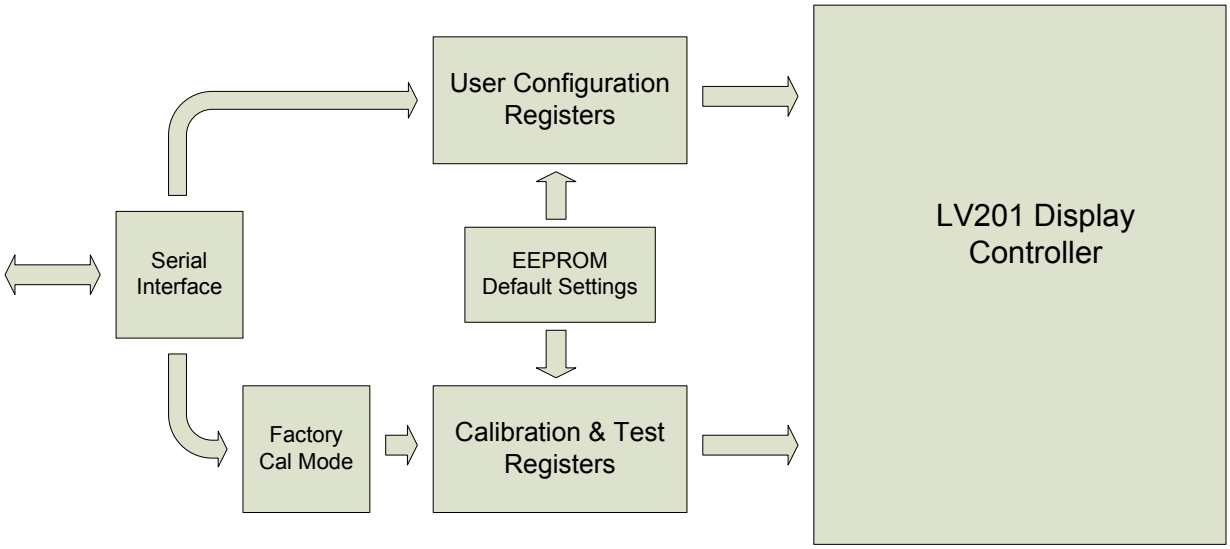

Figure 21: Configuration Register Structure

Factory Calibration and Test Configuration Registers

The following functional configuration areas exist in the factory calibration and test mode.

- Color Space Configuration – a group of registers exists to allow for customer adjustment of color temperature and color gamut.
- LED/Brightness/Contrast Configuration – the calibrated luminance, brightness and contrast of the display is set by configuration of a group of registers that control the LED drive set points. Each display module is individually adjusted in the factory, to characterize the LED performance with the desired specification for brightness and contrast.
- Temperature/Arctic Mode Configuration – each display is set to respond to temperature changes and calibrate the set point for arctic mode enable.
- Built-In-Self-Test (BIST) Configuration – a group of registers exist for test which are used during development as a means of validating performance and configuration verification.

User Configuration Registers

The configuration registers are set at power-up by the configuration EEPROM, subsequently they can be written with the three-wire serial interface to control the LDM-0201-E3A as desired. Register Indexes are given in MSB to LSB order as shown in Figure 12 (i.e. A3,A2,A1,A0). For example registers address 5h would be accessed by sending the serial address such that A3= 0, A2= 1, A1= 0, A0= 1. Similarly, values for the data registers are given in MSB to LSB. Reserved Bits must be written as specified, for proper operation.

Display Configuration Register, with default settings.

Register Index: 00h.

7	6	5	4	3	2	1	0
RES							
01h							

Reserved Bits (RES): This register must be set to 01h for proper operation of the Serial Interface.

Video Configuration Register 0, with Default Settings

Register Index: 01h.

7	6	5	4	3	2	1	0
RES	SyncMode		DitherMode		DataMode		
0	00		10		101		

SyncMode: 00=Use Inputs for video timing
01=Use HSync and VSync inputs, Valid timing specified from Valid delay registers
10= Reserved
11= Use 656 SAV/EAV control codes

DitherMode: 00=No Dither, Input data rounded to 6-bit values
01=½ bit spatial, ¼ bit temporal
10=½ bit temporal, ¼ bit spatial
11=½ bit spatial

DataMode: 000 = RGB Serial
101 = CCIR 601/656
All other values are reserved.

Reserved Bits (RES): The reserved bits must be set to 0s for proper operation.

Video Configuration Register 1, with Default Settings

Register Index: 02h.

7	6	5	4	3	2	1	0
VPol	HPol	ValidPol	ArcticModeEn	RES	RES	VideoMask	
1	1	0	0	0	0		

VPol: Vertical Sync Polarity, 0=Active High, 1=Active Low

HPol: Horizontal Sync Polarity, 0=Active High, 1=Active Low

ValidPol: Valid input Polarity, 0=Active High, 1=Active Low

ArcticModeEn Enable Arctic Mode 0=Disable, 1=Enable

VideoMask: Mask LSB Data Bits, If VideoMask[0] is asserted, input data will be considered 7-bit from VideoIn[7:1], if both VideoMask[1] and VideoMask[0] are asserted, input data will be 6-bit.

LED Brightness Register, with default settings.

Register Index: 03h.

7	6	5	4	3	2	1	0
RES	RES	Brightness Ratio[5:0]					
1	1	3Fh					

Brightness Ratio: The settings of these bits determine the duty cycle for driving the illumination LEDs. When the Brightness Ratio is set to 3Fh, the duty cycle is 100% and the maximum brightness results. When the Brightness Ratio is set to 0h, the duty cycle will be $1/64^{th}$, resulting in the minimum brightness.

Reserved Bits: These bits must be set to 11h for proper operation.

Vertical Field Offset Register, with default settings

Register Index: 04h.

7	6	5	4	3	2	1	0
VldDelOffset[3:0]				VertInterpMode		HVldDelay[9:8]	
0h				10		00	

VVldDelOffset: Offset of even field Valid delay. This is a twos-complement value from –8 (8h) to +7 (7h).
VertInterpMode: 00=No Vertical Interpolation
01=Odd lines not interpolated, Even lines interpolated up ½ line.
10=Odd lines interpolated down ¼ line, Even lines interpolated up ¼ line.

HVldDelay[9:8]: The most significant bits of the horizontal valid delay setting

Horizontal Valid Delay Register, with default settings

Register Index: 05h. Register can be read and written.

7	6	5	4	3	2	1	0
HVldDelay[7:0]							
00h							

HVldDelay: Horizontal sampling delay. The meaning of this register is determined by the value programmed for SyncMode in the Video Configuration 0 register.

SyncMode	HVldDelay Meaning
00	Number of clocks to delay sampling of video data after the assertion of VALID
01	Number of clocks minus one to delay sampling of video data after the assertion of HSYNC
11	Number of clocks to delay sampling of video after SAV

Video Configuration Register 3, with Default Settings

Register Index: 06h.

7	6	5	4	3	2	1	0
RES	VFlip	HFlip	RES	NSleepMode	RES		
0	0	0	0	0	000		

VFlip: Flip display vertically, 0=Don't flip, 1=Flip

HFlip: Flip display horizontally, 0=Don't flip, 1=Flip

NSleepMode: Disable display 0=Power Save Mode, 1=Normal Mode

Reserved Bits (RES): The reserved bits must be set to 0s for proper operation.

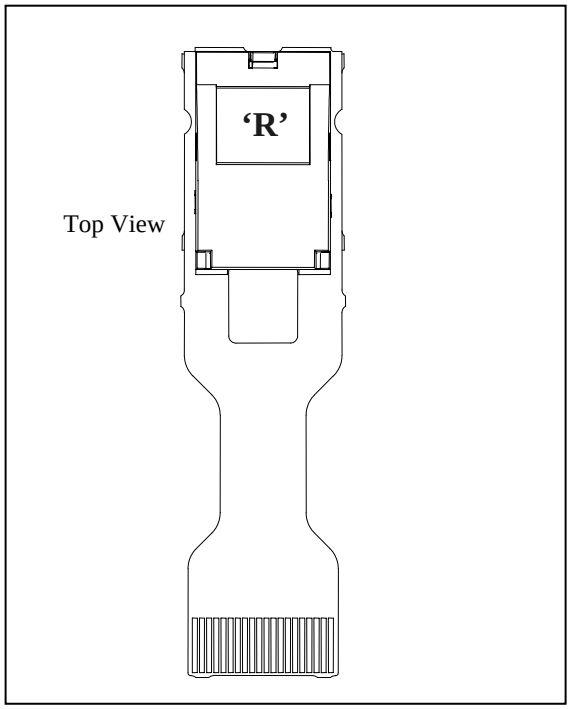

Figure 22: Display Orientation with VFlip=0 and HFlip=0

Scaling Coefficient Upper Register, with default settings

Register Index: 07h.

7	6	5	4	3	2	1	0
RES			HScaleCycle[8]	VScaleStep[9:8]		HScaleStep[9:8]	
000			0	01		00	

HScaleCycle[8]: Most significant bit of the HScaleCycle value.

VScaleStep[9:8]: Most significant two bits of the VScaleStep value

HScaleStep[9:8]: Most significant two bits of the HScaleStep value

Reserved Bits (RES): The reserved bits must be set to 000 for proper operation.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Horizontal Scaling Coefficient Register, with default settings

Register Index: 08h.

7	6	5	4	3	2	1	0
HScaleStep[7:0]							
D6h							

HScaleStep: Horizontal scaling coefficient.

Horizontal Scaling Cycle Register, with default settings

Register Index: 09h.

7	6	5	4	3	2	1	0
HScaleCycle[7:0]							
05h							

HScaleCycle: Horizontal scaling repeat count.

Vertical Scaling Coefficient Register, with default settings

Register Index: 0Ah.

7	6	5	4	3	2	1	0
VScaleStep[7:0]							
DEh							

VScaleStep: Vertical Scaling Coefficient.

Vertical Scaling Cycle Register, with default settings

Register Index: 0Bh.

7	6	5	4	3	2	1	0
VScaleCycle [7:0]							
0Eh							

VScaleCycle: Vertical scaling repeat count.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Vertical Valid Delay Register, with default settings

Register Index: 0Ch.

7	6	5	4	3	2	1	0
VVldDelay[7:0]							
01h							

VVldDelay: Vertical Valid Delay. The meaning of this register is determined by the value programmed for SyncMode in the Video Configuration 0 register.

SyncMode	VertValidDel Meaning
00	Number of VALID lines to delay sampling of video
01	Number of HSYNC periods to delay sampling of video data after the assertion of VSYNC
11	Number of EAV codes to delay sampling of video after clearing the VBlank bit

Cinema Mode Register, with default settings

Register Index: 0Dh.

7	6	5	4	3	2	1	0
RES				CinemaLines			
0h				0h			

CinemaLines: Black Lines added to the top and bottom of the display in Cinema or widescreen mode. The number of lines added will be 2x the CinemaLines register setting at both the top and bottom of the display. For approximately 16:9 aspect ratio, CinemaLines would be set to 0Eh, resulting in 168 active display lines centered vertically in the display. Note: This register is not independent of the vertical and horizontal scaling; the scaling coefficients must be adjusted to fit the display input to the new aspect ratio.

Reserved Bits (RES): The reserved bits must be set to 0h for proper operation.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Gamma Register, with default settings

Register Index: 0Eh.

7	6	5	4	3	2	1	0
RES				GammaValue			
0h				9h			

GammaValue: The gamma value selected from the following table. Note: The display brightness is not independent of Display Gamma, the maximum brightness will be reduced as the gamma of the display is increased.

GammaValue	Display Gamma	GammaValue	Display Gamma
0h	1.0	8h	2.0
1h	1.2	9h	2.1
2h	1.4	Ah	2.2
3h	1.5	Bh	2.3
4h	1.6	Ch	2.4
5h	1.7	Dh	2.6
6h	1.8	Eh	2.8
7h	1.9	Fh	3.0

Table 20: Gamma selection table

Reserved Bits (RES): The reserved bits must be set to 0h for proper operation.

Color Space Gain Registers, with default settings

Register Index: 0F-17h

Index	Default	7	6	5	4	3	2	1	0
0Fh	00h	ColorSpace11 (-128 to +127)							
10h	00h	ColorSpace12 (0 to +255)							
11h	00h	ColorSpace13 (-128 to +127)							
12h	00h	ColorSpace21 (-128 to +127)							
13h	00h	ColorSpace22 (-128 to +127)							
14h	00h	ColorSpace23 (-128 to +127)							
15h	00h	ColorSpace31 (-128 to +127)							
16h	00h	ColorSpace32 (-128 to +127)							
17h	00h	ColorSpace33 (0 to +255)							

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Hardware Configuration Register, with default settings

Register Index: 18h

7	6	5	4	3	2	1	0
Resolution				Revision			
5h				4h			

Resolution: Display Resolution, set to 5h for 300x224

Revision: Display Revision, Rev. D is 4h.

Color Space Offset Registers, with default settings

Register Index: 19-1Bh

Index	Default	7	6	5	4	3	2	1	0
19h	00h	ColorOffset1 (-128 to +127)							
1Ah	00h	ColorOffset2 (0 to +255)							
1Bh	00h	ColorOffset3 (0 to +255)							

The LDM-0201-E3A microdisplay may be set to accept RGB or YCbCr color spaces, and additionally allows for scaling or offset of each color independently to adapt to optional color space scaling or white point adjustment. Please refer to the below formula's when setting Color Space Gain & Offset Registers. Note: contact Displaytech for color space selection if using RGB data mode.

$$\begin{bmatrix} R_O \\ G_O \\ B_O \end{bmatrix} = \frac{1}{128} \begin{bmatrix} 128+cs_{11} & 0+cs_{12} & 175+cs_{13} \\ 128+cs_{21} & -42+cs_{22} & -90+cs_{23} \\ 128+cs_{31} & 222+cs_{32} & 0+cs_{33} \end{bmatrix} \bullet \begin{bmatrix} Y_I+O_1 \\ Cb_I-128+O_2 \\ Cr_I-128+O_3 \end{bmatrix}$$

Figure 23: Color Space Gain & Offset selection figure

Minimum Vertical Frequency Register, with default settings

Register Index: 1Ch

7	6	5	4	3	2	1	0
RES	MinVFreq[6:0]						
0	2Fh						

MinVFreq: The minimum vertical frequency, in Hz, assuming a 27MHz PIXCLK. If the PIXCLK frequency is different, the number should be multiplied by the ratio of 27MHz over the actual PIXCLK frequency.

Maximum Vertical Frequency Register, with default settings

Register Index: 1Dh

7	6	5	4	3	2	1	0
RES	MaxVFreq[7:0]						
0	3Fh						

MaxVFreq: Maximum vertical frequency, in Hz, assuming a 27MHz PIXCLK. If the PIXCLK frequency is different, the number should be multiplied by the ratio of 27MHz over the actual PIXCLK frequency.

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Product Quality

Defect Acceptance Criteria

Test	Criteria		
	Size	Qty	
		Bright	Dark
Line Out	0		
Large	> 3 pixel < 4 pixel	1	1
Medium	> 1 pixel & ≤ 3 pixel	3	3
Small	>¼ pixel & ≤ 1 pixel	No clumping	

Table 21: Visual Inspection Specification

Shipping and Packing

All LV201k Display Modules arrive in a custom molded ESD safe tray with a static protective bag. These trays were sealed prior to leaving the manufacturing facility in a Class 10,000 clean room. To prevent dust and particulate contamination, do not open the seal on these trays outside of a Class 10,000 or equivalent room for incoming inspection or manufacturing integration. Do not stack trays higher than 10, or place other heavy material on the trays to prevent damage to the sensitive optical components on the display.

Applicable Standards

UL Flammability Standards

Model	Type	UL Rating
LV201k	Flex	VTM-0
LV201k	Packaging	V2

Table 22: UL Flammability Standards

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Mechanical Standards

Product	Mechanical Test Type	Stress Units	Duration
LV201k Module	Vibration	Frequency = 20 Hz – 2 KHz Acceleration = 10 g Non-biased	4 cycles per each axis, 3 translations minimum
	Shock	Acceleration = 300 g Shock Pulse = 2 ms	4 cycles per each axis, 3 translations minimum

Table 23: Mechanical Standards

Regulatory Standards

Product	Test Type	Stress Types
LV201k Module	ESD	Type = Human Body Test Voltage = 1000 V
	EMI	FCC Part 15, Subpart B

Table 24: Regulatory Standards

Environmental Standards

Substance	Parts Per Million (PPM)
Cadmium & Cadmium Compounds	Compliant with RoHS requirement[1]
Halogenated Dioxins & Furans Table	None Intentionally Used.
Hexavalent Chromium Compounds	Compliant with RoHS requirement[1]
Lead & Lead Compounds	Compliant with RoHS requirement[1]
Mercury	Compliant with RoHS requirement[1]
PBB	Compliant with RoHS requirement[1]
PBDE	Compliant with RoHS requirement[1]

Table 25: Banned Substances

Note 1: The PPM level adhered to the requirement set out by RoHS and TAC (Technical Adaptation Committee).

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com

Corporate Profile

Displaytech, Inc. makes and sells microdisplays with superior image quality for electronic viewfinders in consumer digital still cameras, camcorders, and mobile communication devices. The low power and compact form factor of Displaytech's LightView™ microdisplay product line enable innovative end-product design. The patented Ferroelectric Liquid Crystal (FLC) technology at the heart of the Company's microdisplays is also used in a line of ultra-fast photonics switching products for emerging optical applications. A fabless manufacturing model positions Displaytech to keep pace with the high-volume consumer electronics market.

For more information visit **www.displaytech.com**

Displaytech, Inc.
2602 Clover Basin Drive
Longmont, Colorado 80503-7604 USA
303-772-2191
www.displaytech.com
LV201support@displaytech.com