Himax Display, Inc.

DATA SHEET

(DOC No. HX7033CTNPA-DS)

HX7033CTNPA

320X240 0.28” LCOS Module

Version 04 May, 2015

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Revision History

May, 2015

Version	Date	Description of changes
01	2014/07/07	New setup.
02	2014/11/26	Page 28 1. Modify CH 10.2.1 ‘Carton label’.
03	2015/03/20	All pages 1. Remove ‘preliminary’ wording. Page 25 2. Modify CH 9.3 ‘The panel reflection spectrum (Typical)’. 3. Modify CH 9.4 ‘The panel Y-V curves (Typical)’
04	2015/05/19	Page 8, 12 1. Modify ‘Operation frequency **(Pixel clock)** typical spec. from 14.4 to 12.0 MHz. Page 12 2. Modify ‘CH 7.1 Input timing (QVGA)’.

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Important Notice

May, 2015

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1. General Description

The HX7033CTNPA is an active matrix liquid crystal display with resolutions of 320 x 240 x 3 dots, which is ideal for portable and industrial applications. Horizontal digital data drivers and vertical scan drivers are integrated with single crystal pixel transistors meet the performance demands of light weight, high speed and high resolution applications.

The HX7033CTNPA receives 6-bit x 3-dot of digital display data per clock simultaneously and generates corresponding voltage output of 256-level gray scales, which embedded with two-wired serial bus that can be used to programming gamma voltage and COM directly.

2. Features

- LCOS color filter panel with resolution 320 x 240 x 3
- Support display mode: QVGA input source
- Support input interface: RGB666
- No spacers in the display area
- Integrated horizontal data and vertical scan drivers
- Horizontal and vertical bi-directional scanning
- Embedded with DE mode timing controller.
- Capable of displaying 256-level gray scales by 12 x 3 **(RGB separately)** internal γ reference voltages
- Embedded with programmable gamma reference voltages
- Embedded with COM modulation
- Embedded with timing controller
- Dual-edge interface with INV function for lower EMI
- Two-wired serial interface for internal register setting
- Operation powers: analog power **(10.0V)** and digital power **(1.8V / 3.3V)**
- Module pin number=35
- Ideal for mini-projector application

3. Quick Reference Data

3.1. Reference data

Parameter	Spec.	Unit
Active area diagonal	0.28”	Inch
Active area dimensions	5.76 x 4.32	mm
Native aspect ratio	4:3	-
Display resolution	320 x 240 x 3	Pixel
Pixel pitch	18x18	μm
Pixel configuration	RGB	-
Gray level	256	-
Typical contrast ratio @ F/2.5	170	-
Typical reflectance **(Luminance, Y)**	20[2]	%
Optical mode	Reflective	-
Liquid crystal type	Twisted Nematic mode	-
Operation mode	Normally white	-
Response time **(T_R+T_F)**	15	ms

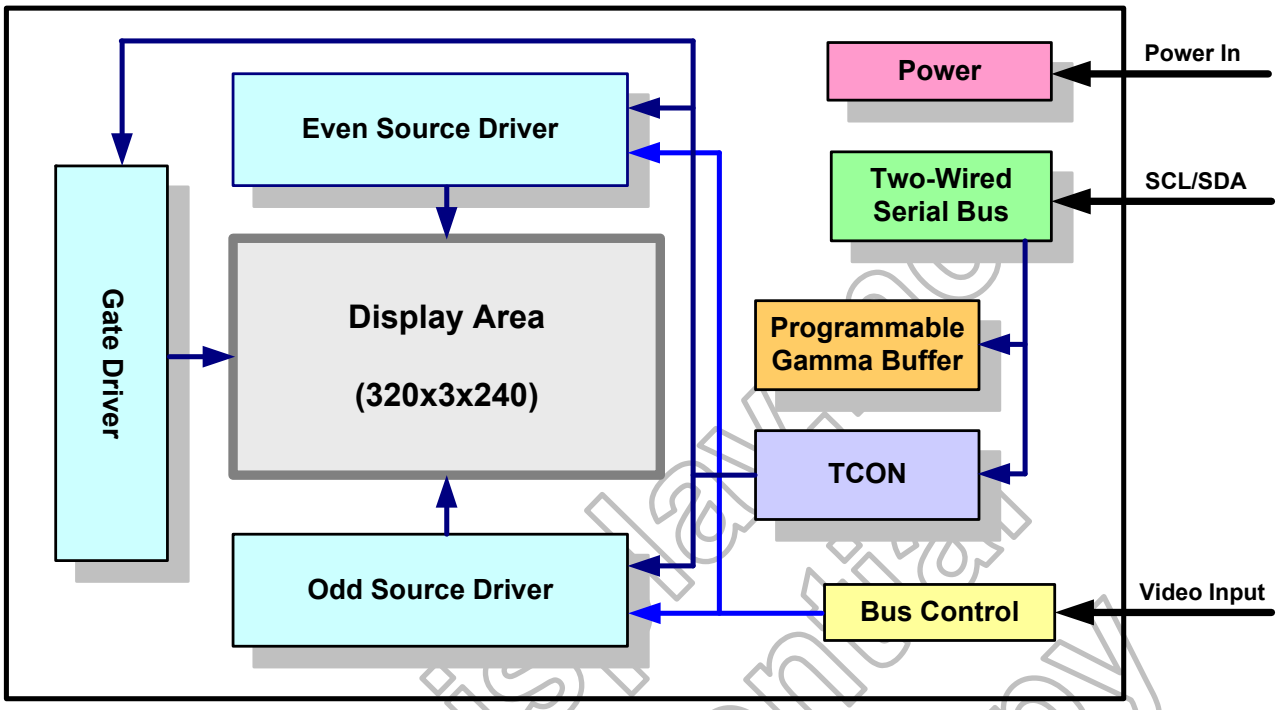
Note: (1) All values specified at a display ambient temperature of 25°C.
(2) For light with wavelength from 430mm to 650mm **(Refer to section 9.3)**

3.2. Recommended operating conditions

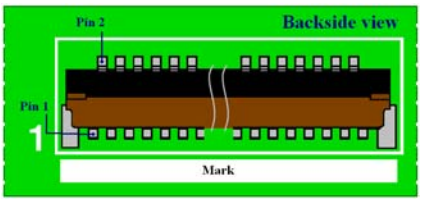
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDA	10.0	10.0	11.0	V
	VDDD	1.62	1.8/3.3	3.63	V
γ correction reference voltage	$V_{\gamma1}$ ~ $V_{\gamma6}$	0.5VDDA	-	VDDA-0.2	V
	$V_{\gamma7}$ ~ $V_{\gamma12}$	0.2	-	0.5VDDA	V
Operation frequency	F_{CLKX}	10.4	12.0	-	MHz
Illumination power[1],[3]	-	-	-	2.2	Mlux
Illumination wavelength[1],[3]	-	430	-	-	nm
Operation temperature[2],[3]	-	0	-	50	℃

Note: (1) If the maximum illumination power is larger than 2.2 Mlux or the illumination wavelength is smaller than 430nm, the life time of panel should be less than cumulative 3000 hours.
(2) If imager is operated at temperature higher than 50˚C **(on module substrate)**, the display will be appeared worse quality and its useful life will be reduced due to the characteristics of Liquid Crystal.
(3) The maximum operating conditions of illumination power and wavelength and operating temperature shall not be implemented simultaneously.

4. Block Diagram



5. Pin Assignment



Pin no.	Pin name
1	COM
3	NC
5	VDDAL
7	VSSA
9	VSSD
11	SCL
13	R4
15	R2
17	R0
19	INV
21	VDDD
23	G5
25	G3
27	G1
29	VSSD
31	B4
33	B2
35	B0

Pin no.	Pin name
2	NC
4	VDDA
6	BIASX
8	VSSAL
10	SDA
12	R5
14	R3
16	R1
18	DE
20	CLKX
22	RESETB
24	G4
26	G2
28	G0
30	B5
32	B3
34	B1

6. Pin Description

Pin name	Pin no.	I/O	Function description
R[5:0] G[5:0] B[5:0]	12~17 23~28 30~35	In	Display data input. The display data is input with 6-bit x 3-dot **(RGB)** per CLK clock. For each input dot, X0 is LSB and X5 is MSB.
DE	18	In	Display active. CMOS input pin.
INV	19	In	INV function to decrease EMI issue.
CLKX	20	In	X-axis shift clock input. The display data is stored to the internal data register at the edge of CLKX.
SDA	10	In/Out	Data for two-wired serial interface. Connect to VDDD with a pull-up resistor.
SCL	11	In	Clock for two-wired serial interface. Connect to VDDD with a pull-up resistor.
COM	1	Out	Reference common voltage output. **(No current)** Connect a 0.1μF capacitor to VSSA.
BIASX	6	In	Bias pin. Connect to VSSA with a bias resistor 100KΩ to generate driver bias current.
RESETB	22	In	Active low reset. When RESETB=0, panel is reset.
VDDA	4	In	Driver power supply. Connect to 10.0V power source.
VDDAL	5	In	Driver power supply for LS. Connect to 10.0V power source.
VDDD	21	In	Logic power supply. Connect to 1.8V or 3.3V power source.
VSSA	7	In	Grounding for VDDA.
VSSAL	8	In	Grounding for VDDAL.
VSSD	9,29	In	Grounding for VDDD.
NC	2~3	-	No connect.

7. Function Description

Following by the general timing standard of QVGA **(Refers to Chapter 7.1: Input timing)**, customers can light on the HX7033CTNPA display. If the DE is logically high, the HX7033CTNPA starts to latch input data into its line buffer immediately. Followed by the start pulse falling edge, a total 320 x 18-bit input data latched at 320 continuous at CLKX rising edge. Both gamma and COM are embedded with the HX7033CTNPA, which are programmable through two-wired serial bus.

7.1. Input timing (QVGA)

Parameter	Spec.			Unit
	Min.	Typ.	Max.	
Horizontal total	344	400	488	Pixel
Horizontal display	-	320	-	Pixel
Horizontal blanking	24	80	168	Pixel
Vertical total(1)	251	251	264	Line
Vertical display	-	240	-	Line
Vertical blanking	11	11	24	Line
Frame rate	120	120	-	Hz
Pixel clock	10.4	12.0	-	MHz

Note: (1) Use the minimum vertical total value will get the best CR.

Table 7.1: Timing parameter

7.2. Relationship between input data and output position

- Input data format: 6-bit x 3 **(4-dot per CLK)**
- Input data width: 18-bit **(1-pixel data)** with x 5 is MSB and x 0 is LSB

RL=H	Data first	→	Data last
	R[5:0]G[5:0]B[5:0]	•••	R[5:0]G[5:0]B[5:0]
OUT	OUT0	•••	OUT319
RL=L	Data last	←	Data first
	R[5:0]G[5:0]B[5:0]	•••	R[5:0]G[5:0]B[5:0]
OUT	OUT319	•••	OUT0

UD=H	Scan first	→	Scan last
Line	Line 1	•••	Line 240
UD=L	Scan last	←	Scan first
Line	Line 240	•••	Line 1

Table 7.2: Relationship between input data and output position

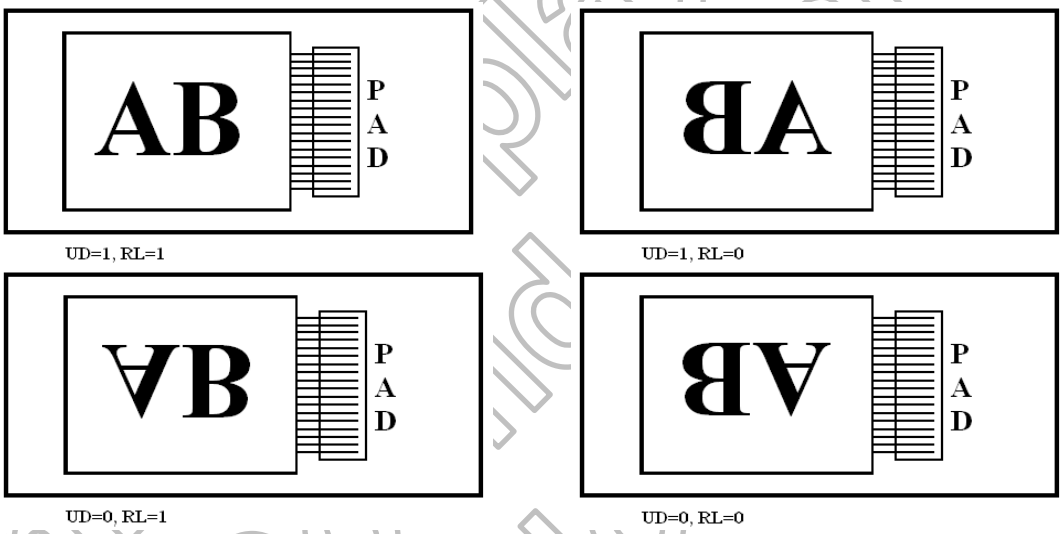


Figure 7.1: Display result

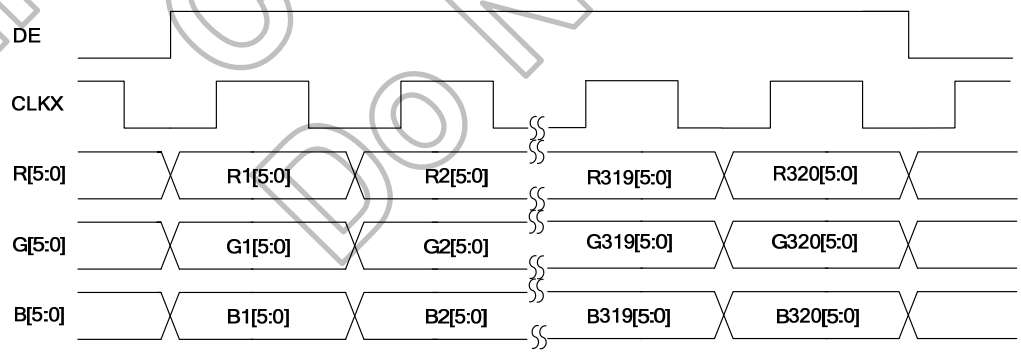


Figure 7.2: Timing diagram of DE, CLKX and input data (LR=H)

7.3. Relationship between input data and output voltage

The output voltage is determined by these 6-bit digital input data, internal signal POL, and the 6 γ correction reference voltage. Through 6 embedded with γ correction reference voltage, $V_{\gamma1}$~ $V_{\gamma6}$ are for positive polarity voltage output, and embedded with voltage $V_{\gamma7}$ ~ $V_{\gamma12}$ are for negative polarity voltage output.

7.4. Gamma correction characteristic curve

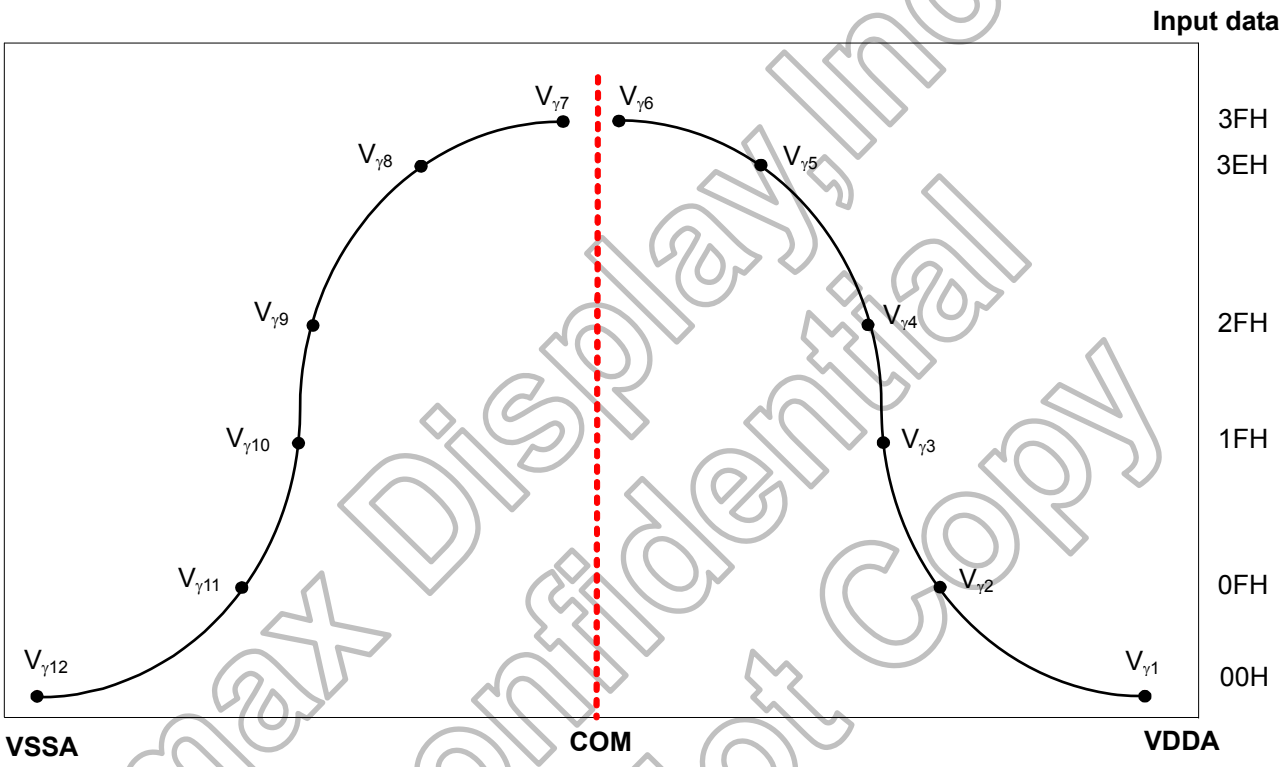


Figure 7.3: Gamma curve

7.5. Programmable gamma buffer

The HX7033CTNPA contains 12 x 3 **(RGB)** programmable gamma buffers. Each contains rail-to-rail output buffer and 8-bit resolution DAC **(Digital to Analog Converter)** with resistor-string voltage reference input. Reference voltage level is written by two-wired serial interface. Detail programmable address and default value refer to Table 7.4. Since the input coding to the DAC is straight binary and functions of positive polarity, negative polarity, gamma voltage and COM, the ideal output voltage is given by:

$$V_{rP} = VDDA - \frac{VDDA * D}{510}$$

$$V_{rN} = \frac{VDDA}{2} - \frac{VDDA * D}{510}$$

Where *D*=decimal equivalent **(0~255)** of the binary code that is loaded to the DAC register; $V_{\gamma P}=V_{\gamma 1} \sim V_{\gamma 6}$, $V_{\gamma N}=V_{\gamma 7} \sim V_{\gamma 12}$, COM voltage can select one of them **($V_{\gamma P}$ and $V_{\gamma N}$)** via a two-wired serial interface.

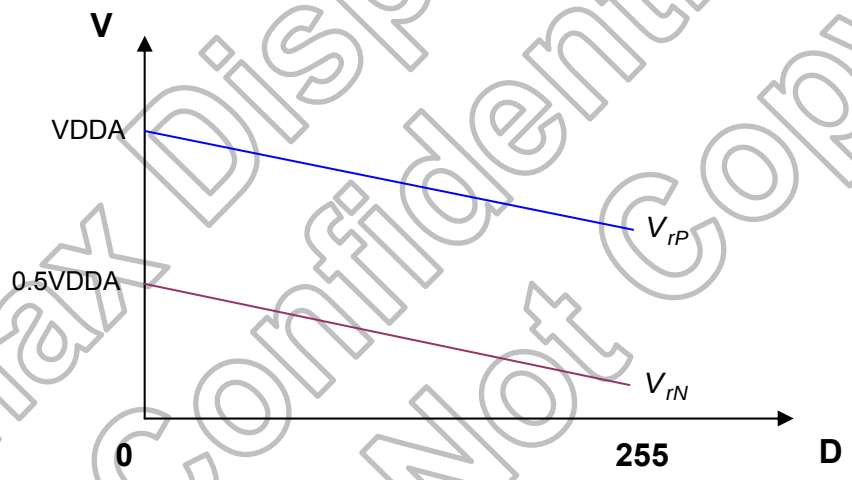


Figure 7.4: Relationship between output voltage and data

7.6. Serial interface

The HX7033CTNPA is controlled via a two-wired serial interface. The device is connected to this bus as a slave device. The HX7033CTNPA has a 7-bit slave address. There are seven MSBs as 1001000. **(Refer to chapter 7.7 Details of read/write sequence of the two-wire serial interface)**.

Two-wired serial bus protocol operates as follows

A. The master initiates data transfer by establishing a START condition, when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7th bit slave address followed by an *R/W* bit. **(this bit determines whether data will be read from or written to the slave device)**

The slave whose address corresponds to the transmitted address responds by pulling SDA low during the 9th clock pulse **(this is the Acknowledge bit)**. At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

B. Data is transmitted over the serial bus in sequences of nine clock pulses **(eight data bits followed by an Acknowledge bit)**. The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

C. When all data bits have been read or written to, a STOP condition is established. In Write/Read mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

7.7. Details of read/write sequence through two-wired serial interface

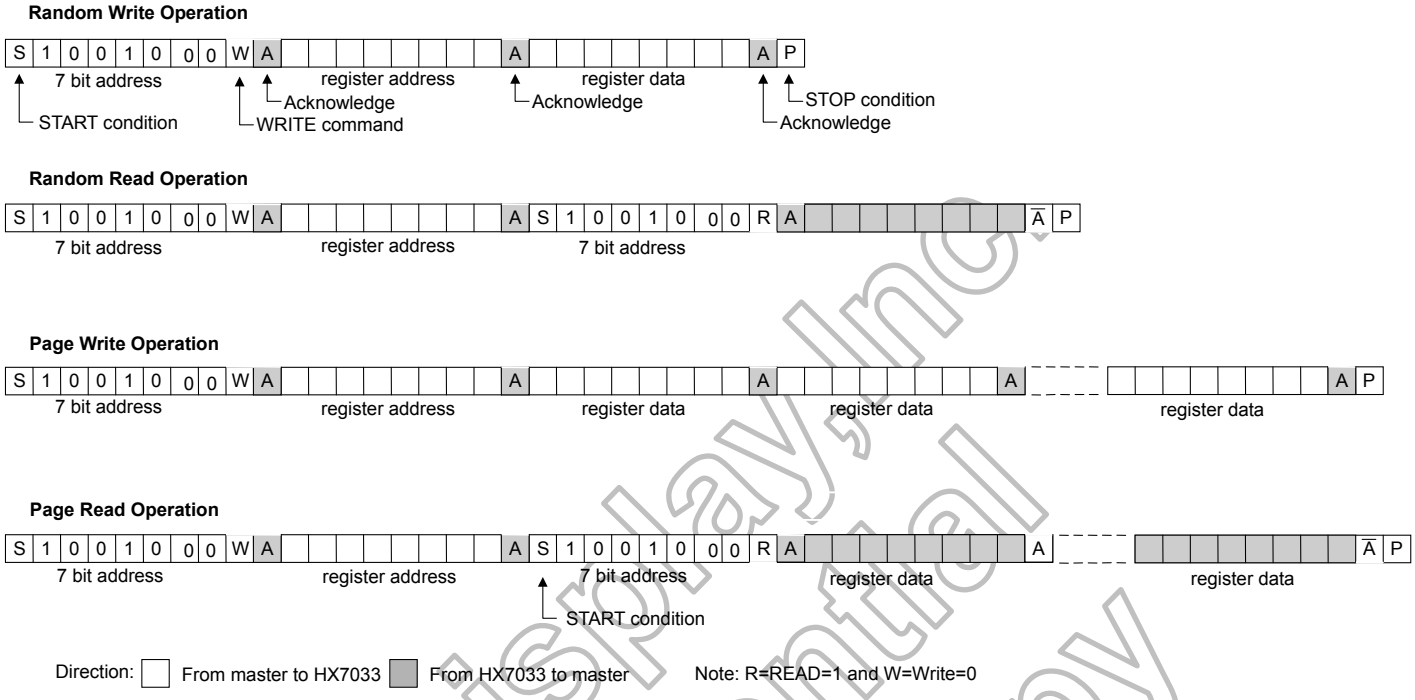


Figure 7.5: Read/write sequence of the two-wired serial bus

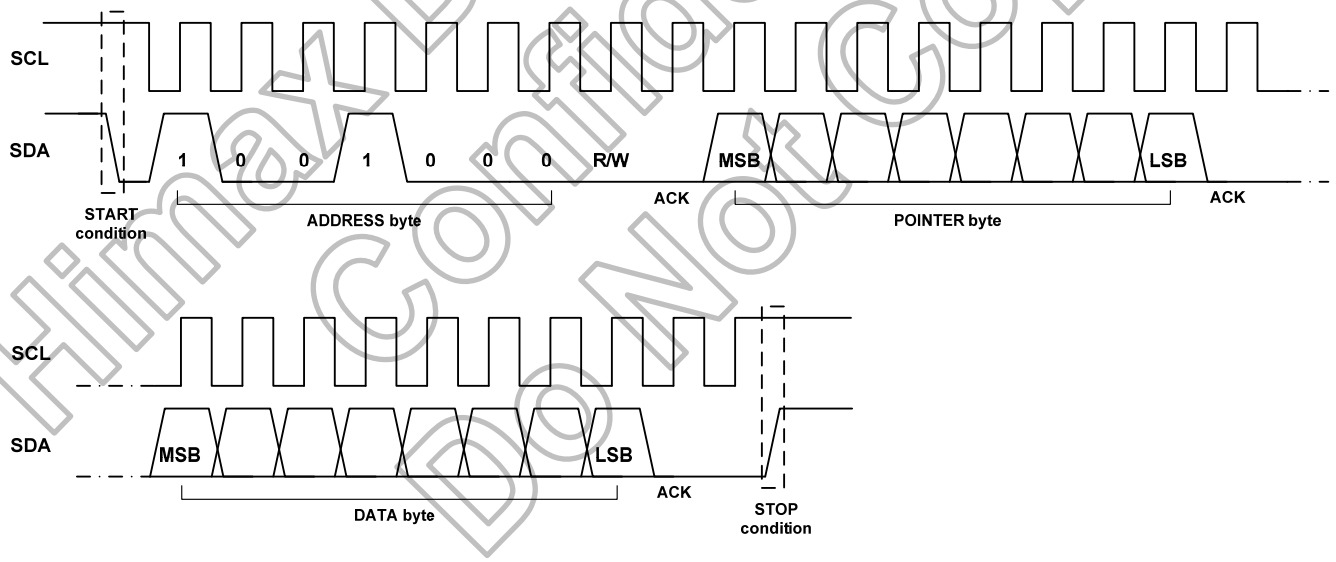


Figure 7.6: Timing diagrams of SCL and SDA

7.8. I2C description

Address	D7	D6	D5	D4	D3	D2	D1	D0	Default value	Function
00h	LR	UD	0	1	0	1	1	0	[1 , 1 , 0 , 1 , 0 , 1 , 1 , 0]	Control setting
01h	SC_I2C	0	0	0	0	0	0	0	[0 , 0 , 0 , 0 , 0 , 0 , 0 , 0]	Control setting

Table 7.3: I2C register table for control settings

Register	Description
LR	1, Display left to right. **(Default)**
UD	1, Display up to down. **(Default)**
SC_I2C	0, Disable single cell. **(Default)**
COMPN	1, COM range is 1/2VDDA~VDDA.
	0, COM range is 0~1/2VDDA.

Table 7.4: Description of control settings

Address	D7	D6	D5	D4	D3	D2	D1	D0	Function
0Ah	1	1	1	1	0	1	1	0	COM
0Bh	COMPN	0	0	0	0	0	0	0	COM
0Ch	0	0	0	0	0	0	0	0	$V_{\gamma R1P}$
0Dh	0	1	0	0	1	1	0	0	$V_{\gamma R2P}$
0Eh	0	1	1	0	1	0	1	1	$V_{\gamma R3P}$
0Fh	1	0	0	0	1	0	1	0	$V_{\gamma R4P}$
10h	1	0	1	1	0	1	0	1	$V_{\gamma R5P}$
11h	1	1	1	0	1	0	1	0	$V_{\gamma R6P}$
12h	0	0	0	1	0	1	0	1	$V_{\gamma R6N}$
13h	0	1	0	0	1	0	1	0	$V_{\gamma R5N}$
14h	0	1	1	1	0	1	0	1	$V_{\gamma R4N}$
15h	1	0	0	1	0	1	0	0	$V_{\gamma R3N}$
16h	1	0	1	1	0	0	1	0	$V_{\gamma R2N}$
17h	1	1	1	1	1	1	1	1	$V_{\gamma R1N}$
18h	0	0	0	0	0	0	0	0	$V_{\gamma G1P}$
19h	0	1	0	0	1	1	0	0	$V_{\gamma G2P}$
1Ah	0	1	1	0	1	0	1	1	$V_{\gamma G3P}$
1Bh	1	0	0	0	1	0	1	0	$V_{\gamma G4P}$
1Ch	1	0	1	1	0	1	0	1	$V_{\gamma G5P}$
1Dh	1	1	1	0	1	0	1	0	$V_{\gamma G6P}$
1Eh	0	0	0	1	0	1	0	1	$V_{\gamma G6N}$
1Fh	0	1	0	0	1	0	1	0	$V_{\gamma G5N}$
20h	0	1	1	1	0	1	0	1	$V_{\gamma G4N}$
21h	1	0	0	1	0	1	0	0	$V_{\gamma G3N}$
22h	1	0	1	1	0	0	1	0	$V_{\gamma G2N}$
23h	1	1	1	1	1	1	1	1	$V_{\gamma G1N}$
24h	0	0	0	0	0	0	0	0	$V_{\gamma B1P}$
25h	0	1	0	0	1	1	0	0	$V_{\gamma B2P}$
26h	0	1	1	0	1	0	1	1	$V_{\gamma B3P}$
27h	1	0	0	0	1	0	1	0	$V_{\gamma B4P}$
28h	1	0	1	1	0	1	0	1	$V_{\gamma B5P}$
29h	1	1	1	0	1	0	1	0	$V_{\gamma B6P}$
2Ah	0	0	0	1	0	1	0	1	$V_{\gamma B6N}$
2Bh	0	1	0	0	1	0	1	0	$V_{\gamma B5N}$
2Ch	0	1	1	1	0	1	0	1	$V_{\gamma B4N}$
2Dh	1	0	0	1	0	1	0	0	$V_{\gamma B3N}$
2Eh	1	0	1	1	0	0	1	0	$V_{\gamma B2N}$
2Fh	1	1	1	1	1	1	1	1	$V_{\gamma B1N}$

Table 7.5: I2C register table for default settings

8. Electrical Characteristics

8.1. Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDA	-0.5	-	13.3	V
	VDDD	-0.5	-	4.39	V
Input voltage	CMOS/TTL input	-0.5	-	VDDD	V
ESD	HBM	-	±2000	-	V
	MM	-	±200	-	V
	CDM	-	±1000	-	V
	Latch-up	-	±100	-	mA

Note: (1) The device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

8.2. DC characteristics

8.2.1. DC electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH1}	R[5:0], G[5:0], B[5:0], CLKX, DE, INV	0.7VDDD	-	VDDD	V
Low level input voltage	V_{IL1}		0	-	0.3VDDD	V
High level input voltage	V_{IH2}	SDA, SCL	0.8VDDD	-	VDDD	V
Low level input voltage	V_{IL2}		0	-	0.2VDDD	V
Input leakage current	I_L	Digital input pin	-1	-	1	μA
Static current	I_{VDDD_STA}	VDDD=1.8V/3.3V RESETB=0	-	1	-	μA

Note: (1) All values specified at a display ambient temperature of 25℃.

8.2.2. Power consumption

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Current of VDDA	I_{VDDA_ACT} **(@VDDA=10.0V)**	Pattern=256-level gray F_{CLKX}=12.0MHz	-	2.2	-	mA
		Pattern=R-purity F_{CLKX}=12.0MHz	-	2.6	-	mA
Current of VDDD	I_{VDDD_18} **(@VDDD=1.8V)**	Pattern=256-level gray F_{CLKX}=12.0MHz	-	1.1	-	mA
		Pattern= 2-pixel on/off F_{CLKX}=12.0MHz	-	2.0	-	mA
	I_{VDDD_33} **(@VDDD=3.3V)**	Pattern=256-level gray F_{CLKX}=12.0MHz	-	2.6	-	mA
		Pattern=2-pixel on/off F_{CLKX}=12.0MHz	-	4.0	-	mA

Note: (1) All values specified at a display ambient temperature of 25℃ by default gamma.

8.3. AC characteristics

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock pulse width	t_{CLKX}	20	69	-	ns
Clock pulse low period	$t_{CLKX(L)}$	10	34.5	-	ns
Clock pulse high period	$t_{CLKX(H)}$	10	34.5	-	ns
Data & DE setup time	t_{SETUP}	1	-	-	ns
Data & DE hold time	t_{HOLD}	5	-	-	ns

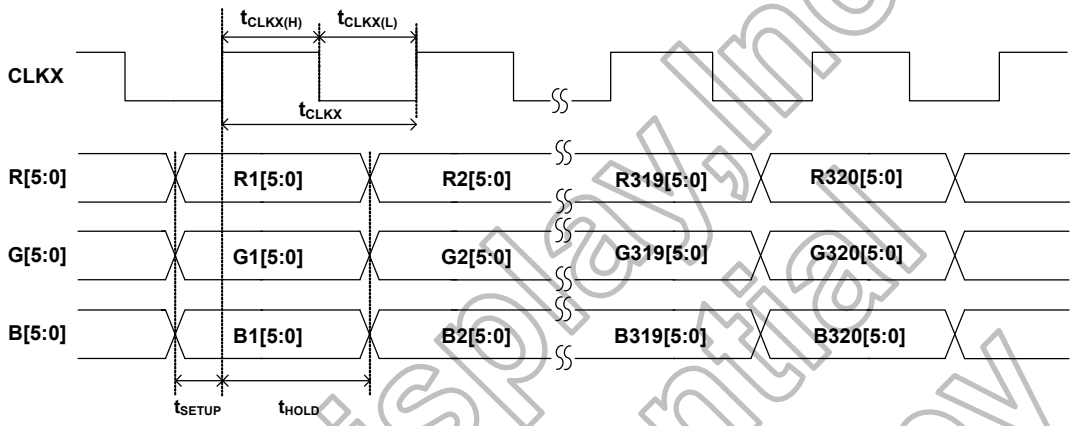


Figure 8.1: Input timing diagram

9. Optical Characteristics

Reflective Twisted Nematic liquid crystal mode is employed in the HX7033CTNPA. When no voltage is applied, the HX7033CTNPA presents bright state **(e.g. the normally white mode)**. The images darken up as the applied voltage increases. Different gray-level can be obtained by tuning the applied voltage

The HX7033CTNPA is a Color-Filter inside **(CF-LCOS)** design that exhibits color images by a single panel.

9.1. Test condition

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Ambient temperature	T_A	-	25±5	-	℃
Ambient humidity	H_A	-	50±20	-	%RH
Supply voltage	VDDA	-	6.0	-	V
Input signal	According to typical value in "Electrical Characteristics"				

9.2. Optical specifications

Parameter			Condition	Spec.			Unit
				Min.	Typ.	Max.	
Reflectance **(Luminance)**(1)		Y	%(430~650nm) @F/2.5	18	20	-	%
Uniformity of reflectance(2)			Measure 9 points as Figure 9.3	80	-	-	%
Contrast ratio(3)			Full white/black @F/2.5	100	170	-	-
Chromaticity(4)	R	X	%(430~650nm) @F/2.5 @Display center	0.540	0.580	0.620	-
		Y		0.324	0.364	0.404	-
	G	X		0.275	0.315	0.355	-
		Y		0.505	0.545	0.585	-
	B	X		0.121	0.161	0.201	-
		Y		0.079	0.119	0.159	-
	W	X		0.308	0.348	0.388	-
		Y		0.332	0.372	0.412	-
Response time(5)	T_R		Full bright to dark	-	5	-	ms
	T_F		Full dark to bright	-	10	-	ms
	T_R+T_F		-	-	15	-	ms

Note: (1) Definition of reflectance **(luminance, Y)**: Y is derived from "panel reflection spectrum" as shown below.

$$Y = k\int_{430nm}^{650nm} R(\lambda) \times \bar{y}(\lambda) d\lambda$$

where
R(λ) is the panel reflection spectrum
λ is the wavelength and
k is a constant as below:

$$k = \frac{100}{\int_{430nm}^{650nm} y(\lambda) d\lambda}$$

$\bar{y}$ (λ) is the spectral luminous efficiency function.

Y and white coordinates **(x, y)** are measured by MDIS **(Westar Inc.)** at gray level 255 at the display center.
Figure 9.1 shows the optic measurement system of MDIS.
Figure 9.2 shows the polarization direction of entrance light.

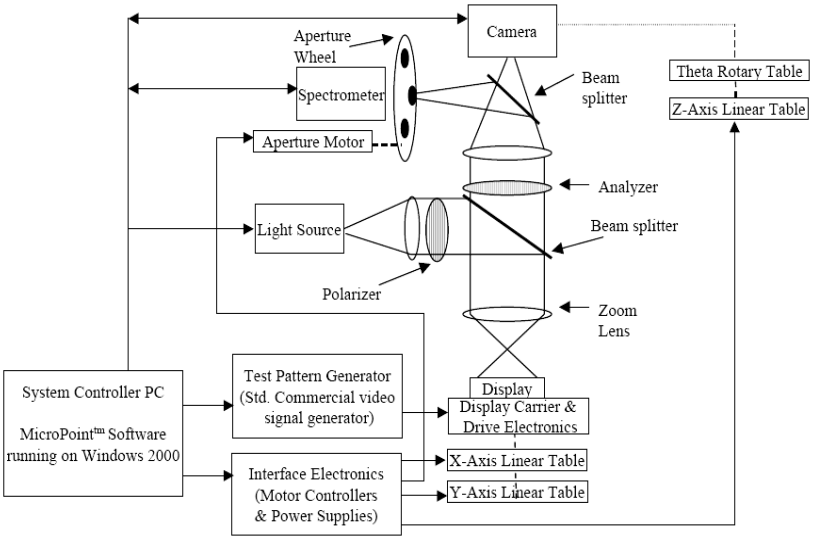


Figure 9.1: MDIS optic measurement systems

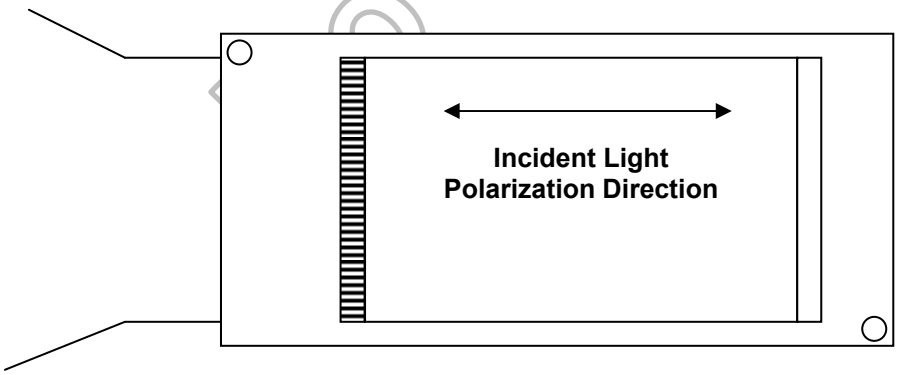


Figure 9.2: Polarization direction of entrance

(2) Definition of uniformity of reflectance
Measure the luminance of gray 255 at 9 points by MDIS.
Uniformity=Min.[L(1),L(2),L(3),L(4),L(5),L(6),L(7),L(8),L(9)] /
Max.[L(1),L(2),L(3),L(4),L(5),L(6),L(7),L(8),L(9)]

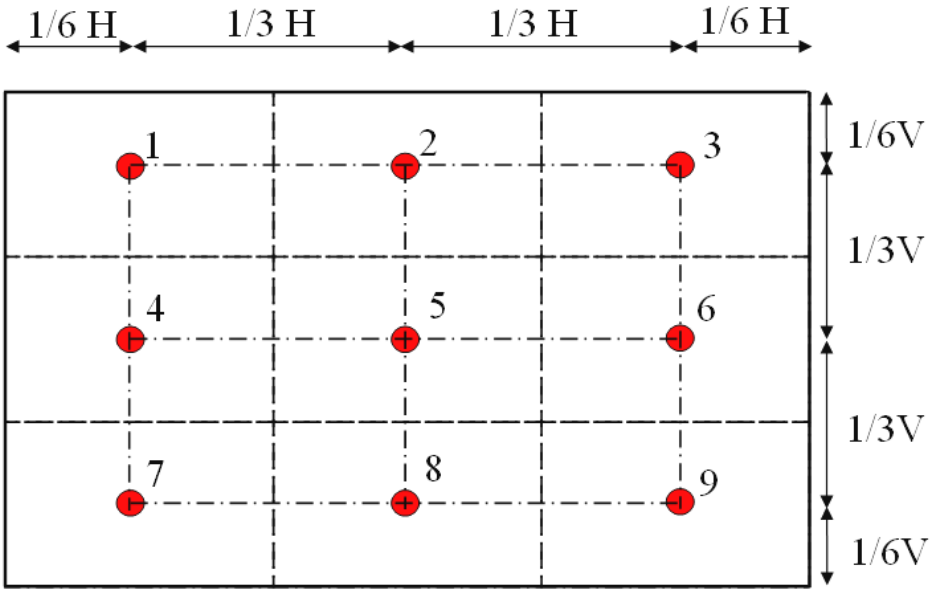


Figure 9.3: Definition of ANSI 9 points on panel

(3) Definition of contrast ratio:
Luminance of gray 255 and gray 0 are measured by MDIS at the center point. The contrast ratio is calculated by the following expression.
CR=L255/L0
L255=Luminance of gray level 255

(4) Definition of chromaticity
WRGB reflection spectra are measured by MDIS **(Westar Inc.)**
The color chromaticity values are calculated by assuming an equal intensity visible waveband **(430nm~650nm)** light source.

(5) Definition of response time **(T_R and T_F)**
Measured by HIMAX DISPLAY photo diode sensor & oscilloscope under temperature at 50℃.
Figure 9.4 Definitions of T_R and T_F

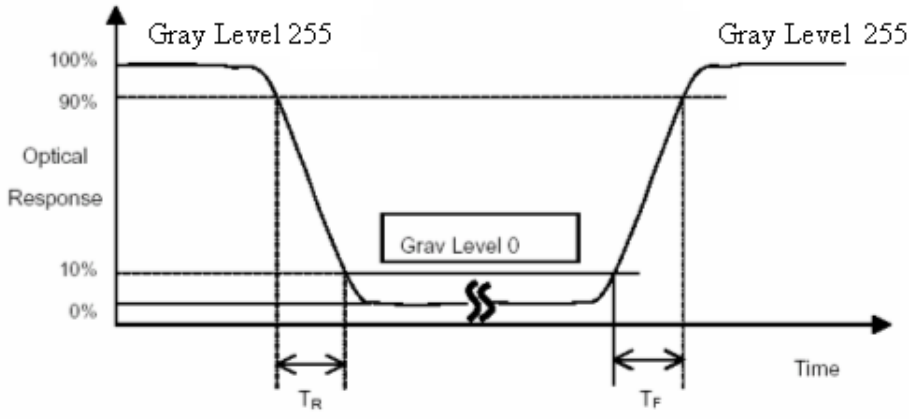


Figure 9.4: Definition of T_R and T_F

9.3. The panel reflection spectrum (Typical)

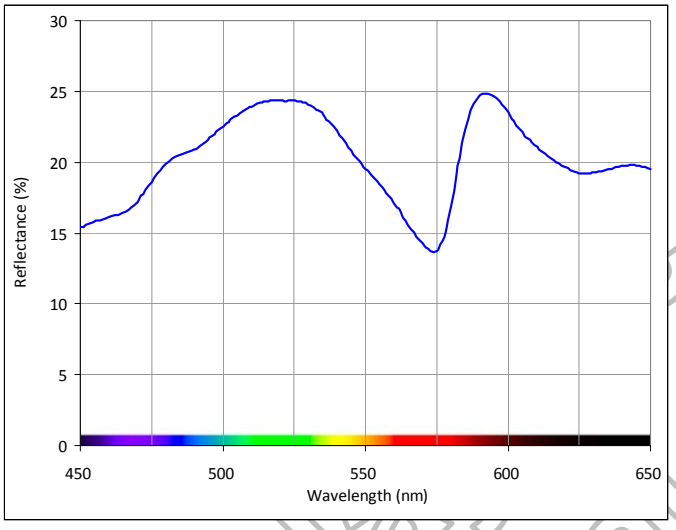


Figure 9.5: The panel reflection spectrum (Typical)

9.4. The panel Y-V curves (Typical)

The Y-V curve is measured by MDIS **(Westar Inc.)**. Normalized Y=Y/Ymax

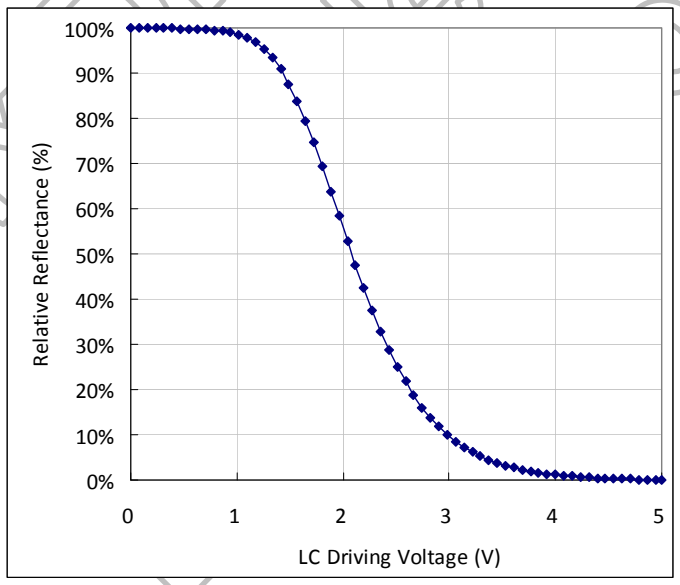


Figure 9.6: The panel Y-V curves (Typical)

10. Package Specifications

- Box content: 15 trays + cover tray. **(Each tray can contain 20 panels)**
- Box dimension: 368 **(L)** x 175 **(W)** x 245 **(H)** **(Unit: mm)**
- Gross weight: 1.4Kg

10.1. Packing procedure

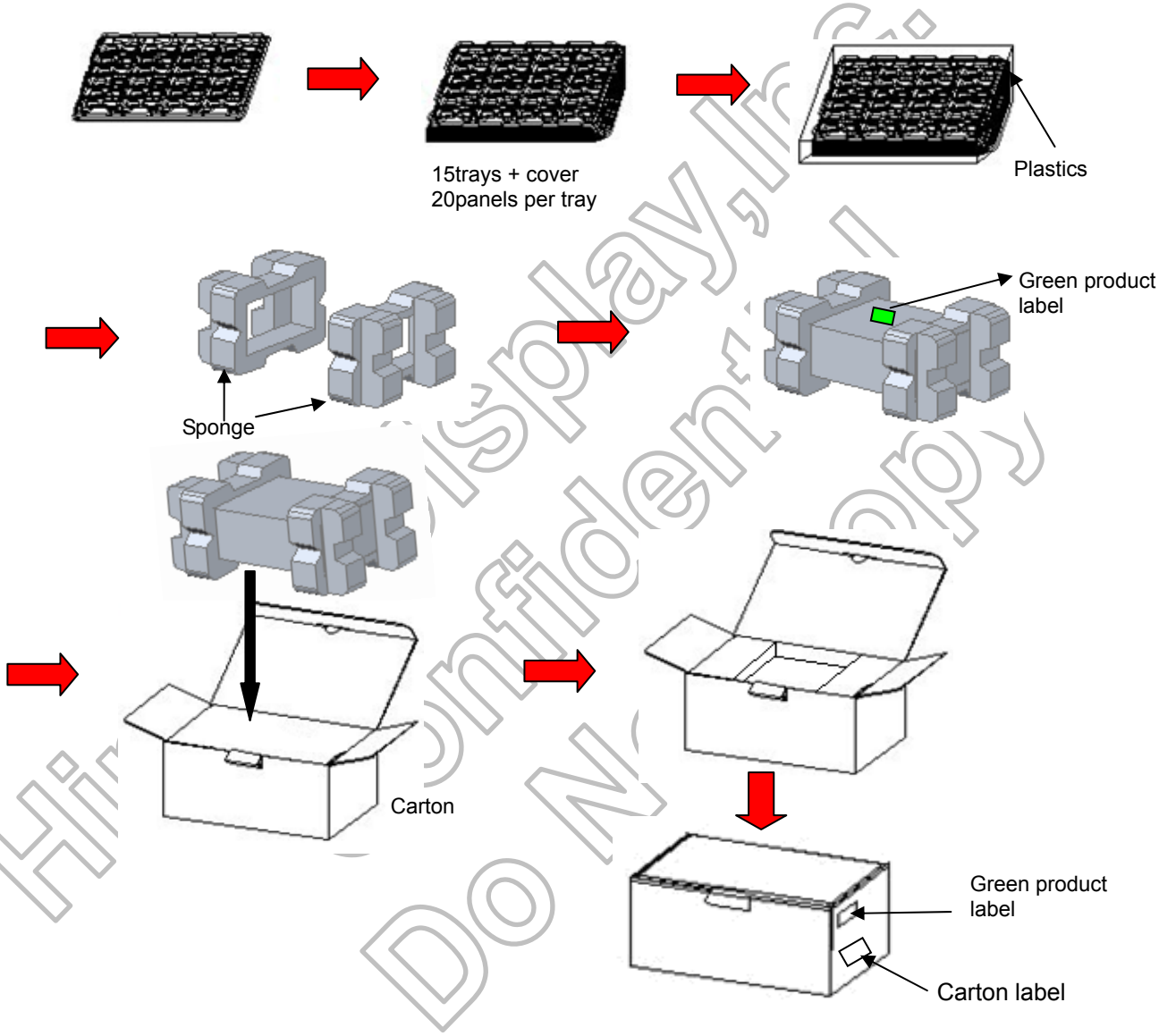


Figure 10.1: Packing procedure

10.2. Label information

10.2.1. Carton label

Label information indicates model name and shipping quantity.

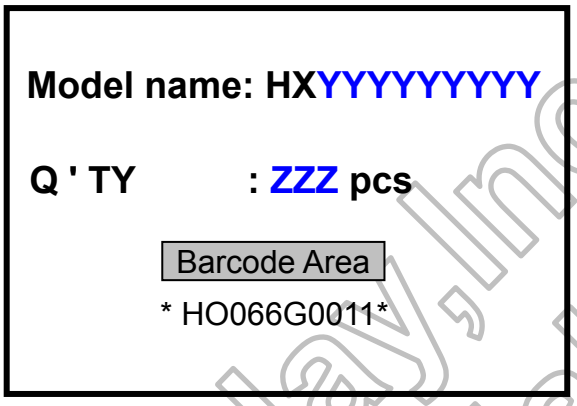


Figure 10.2: Label information

10.2.2. Green product label

Figure 10.3: Green product label

11. Green Product

The HX7033CTNPA is a RoHS **(Restriction on the use of certain Hazardous Substances)** compliance product.