SHION-M70 BT MODULE

技术手册

Version1.0

June 6 2013

一. Description:

SHION-M70 is an easy to use Bluetooth module, compliant with Bluetooth v4.0. The module provides complete RF platform in a small form factor.

The module enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The module being a certified solution optimizes the time to market of the final application.

The module built-in enhanced Kalimba DSP coprocessor with 80MIPS, supports enhanced audio and DSP Applications (t Apt-X, AAC, Apt-XLL, SBC codec).Support GATT,A2DP, AVRCP, HSP, HFP,SPP, iAP and PBAP Profiles communication with smart ready devices. The module offers all Bluetooth low energy features: radio, stack, profiles and application space for customer application, so no external processor is needed. The module also provides flexible hardware interfaces to connect sensors, simple user interface or even displays directly to the module.

The module has 14 x general purpose IOs, 2x Analogue inputs/outputs (temperature sensor, charger control, etc), 3xs capacitive touch sensors, three fully configurable LED drivers (PWM).The module optional support for 64Mb of external SPI flash 16Mb internal flash memory (64-bit wide, 45ns),support Li-Ion battery charger with Instant-ON.

二. Applications：

- Home entertainment eco-system
- TVs
- Wired or wireless soundbar
- Wired or wireless speakers and headphones
- Bluetooth low energy connectivity to external 3D
- Wired or wireless headphones for music / gaming / multimedia content
- Wired or wireless speakers
- Wired or wireless speaker phones
- Mono Headsets for voice

三. Features:

- Dual mode Bluetooth v4.0
- 9.5 dBm TX power/ -92.5dBm RX sensitivity

- Support master and slave operation
- Support Bluetooth low energy
- Profile: GATT,A2DP, AVRCP, HSP, HFP,SPP, iAP and PBAP
- UART, I2C, SPI, PCM, I2S,SPDIF, MIC,USB
- Aptx, aac, aptx-ll, sbc and mp3.
- 3 analog IOs, 3 led drivers and six capacitive touch sensor inputs.
- 10 bits ADC IOs
- SMT pads for easy and reliable PCB mounting, Internal chip antenna or U.FL port
- RoHS compliant

1. SHION-M70 PRODUCT NUMBERING

SHION-M70-X-V1.0

A. SHION ---------- COMPANY NAME
B. M70 --------- MODULE NAME
C. X ---------- A=ANTENNA E=U.FL
D. V ---------- HARDWARE REVISION

2. PINOUT AND TERMINAL DESCRIPTION

2.1 Pin configuration

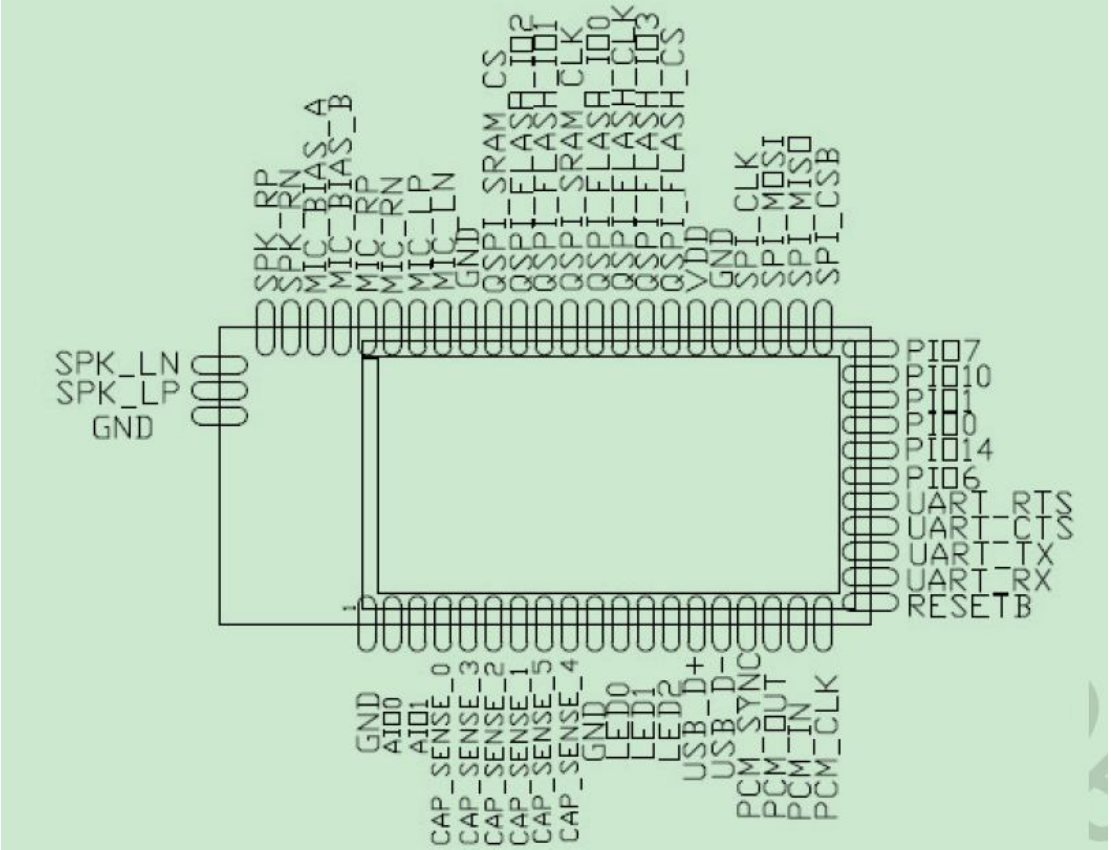

Figure 1: Pin out of SH-MC70

Symbol	Pin	PAD Type	Description
GND	1	Ground	Ground
AIO0	2	Bidirectional analogue	10bit analogue programmable I/O line
AIO1	3	Bidirectional analogue	10bit analogue programmable I/O line
CAP_SENSE0	4	Analogue input	Capacitive touch sensor input
CAP_SENSE3	5	Analogue input	Capacitive touch sensor input
CAP_SENSE2	6	Analogue input	Capacitive touch sensor input
CAP_SENSE1	7	Analogue input	Capacitive touch sensor input
CAP_SENSE5	8	Analogue input	Capacitive touch sensor input
CAP_SENSE4	9	Analogue input	Capacitive touch sensor input
GND	10	Ground	Ground
LED0	11	Open drain output	LED Driver

LED1	12	Open drain output	LED Driver
LED2	13	Open drain output	LED Driver
USB_D+	14	Bi-directional	USB data plus with selectable internal 1.5K pull up resistor
USB_D-	15	Bi-directional	USB data minus
PCM_SYNC	16	Bi-directional with weak internal pull-down	Synchronous Data Sync
PCM_OUT	17	CMOS output, tri-state, with weak internal pull-down	Synchronous Data Output
PCM_IN	18	CMOS Input, with weak internal pull-down	Synchronous Data Input
PCM_CLK	19	Bi-directional with weak internal pull-down	Synchronous Data Clock
RESETB	20	CMOS input with weak internal pull-up	Active LOW RESETB, input debounced so must be low for >5ms to cause a RESETB
UART_RX	21	CMOS input with weak internal pull-down	UART data input
UART_TX	22	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART data output
UART_CTS	23	Bi-directional with weak pull down	Uart clear to send ,active low
UART_RTS	24	Bi-directional with weak internal pull-up	uart request to send ,active low
PIO6	25	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO14	26	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO0	27	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO1	28	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO10	29	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO7	30	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
SPI_CSB	31	Input with weak internal pull-up	Chip select for Synchronous Serial Interface for programming only, active low
SPI_MISO	32	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface output for programming only
SPI_MOSI	33	CMOS input, with weak internal pull-down	Serial Peripheral Interface input for programming only
SPI_CLK	34	Input with weak internal pull-down	Serial Peripheral interface clock for programming only
GND	35	Ground	Ground

VDD_3V3	36	Power Supply	+2.7V- +4.2V power input
QSPI_FLASH_CS	37	Bi-directional with strong internal pull-down	SPI flash chip select
QSPI_FALSH_IO3	38	Bi-directional with strong internal pull-down	Serial quad I/O flash data bit 3
QSPI_FLASH_CLK	39	Bi-directional with strong internal pull-down	SPI flash clock
QSPI_FLASH_IO0	40	Bi-directional with strong internal pull-down	Serial quad I/O flash data bit 0
QSPI_SRAM_CLK	41	Bi-directional with strong internal pull-down	SPI RAM clock
QSPI_FLASH_IO1	42	Bi-directional with strong internal pull-down	Serial quad I/O flash data bit 1
QSPI_FLASH_IO2	43	Bi-directional with strong internal pull-down	Serial quad I/O flash data bit 2
QSPI_SRAM_CS	44	Bi-directional with strong internal pull-down	SPI RAM chip select
AGND	45	Audio Ground	Audio Ground
MIC_LN	46	Analogue	Microphone input negative, right
MIC_LP	47	Analogue	Microphone input positive, left
MIC_RN	48	Analogue	Microphone input negative, right
MIC_RP	49	Analogue \	Microphone input positive, right
MIC_BIAS_B	50	Analogue out	Microphone bias B
MIC_BIAS_A	51	Analogue out	Microphone bias A
SPK_RN	52	Analogue	Speaker output negative, right
SPK_RP	53	Analogue	Speaker output positive, right
SPK_LN	54	Analogue	Speaker output negative, left
SPK_LP	55	Analogue	Speaker output positive, left
GND	56	Ground	Ground

Table 1: PIN Terminal Description

3. ELECTRICAL CHARACTERISTICS

3.1. Absolute Maximum Rating

Table 2: Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+125	℃
PIO Voltage	-0.4	3.6	V
AIO Voltage	-0.4	+1.95	V
LED	-0.4	+4.4	V
VDD Voltage	-0.4	+4.4	V
VCHG	-0.4	+5.75	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages	Vss-0.4	VDD+0.4	V

***short-term operation up to a maximum of 10% of product lifetime is permissible without damage, but output regulation and other specification are not guaranteed in excess of 4.2V.**

3.2. Recommended Operation Conditions

Table 3: Recommended Operation Conditions

Operation Condition	Min	Typical	Max	Unit
Operating Temperature range	-40	--	+85	℃
PIO Voltage	+1.7	+3.3	+3.6	V
AIO Voltage	+1.7	+1.8	+1.95	V
LED	+1.1	3.7	+4.25	V
VDD Voltage	+2.5	+3.3	+4.25	V
VCHG(a)	+4.75	+5	+5.75	V
RF frequency	2400	2441	24800	MHz

3.3. Input/Output Terminal Characteristics

Table 4: Digital I/O Characteristics

Input Voltage Levels	Min	Typical	Max	Unit
VIL input logic level low	-0.4	--	0.4	V
VIH input logic level high	0.7xVDD	--	VDD+0.4	V
T_r/T_f	-	--	25	ns
Output Voltage Levels	**Min**	**Typical**	**Max**	**Unit**
VOL output logic level low, lOL = 4.0mA	--	--	0.4	V
VOH output logic level high, lOH = -4.0mA	0.75 x VDD	--		V
Tr/Tf	--	--	5	ns
Input and Tri-state Current	**Min**	**Typical**	**Max**	**Unit**

With strong pull-up	-150	-40	-10	µA
With strong pull-down	10	40	150	µA
With weak pull-up	-5.0	-1.0	-0.33	µA
With weak pull-down	0.33	+1.0	5.0	µA
CI Input Capacitance	1.0	-	5.0	pF

Table 5: AIO Characteristics

Input Voltage Levels	Min	Typical	Max	Unit
AIO	0	-	1.3	v

Table 6 ESD Protection

Condition	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114	2	2000V (all pins)
Machine Model Contact Discharge per JEDEC EIA/JESD22-A115	200V	200V (all pins)
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	III	500V (all pins)

3.4. Power Consumption

The current consumption are measured at the VBAT

Table 7: Current Consumption

DUT Role	Connection		Packet Type	Average Current	Unit
N/A	**Deep sleep**	**With UART host connection**	**-**	**55**	**uA**
N/A	**Page scan**	**Page = 1280ms interval Window = 11.25ms**	**-**	**219**	**uA**
N/A	**Inquiry and page scan**	**Inquiry = 1280ms interval Page = 1280ms interval Window = 11.25ms**	**-**	**378**	**uA**
Master	**ACL**	**Sniff = 500ms, 1 attempt, 0 timeout**	**DH1**	**119**	**mA**
Master	**ACL**	**Sniff = 1280ms, 8 attempts, 1 timeout**	**DH1**	**109**	**mA**
Master	**SCO**	**Sniff = 100ms, 1 attempt, PCM**	**HV3**	**7.6**	**mA**
Master	**SCO**	**Sniff = 100ms, 1 attempt, mono audio codec**	**HV3**	**9.8**	**mA**
Master	**eSCO**	**Setting S3, sniff = 100ms, PCM**	**2EV3**	**5.8**	**mA**
Master	**eSCO**	**Setting S3, sniff = 100ms, PCM**	**3EV3**	**5.4**	**mA**
Master	**eSCO**	**Setting S3, sniff = 100ms, mono audio codec**	**2EV3**	**7.9**	**uA**
Master	**eSCO**	**Setting S3, sniff = 100ms, mono audio codec**	**3EV3**	**7.5**	**uA**
Slave	**ACL**	**Sniff = 500ms, 1 attempt, 0 timeout**	**DH1**	**127**	**mA**

Slave	ACL	Sniff = 1280ms, 8 attempts, 1 timeout	DH1	129	mA
Slave	SCO	Sniff = 100ms, 1 attempt, PCM	HV3	7.8	mA
Slave	SCO	Sniff = 100ms, 1 attempt, mono audio codec	HV3	10	mA
Slave	eSCO	Setting S3, sniff = 100ms, PCM	2EV3	6.2	mA
Slave	eSCO	Setting S3, sniff = 100ms, PCM	3EV3	5.8	mA
Slave	eSCO	Setting S3, sniff = 100ms, mono audio codec	2EV3	8.2	mA
Slave	eSCO	Setting S3, sniff = 100ms, mono audio codec	3EV3	7.9	mA

Note: Current consumption values are taken with:

- VBAT pin = 3.7V
- Firmware ID = 7919
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH off

3.5. USB

	Min	Type	Max	Unit
VDD_USB for correct USB operation	3.10	3.30	3.60	V
Input Threshold				
VIL input logic level low	-	-	0.30 x VDD_USB	V
VIH input logic level high	0.70 x VDD_USB	-	-	V
Input Leakage Current				
VSS_DIG < VIN < VDD_USB(a)	-1	1	5	µA
CI input capacitance	2.5	-	10	pF
Output Voltage Levels to Correctly Terminated USB Cable				
VOL output logic level low	0	-	0.2	V
VOH output logic level hig	2.80	-	VDD_USB	V

Table 8: USB Terminal

3.6. Internal CODEC Analogue to Digital Converter

Parameter	Conditions		Min	Type	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz	Fsample				
	B/W = 20Hz→Fsample/2 (20kHz max)	8kHz	-	93	-	dB
	A-Weighted	16kHz	-	92	-	dB
	THD+N < 0.1%	32kHz	-	92	-	dB
	1.6Vpk-pk input	44.1kHz	-	92	-	dB

		48kHz	-	92	-	dB
THD+N	fin = 1kHz	Fsample				
	B/W = 20Hz→Fsample/2 (20kHz max)	8kHz	-	0.004	-	%
	1.6Vpk-pk input	48kHz	-	0.008	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	-21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB steps		3	-	42	dB
Stereo separation (crosstalk)			-	-89	-	dB

Table 9: Analogue to Digital Converter

3.6. Internal CODEC Digital to Analogue Converter

Parameter	Conditions			Min	Type	Max	Unit
Resolution	-			-	-	16	Bits
Output Sample Rate	-			8	-	96	kHz
SNR	fin = 1kHz	Fsample	Load				
	B/W = 20Hz→20kHz	48kHz	100kΩ	-	96	-	dB
	A-Weighted	48kHz	32Ω	-	96	-	dB
	THD+N < 0.01%	48kHz	16Ω	-	96	-	dB
	0dBFS input						
THD+N	fin = 1kHz	Fsample	Load				
	B/W = 20Hz→20kHz	8kHz	100kΩ	-	0.002	-	%
	0dBFS input	8kHz	32Ω	-	0.002	-	%
		8kHz	16Ω	-	0.002	-	%
		48kHz	100kΩ	-	0.002	-	%
		48kHz	32Ω	-	0.002	-	%
		48kHz	16Ω	-	0.002	-	%
Digital gain	Digital gain resolution = 1/32			-24	-	-21.5	dB
Analogue gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Stereo separation (crosstalk)				-	-88	-	dB

Table 10: Digital to Analogue Converter

4. PHYSICAL INTERFACES

4.1 Pio Power Supply

- The module DC3.3V power input.
- Power supply pin connection capacitor to chip and pin as far as possible close
- Capacitor decouples power to the chip
- Capacitor prevents noise coupling back to power plane.

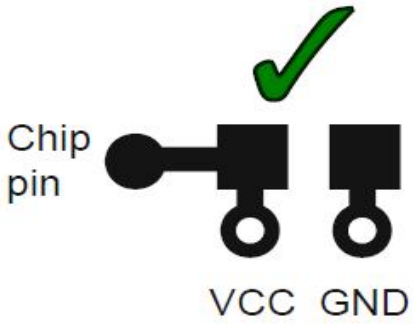

Figure 2: Power Supply PCB Design

4.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via software configured watchdog timer.

The RESETB pin is an active low RESETB and is internally filtered using the internal low frequency clock oscillator. A RESETB will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

At RESETB the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown below.

Pin Name / Group	Pin Status on RESETB
USB_DP	N/a
USB_DN	N/a
UART_RX	Strong PU
UART_TX	Weak PU
UART_RTS	Weak PU
UART_CTS	Weak PD
SPI_MOSI	Weak PD
SPI_CLK	Weak PD
SPI_CSB	Strong PU
SPI_MISO	Weak PD
RESET	Strong PU
PIOs	Weak PD

PCM_IN	Weak PD
PCM_CLK	Weak PD
PCM_SYNC	Weak PD
PCM_OUT	Weak PD
QSPI_SRAM_CS	Strong PU
QSPI_FLASH_CS	Strong PU
QSPI_SRAM_CLK	Strong PD
QSPI_FLASH_CLK	Strong PD

Table 11: Pin Status on Reset

4.3 Pio

SH-MB18 has a total of 13digital programmable I/O terminals. They are powered from VDD . Their functions depend on firmware running on the device. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs.

Note:

All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

4.4 AIO

SH-MB18 has 2 analogue I/O terminals. Their functions depend on software. Typically ADC functions can be configured to battery voltage measurement. They can also be used as a digital PIO.

4.5 RF interface

SH-MB18 internet chip antenna and U.fl port choose one of the ways. U.fl port external antenna, impedance is 50 ohm.

4.6 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

4.7 I2C Master

PIO6, PIO7 and PIO8 can be used to form a master I2C interface. The interface is formed

using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, keyboard scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2KΩ resistors.

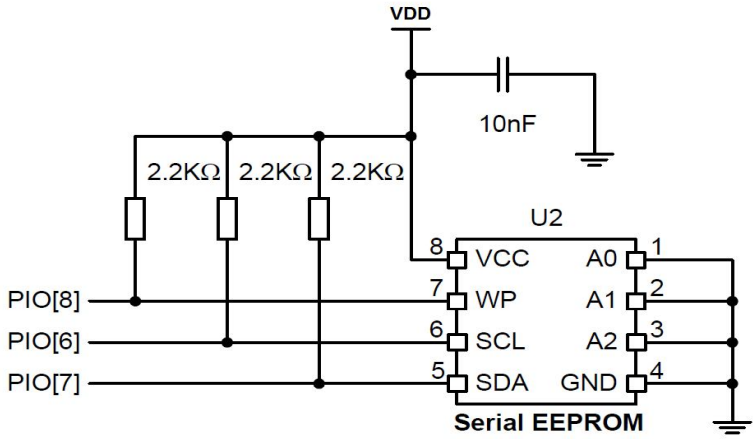

Figure 3 : Example EEPROM Connection with I2C Interface

4.8 Apple iOS CP reference design

The figures below give an indicative overview of what the hardware concept looks like. A specific MFI co-processor layout is available for licensed MFI developers from the MFI program.

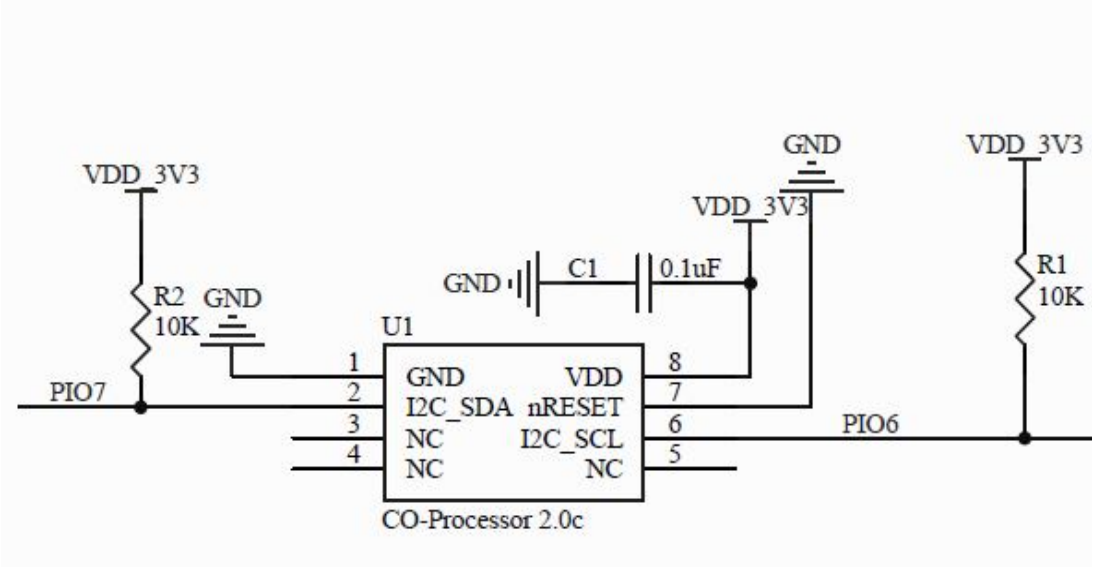

Figure 4 : Apple Co-processor 2.0C

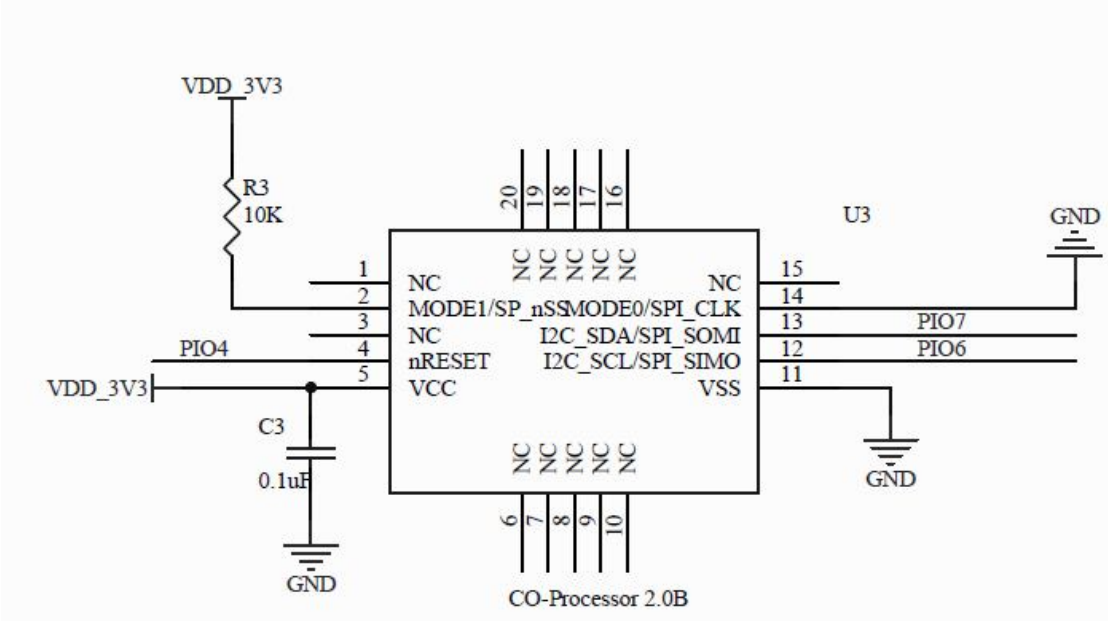

Figure 5 : Apple Co-processor 2.0B

4.9 Digital Audio Interfaces

The audio interface circuit consists of:

■ Stereo/Dual-mono audio codec

■ Dual audio inputs and outputs

■ 6 digital MEMS microphone inputs

■ A configurable PCM, I²S or SPDIF interface

Figure 2 outlines the functional blocks of the interface. The codec supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the codec each contain 2 independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

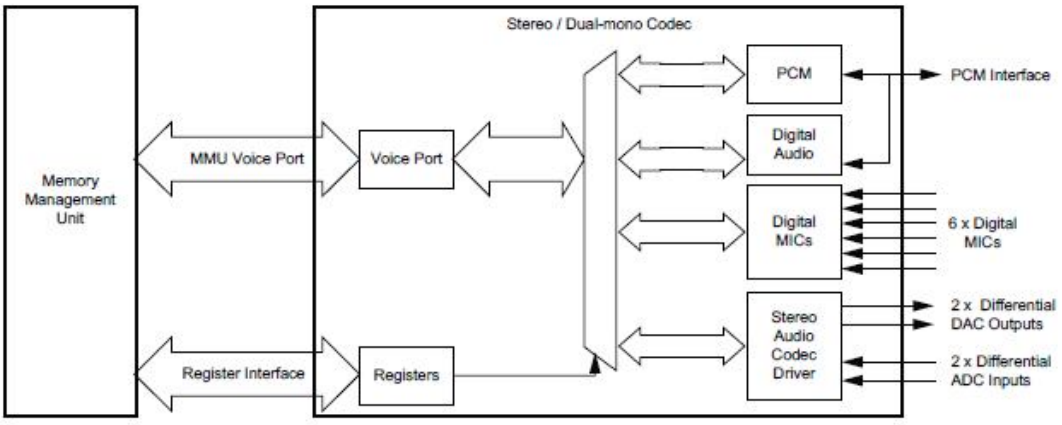

Figure 6 : Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface described in Table 11, which means each of the audio buses are mutually exclusive in their usage. Table 11 lists these alternative functions.

PCM INTERFACE	SPDIF INTERFACE	I²S INTERFACE
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Table 11: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimization of different microphones.

The audio output circuitry consists of a dual differential class A-B output stage.

4.10 PCM

The audio pulse code modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

Hardware on SH-MB18 allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

SH-MB18 can operate as the PCM interface master generating PCM_SYNC and PCM_CLK or as a PCM interface slave accepting externally generated PCM_SYNC and PCM_CLK.

SH-MB18 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit u-law or A-law companded sample formats and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

SH-MB18 interfaces directly to PCM audio devices including the following:

■ Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices

■ OKI MSM7705 four channel A-law and μ-law CODEC

■ Motorola MC145481 8-bit A-law and μ-law CODEC

■ Motorola MC145483 13-bit linear CODEC

■ STW 5093 and 5094 14-bit linear CODECs(8)

■ SH-MB18 is also compatible with the Motorola SSI interface

4.11 Digital Audio Interface (I2S)

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins of the PCM interface as Table 11.

Special firmware is needed if I2S is used. Contact EHong for the special firmware when use I2S as the interface between the module and the host or the codec. The I2S support following formats

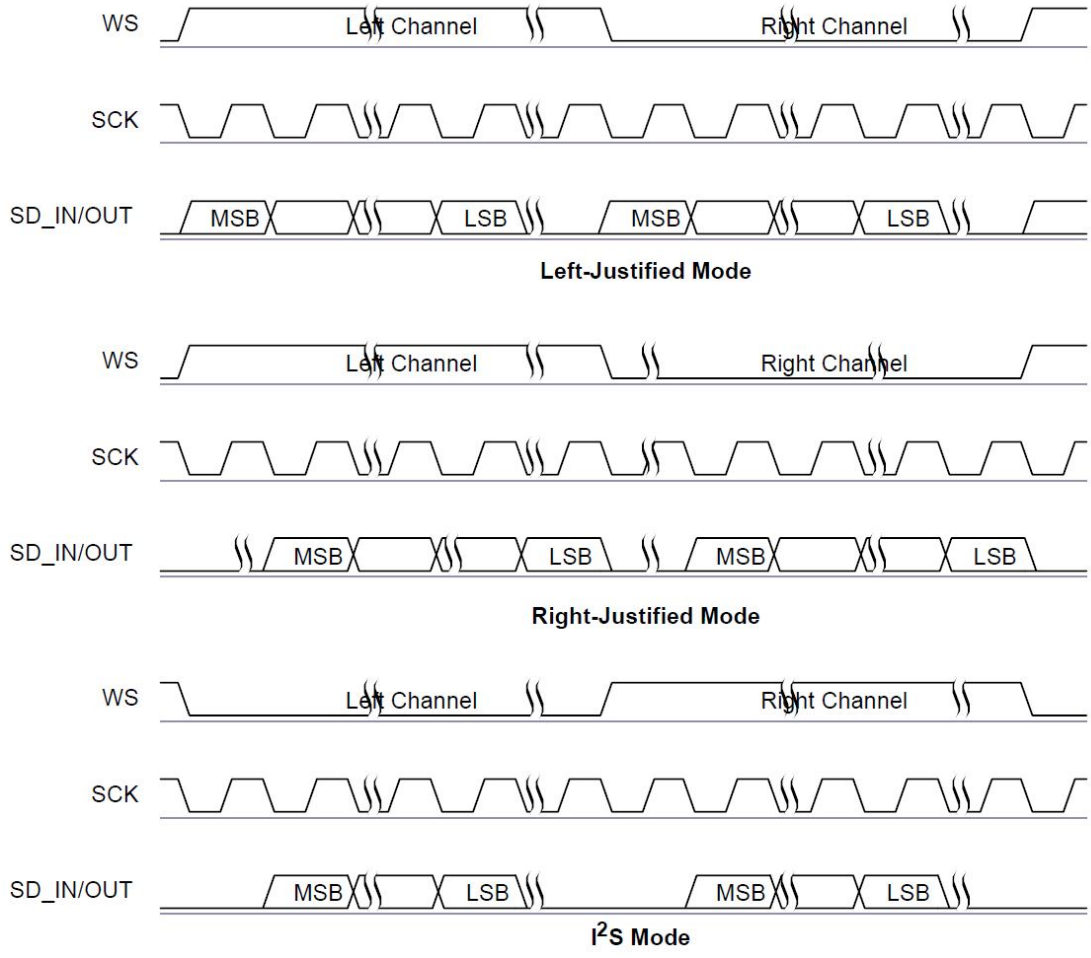

Figure 7 : Digital Audio Interface Modes

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency \	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

tch	SCK high time	80	-	-	ns
tcl	SCK low time	80	-	-	ns
topd	SCK to SD_OUT delay	-	-	20	ns
tssu	WS to SCK set up time	20	-	-	ns
tsh	WS to SCK hold time	20	-	-	ns
tisu	SD_IN to SCK set-up time	20	-	-	ns
tih	SD_IN to SCK hold time	20	-	-	ns

Table 12 : Digital Audio Interface Slave Timing

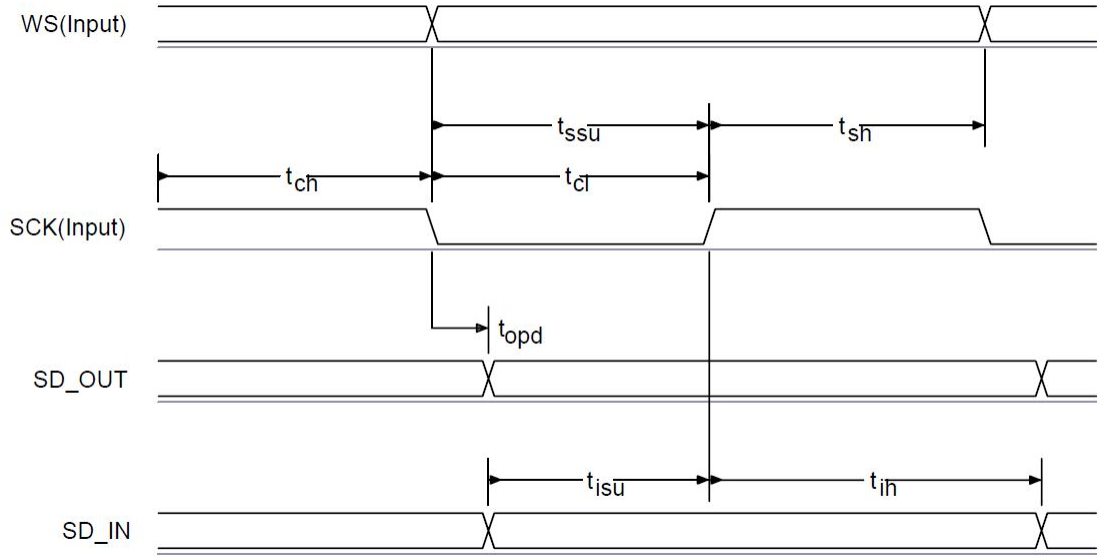

Figure 8 : Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency \	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
topd	SCK to SD_OUT delay	-	-	20	ns
tspd	SCK to WS delay	-	-	20	Ns
tisu	SD_IN to SCK set-up time	20	-	-	Ns
tih	SD_IN to SCK hold time	10	-	-	Ns

Table 13: Digital Audio Interface Master Timing

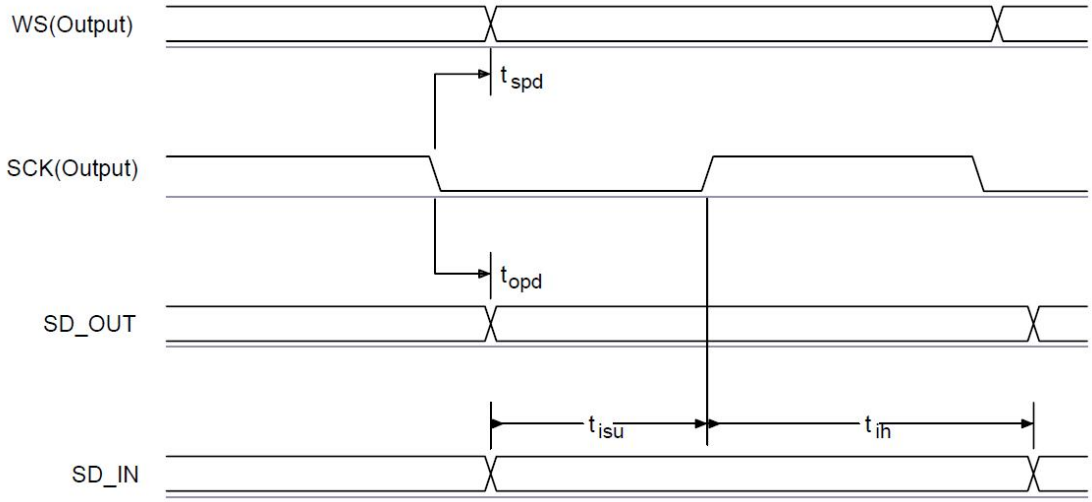

Figure 10 : Digital Audio Interface Master Timing

4.12 IEC 60958 Interface (SPDIF)

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the 2 industry standards:

■ AES/EBU

■ Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins. The input and output stages of the SPDIF pins can interface to:

■ A 75Ω coaxial cable with an RCA connector, see Figure 11.

■ An optical link that uses Toslink optical components, see Figure 12.

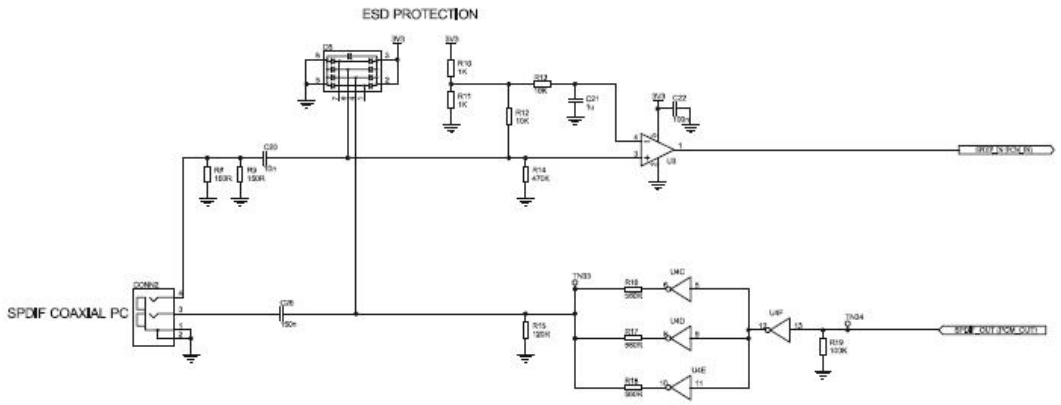

Figure 11: Example Circuit for SPDIF Interface (Co-Axial)

Figure 12: Example Circuit for SPDIF Interface (Optical)

4.13 Microphone input

The module contains 2 independent low-noise microphone bias generators. The microphone bias generators are recommended for biasing electret condensor microphones. Figure 9.6 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa):

Where:

■ The microphone bias generators derives their power from VBAT or VOUT_3V3 \ and requires no capacitor on its output.

■ The microphone bias generators maintains regulation within the limits 70μA to 2.8mA, supporting a 2mA source typically required by 2 electret condensor microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

■ Biasing resistors R1 and R2 equal 2.2kΩ.

■ The input impedance at MIC_LN, MIC_LP, MIC_RN and MIC_RP is typically 6kΩ.

■ C1, C2, C3 and C4 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.

■ R1 and R2 set the microphone load impedance and are normally around 2.2kΩ.

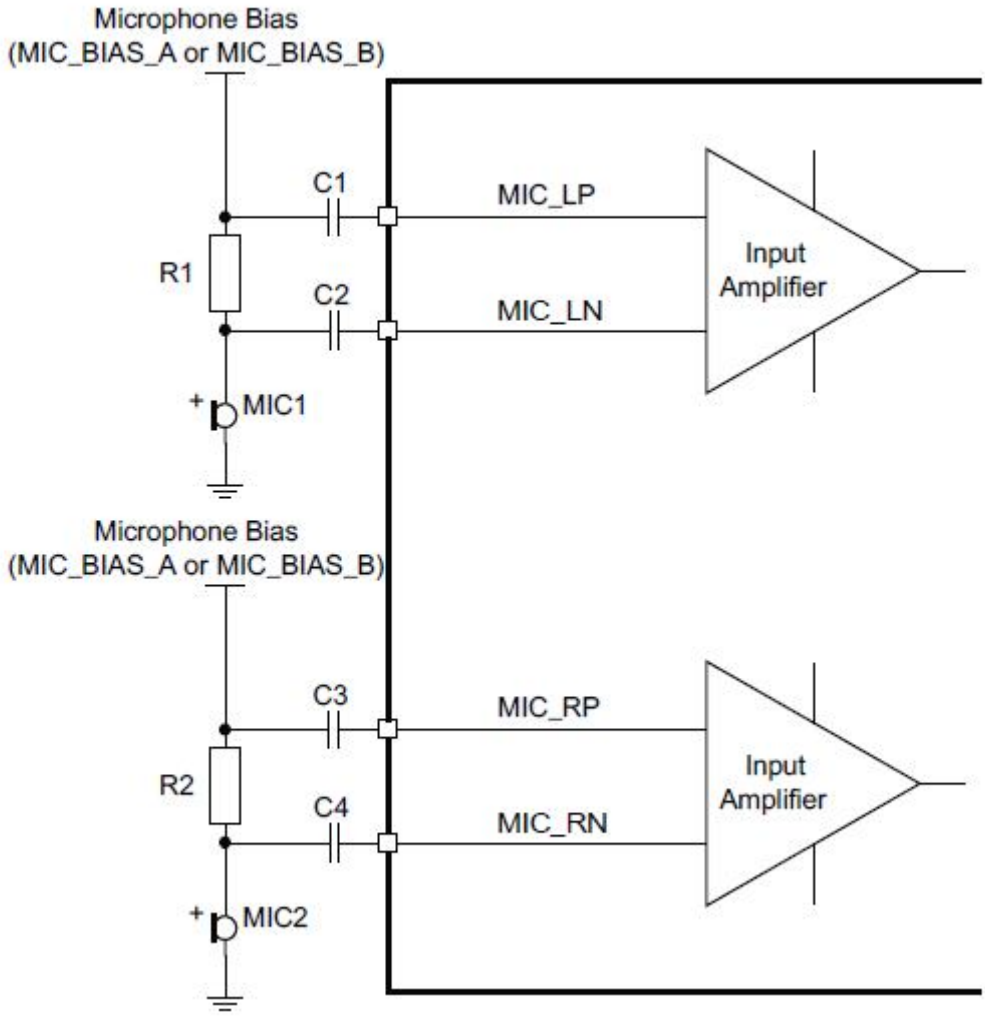

Figure 13: Microphone Biasing (Single Channel Shown)

The microphone bias characteristics include:

■ Power supply:

■ CSR8670 BGA microphone supply is VBAT (via SMP_VBAT) or VOUT_3V3 (via SMPS_3V3)

■ Minimum input voltage = Output voltage + drop-out voltage

■ Maximum input voltage is 4.25V

■ Drop-out voltage:

■ 300mV maximum

■ Output voltage:

■ 1.8V or 2.6V

■ Tolerance 90% to 110%

■ Output current:

■ 70μA to 2.8mA

■ No load capacitor required

4.14 Analog Output stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/s 5-bit multi-bit bit stream, which is fed into the analogue output circuitry.

The output stage circuit is comprised a DAC with gain setting and class AB amplifier. The output is available as a differential signal between SPKR_A_N and SPKR_L_P for the right channel, as Figure 6 shows, and between SPKL_B_N and SPKL_B_P for the left channel.

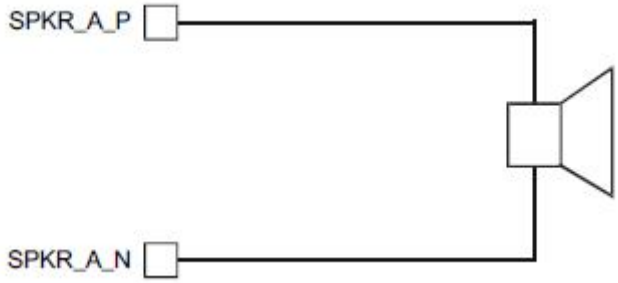

Figure 14: Speaker output

4.15 USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.1+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

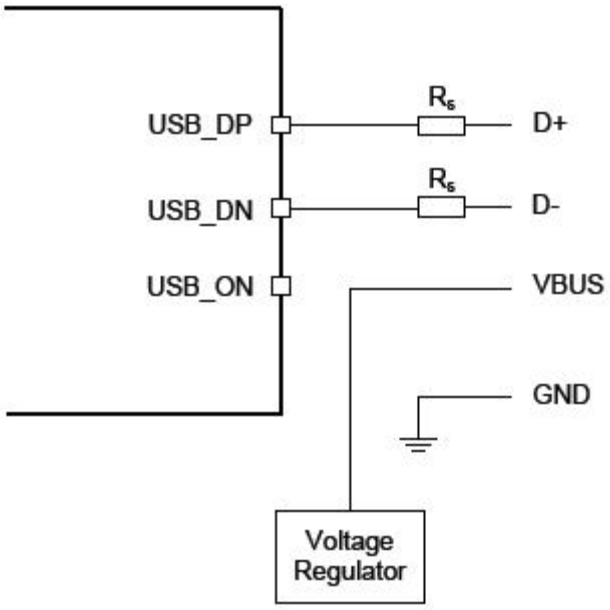

Figure 15: USB Connections

Note:

USB_ON is only used when the firmware need an input to detect if USB is connected and the USB function shall be enabled. In such case it is shared with the module PIO terminals. If detection is not needed (firmware already runs with USB, such as USB DFU or USB CDC), USB_ON is not needed.

RS: 27Ω Nominal

5. REFERENCE DESIGN

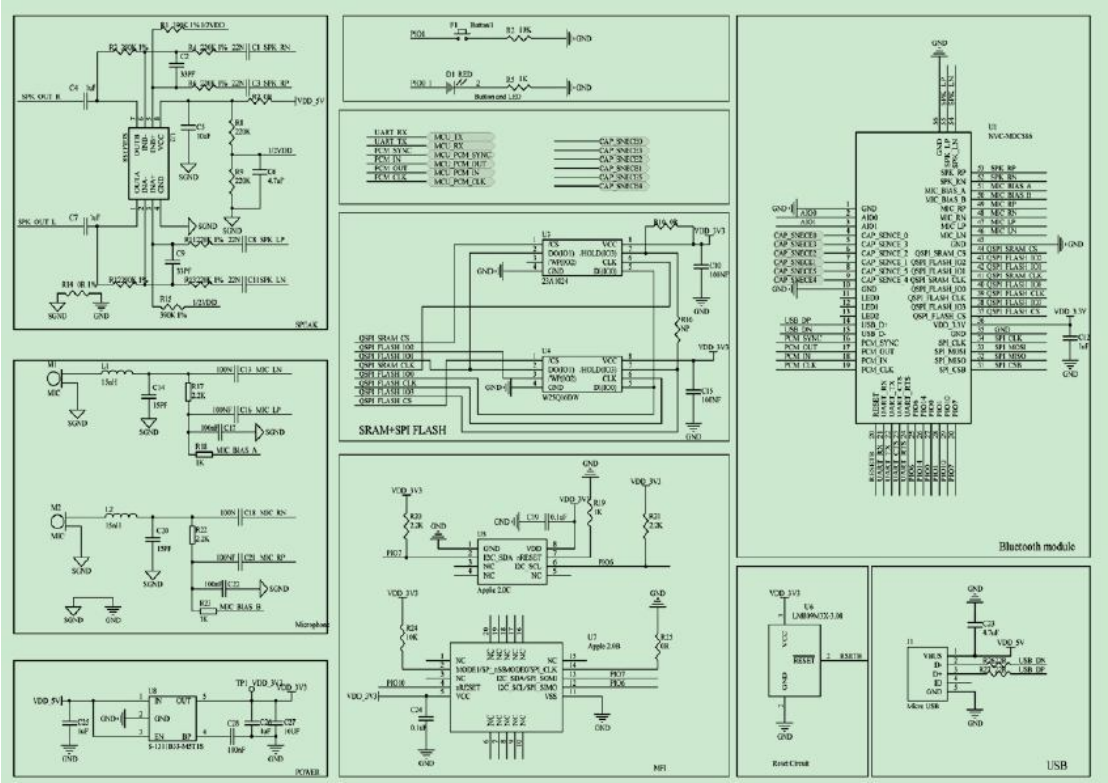

Figure 1: Reference Design

6. MECHANICAL AND PCB FOOTPRINT CHARACTERISTICS

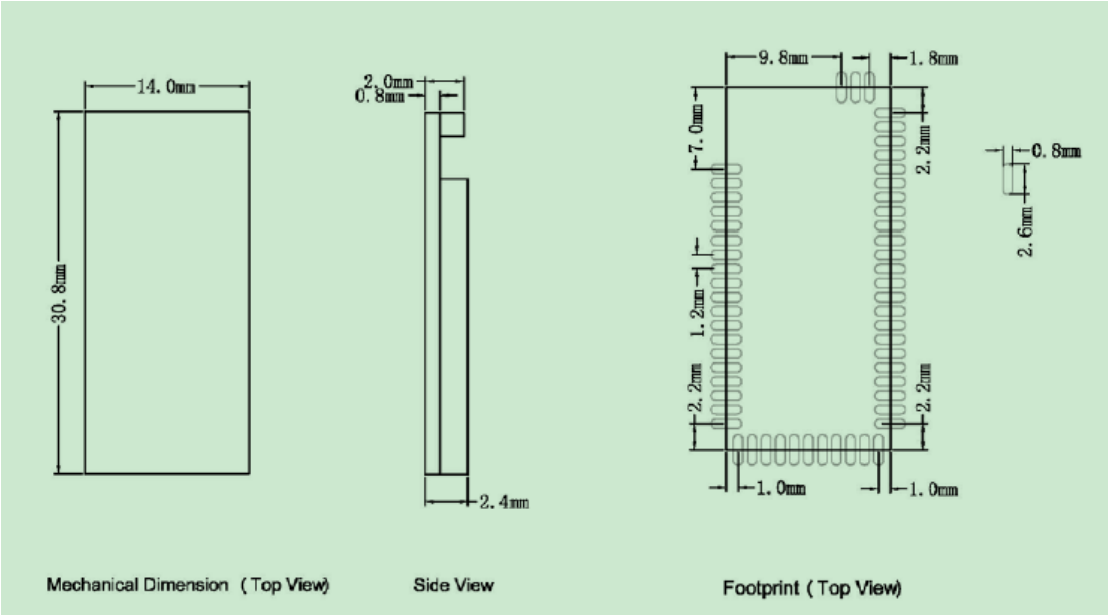

Figure 1: Recommended PCB Mounting Pattern (Unit: mm, Deviation:0.02mm)TOP View

7. RF LAYOUT GUIDELINES

SH-MB18 RF design to ensure enough clearance area of antenna, area length is 1.6 times of antenna length, area width is 4 times of antenna width, the bigger the better if the space allows. Module antenna clearance area size, as follows.

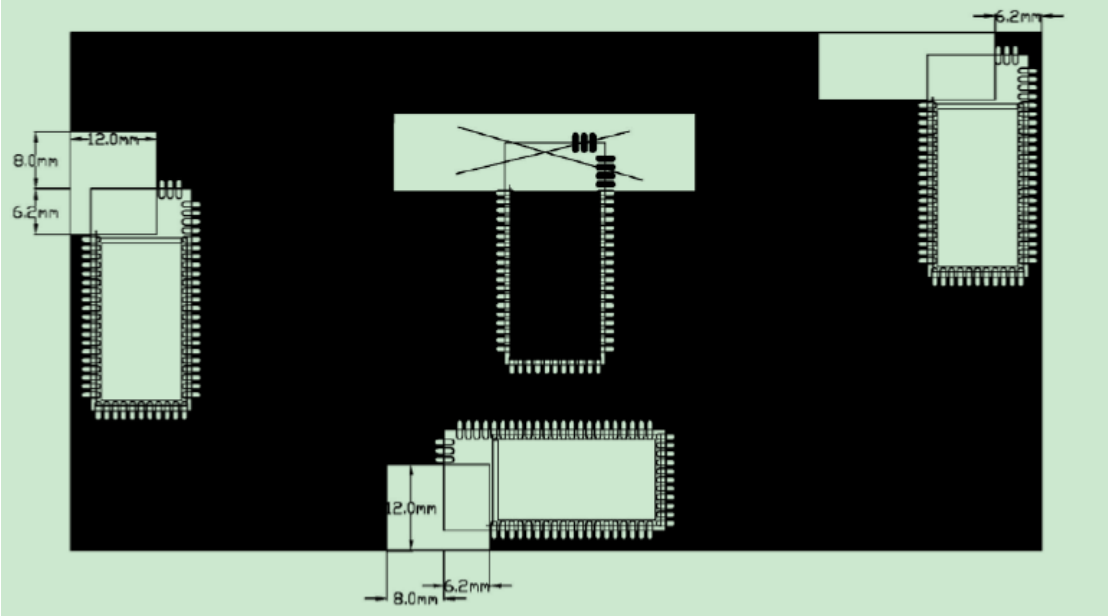

Figure 18: Clearance Area of Antenna