



Interface Protocol Design in Capella

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Agenda

1. Background
2. Interface Design in Capella
3. Extension to Interface Protocol Design
4. Conclusion

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1. Background

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- PGM is short for Pu Gou Moutain, which is a mountain full of treasure, record in “Shan Hai Jing” (Classic of Mountains and Rivers, the earliest annals of geography in China, about 2,500 years ago).
- PGM is a leading provider of MBSE solution and consulting service in China.



Introduction of Speakers



- Renfei Xu is the Technical Director of MBSE from PGM. He has participated in many implementation projects of MBSE in areas like Engine Control, Avionics, Mechatronics, RADAR and so on. In recent years, he is dedicated to the promotion of Capella and ARCADIA in China.

Challenge of Interface Design

- In the development of complex systems, interface design is one of the core tasks. It mainly defines the interface structure, message protocol and cable connection between various equipment/subsystems/devices/modules.
- The traditional way to design interface is based on Interface Control Document (ICD). It is facing more and more challenges.

1. ICD is hard to support collaborative design.

2. ICD data is hard to be quickly reused.

3. ICD has a large amount of data and complex formats, making it difficult to maintain.

4. It's hard to automatically verify the correctness.

5. The granularity of data management is too coarse.

6. Disconnected from the architecture design document.



Example of Traditional ICD

Payload Name	Data Type	Length	Meaning	Unit	Description
Request	char[2]	2	PID	/	—
	uint16	2	CID	/	—
	char[2]	2	SID	/	—
	uint16	2	Length of this payload	byte	—
	uint32	4	Sending time	ms	—
	uint16	2	Counting number	/	—
	uint16	2	Check code	/	—
TimeStamp	char[2]	2	PID	/	—
	uint16	2	CID	/	—
	char[2]	2	SID	/	—
	uint16	2	Length of this payload	byte	—
	uint16	2	Year	/	—
	byte	1	Month	/	—
	byte	1	Day	/	—
	uint32	4	Sending time	ms	—
	uint16	2	Counting number	/	—
	uint16	2	Check code	/	—

- What is the relationship with the architecture definition (in a .vsd file) ?
- Is it the same in the document of the source module and target module?
- Who has the authority to modify it?
- ...

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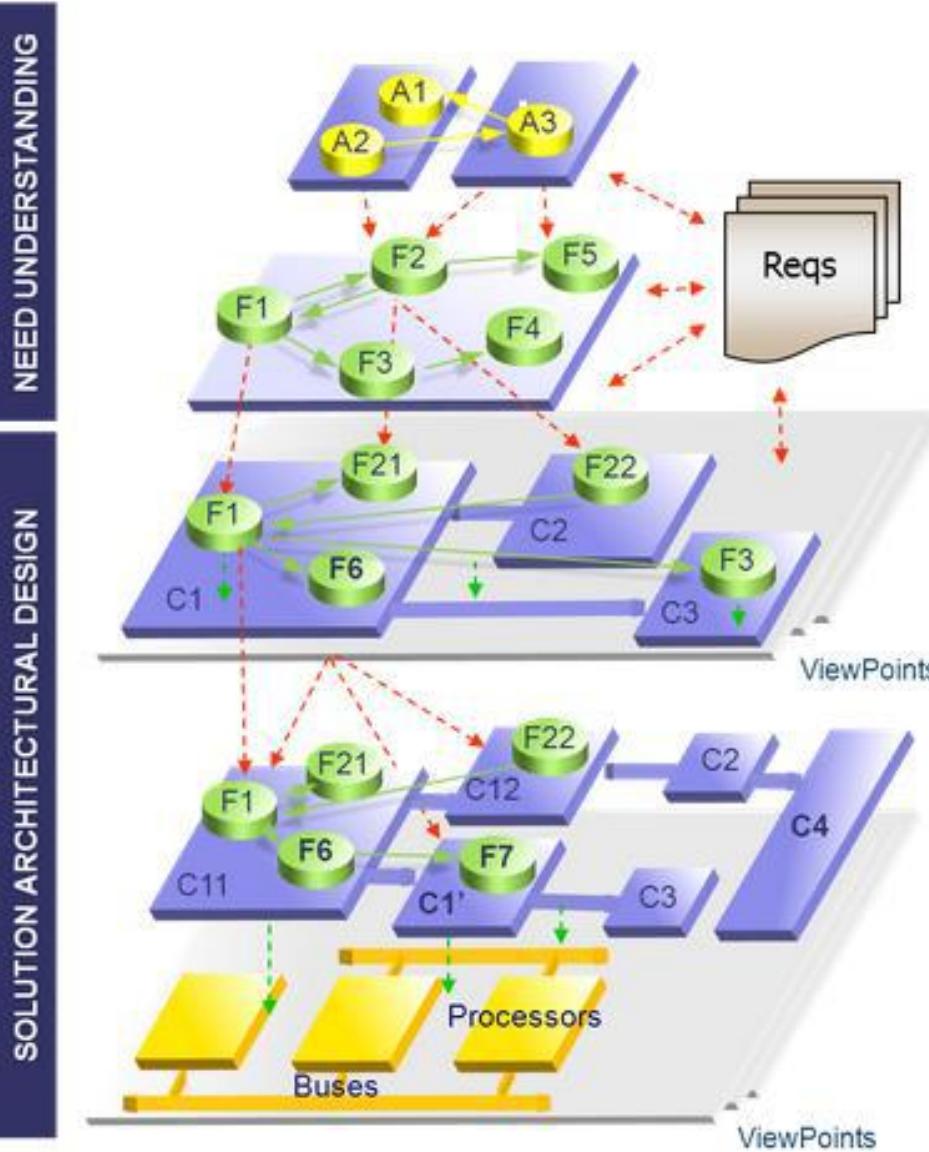
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A Global View of ARCADIA/Capella



What the users of the system need to accomplish

What the system has to accomplish for the users

How the system will work to fulfill expectations

How the system will be developed and built

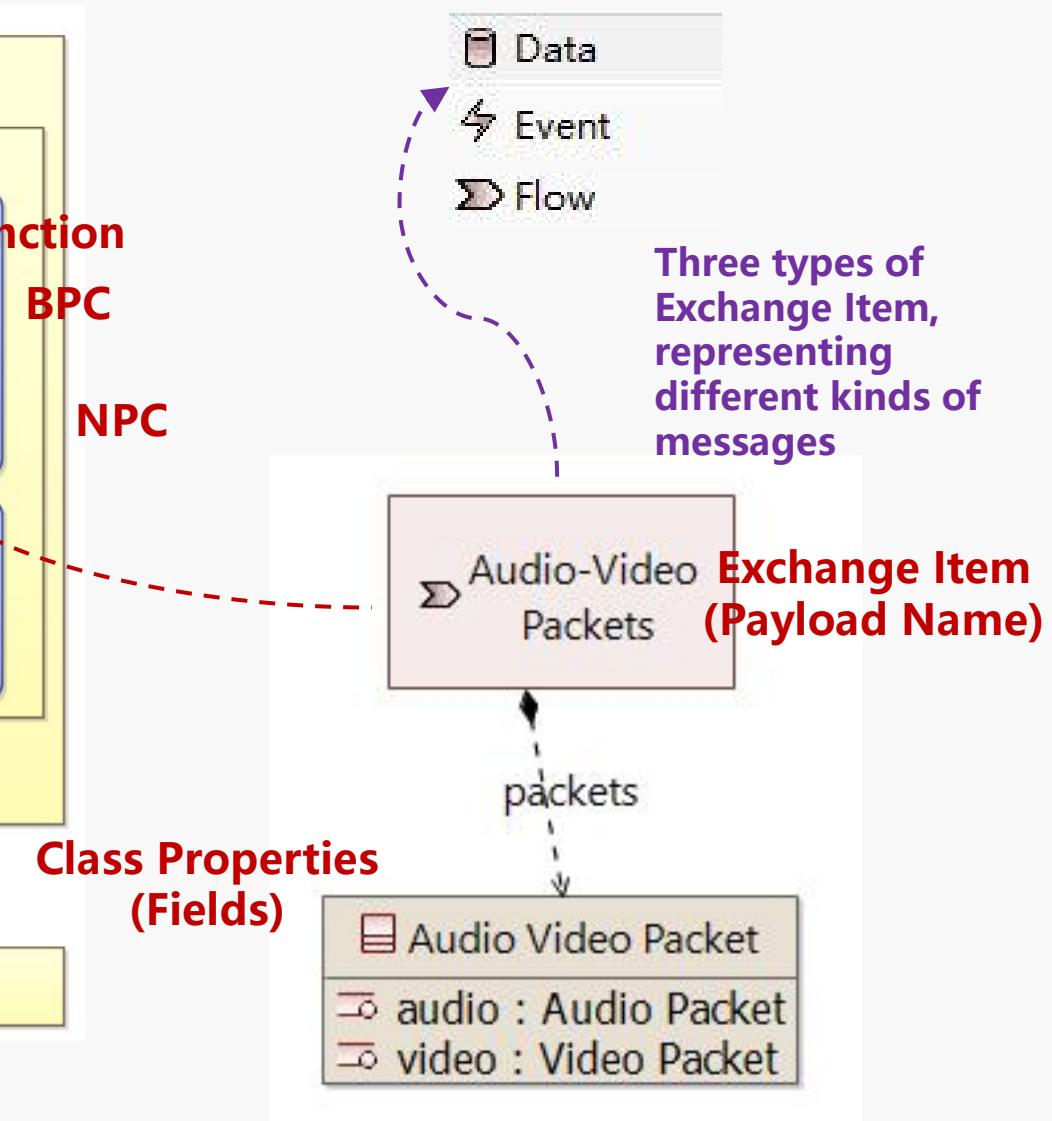
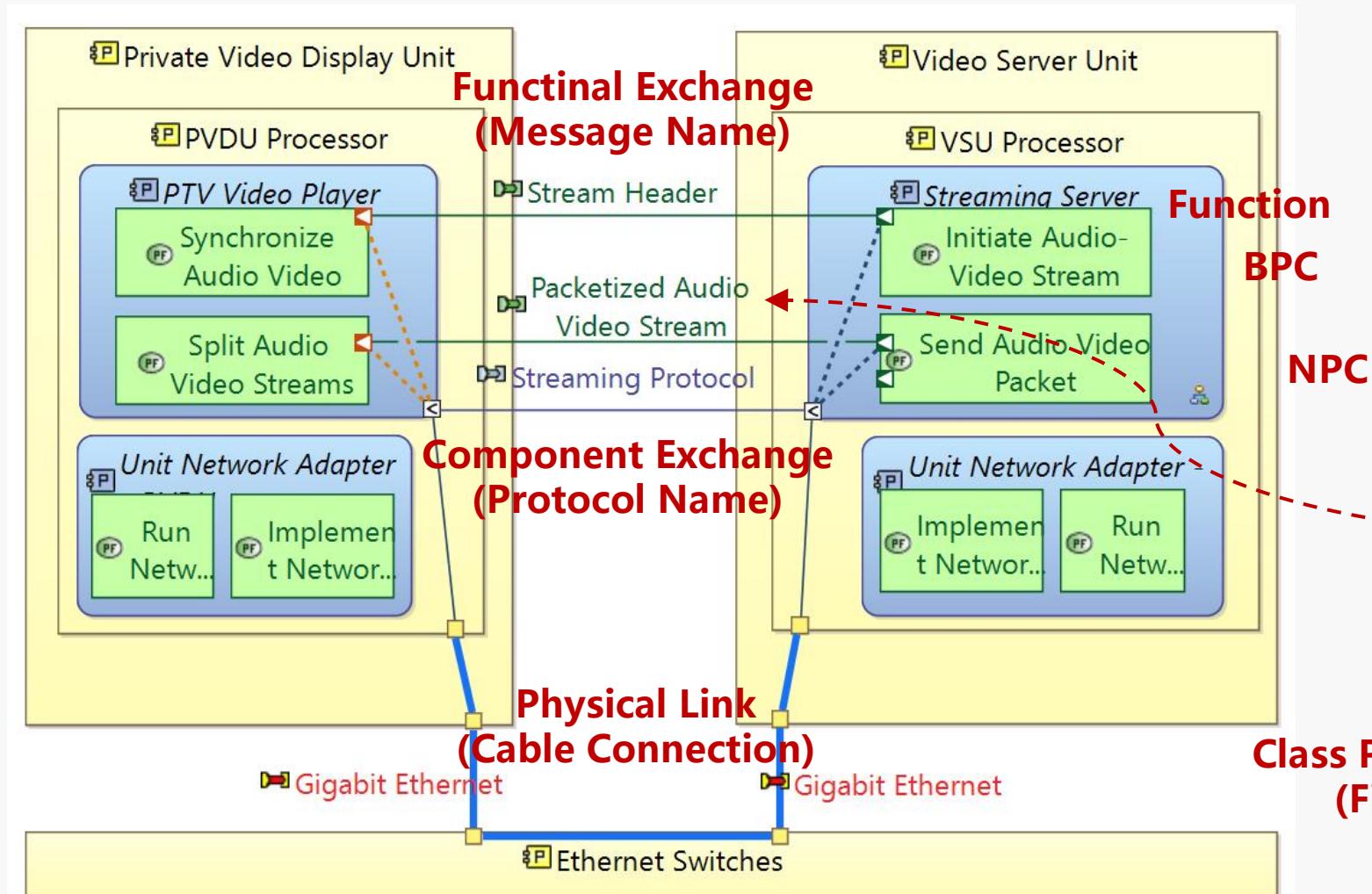
- **Operational Analysis**

- **System Analysis**

- **Logical Architecture Design**

- **Physical Architecture Design**

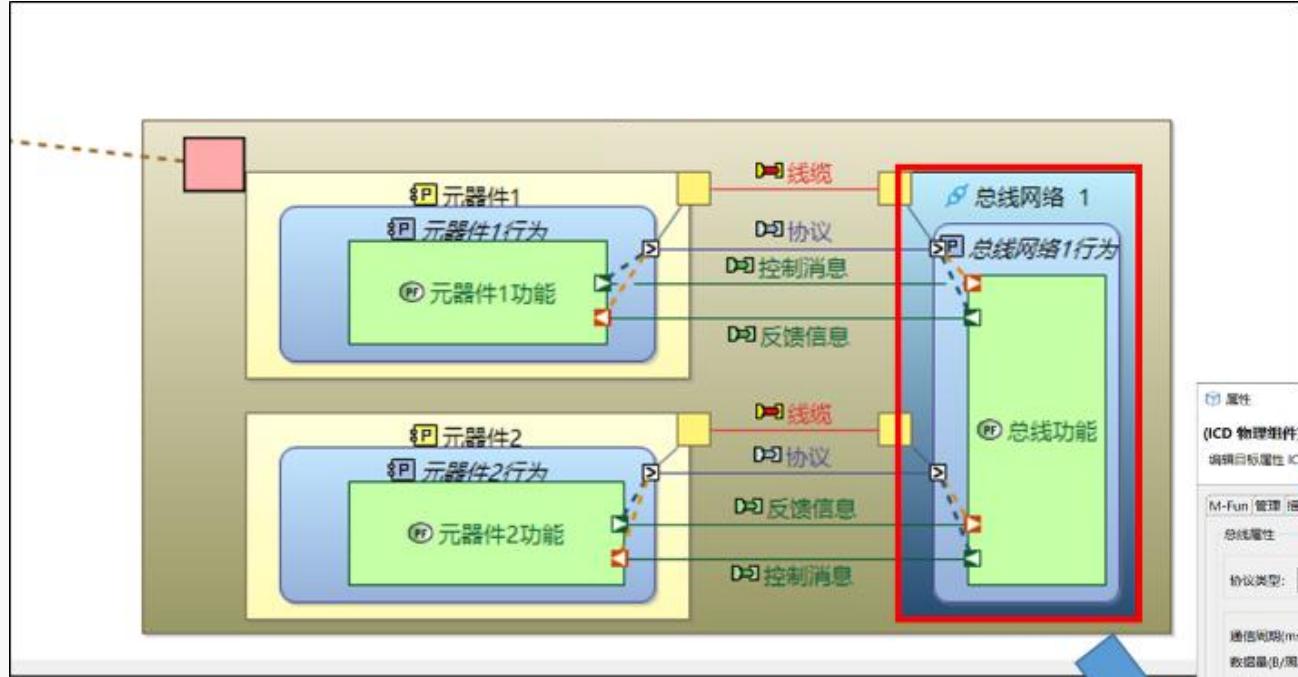
Interface Design In Capella (Example of PA)



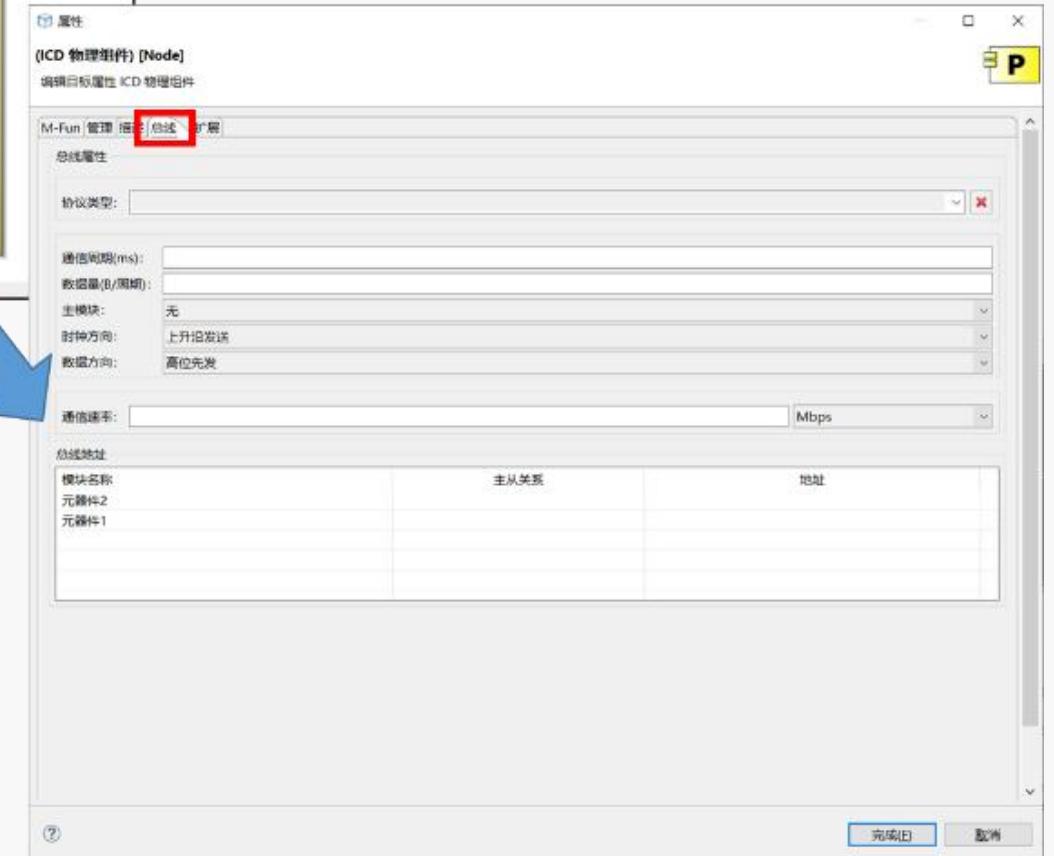
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Bus Structure Definition

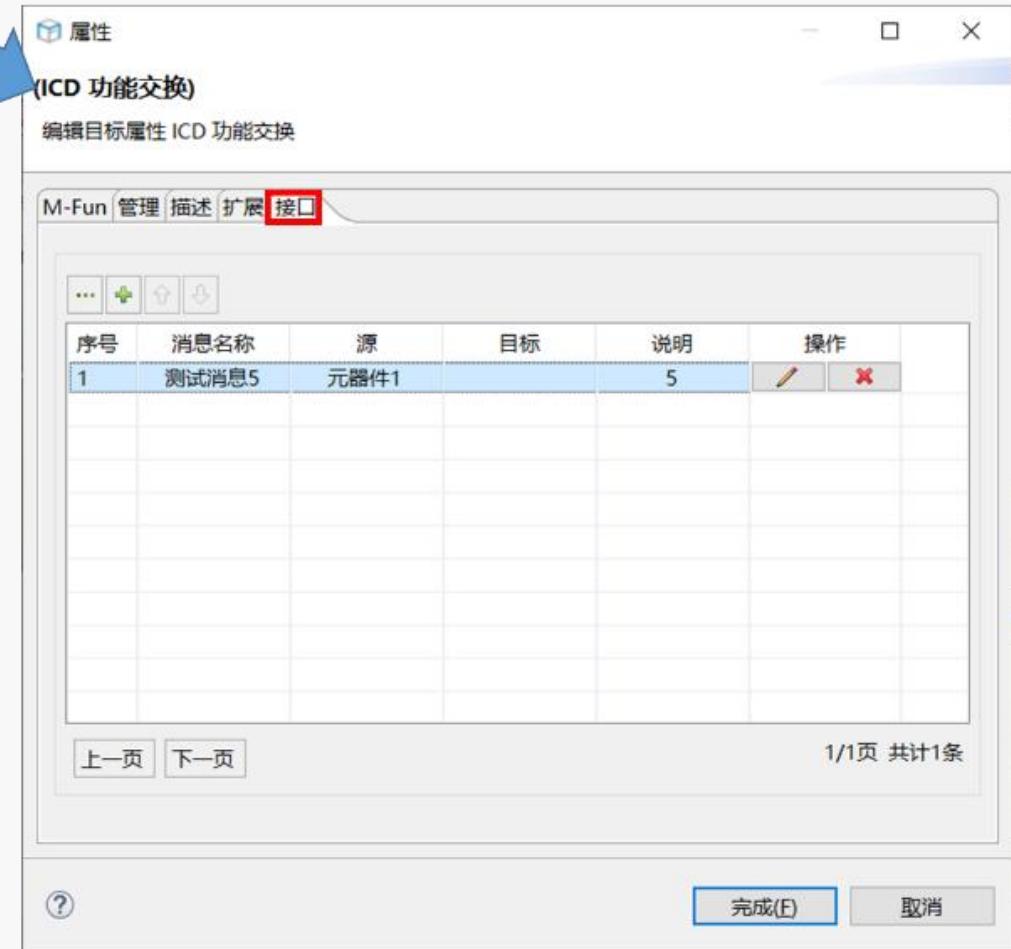
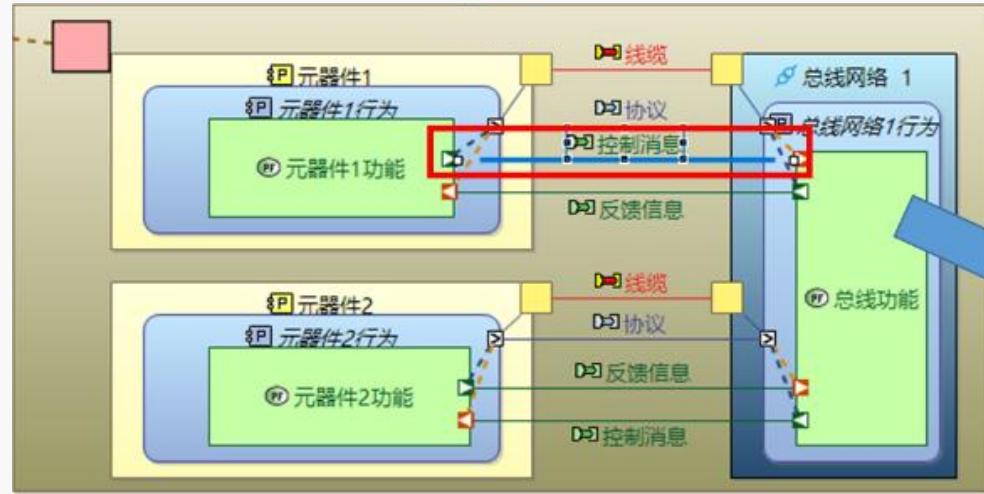


Bus type can be like 1553B, CAN, HDLC and so on.



We have developed a model element called “Bus Network”. Users can define bus type, basic properties, roles and addresses of each module by it.

Message Design (1/3)



For each functional exchange, users can define its relevant messages.

Message Design (2/3)

For each message, users can define its basic properties and inside structure, including its header, body and trailer. If the message body has more than one payload, users can also define the name, length, content and description of these payload.



Message Design (3/3)



All messages can be defined and managed on a server, which can be referenced from Capella model, for quick reuse and standardization.

This is a detailed view of the '新增消息' (Add Message) dialog box. It contains fields for defining a new message, including:

- 消息名称 (Message Name): '请输入消息名称' (Enter message name)
- 源 (Source): '请输入源' (Enter source)
- 目标 (Target): '请输入目标' (Enter target)
- 协议类型 (Protocol Type): '请输入协议类型' (Enter protocol type)
- 通信周期(ms) (Communication Cycle): '请输入通信周期' (Enter communication cycle)
- 数据量(B/周期) (Data Volume): '请输入数据量' (Enter data volume)
- 说明 (Description): '请输入说明' (Enter description)
- 是否可用 (Available): Radio buttons for '可用' (Available) and '不可用' (Not available), with '可用' selected.

At the bottom of the dialog are '提交' (Submit) and '重置' (Reset) buttons.

Payload Design (1/2)

修改消息

* 消息名称 新建消息1 * 协议类型 协议名称2

源 元器件1 通信周期(ms) 1

目标 元器件2 数据量(B/周期) 1

说明 1

信号

序...	名称	长度 (Byte)	内容	说明	操作
1	帧头	1	1		
2	地址	2	22		
3	控制字	3	3		
4	数据段	128	xx	说明内容	
5					

完成(E) 取消 上传至消息库

For each payload in a message, users can define its basic properties and the meaning of each bit or byte.

新增信号

名称 数据段 代号 Data

长度 128 数据单位 bit

内容 xx

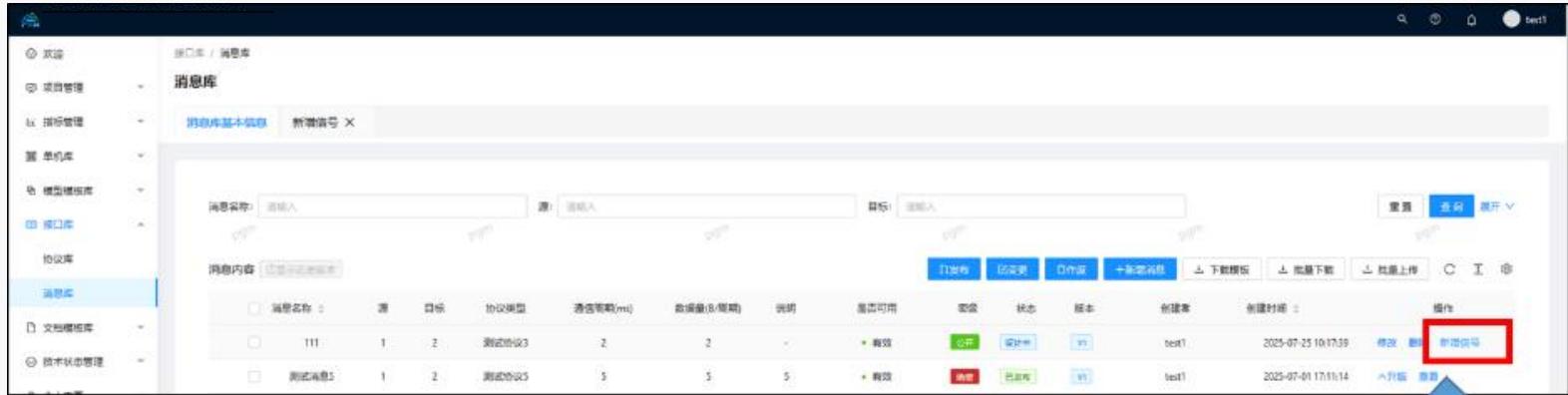
说明 说明内容

数位信息

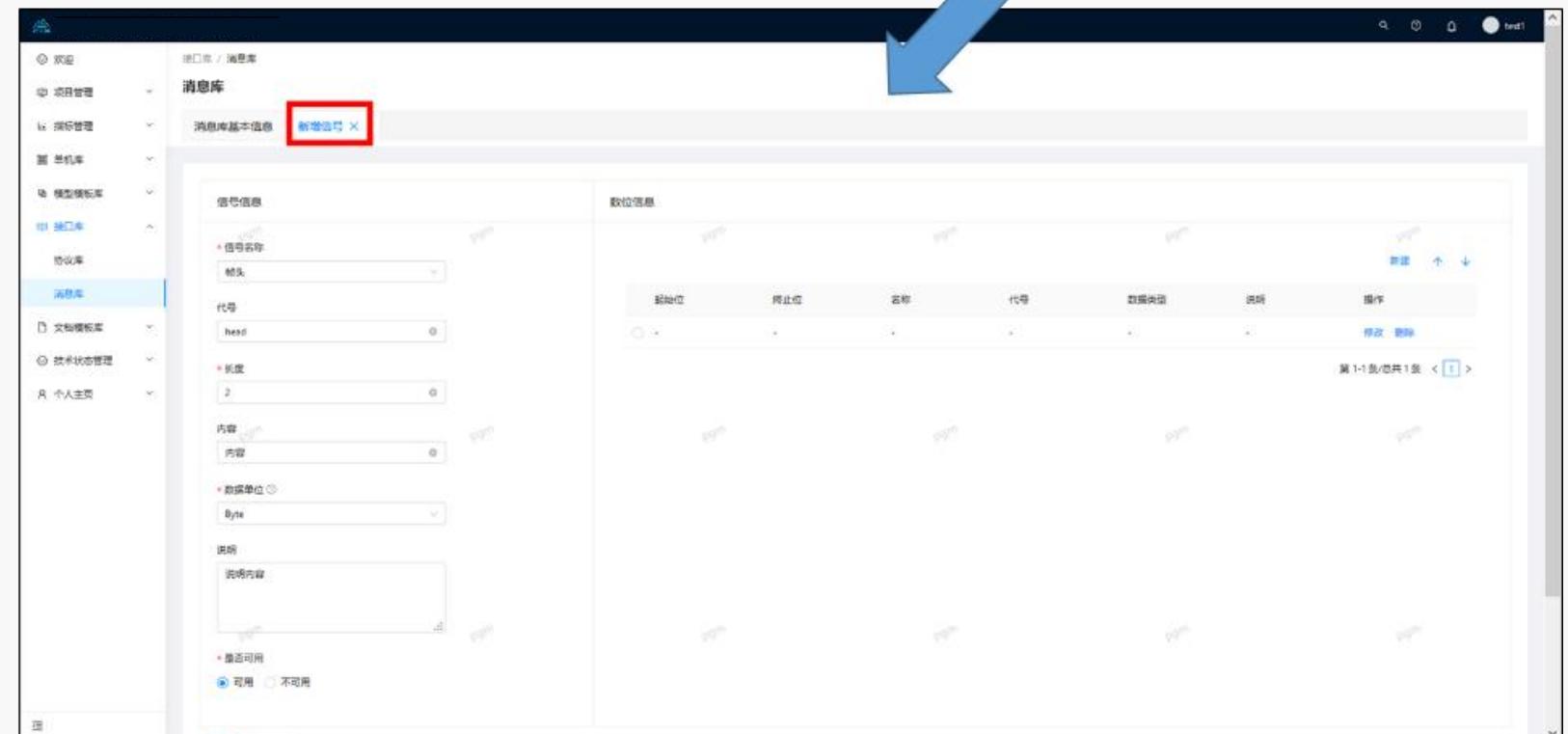
起始位	终止位	名称	代号	数据类型	说明
0	63	数据1	data1	int	
64	127	数据2	data2	int	

完成(E) 取消

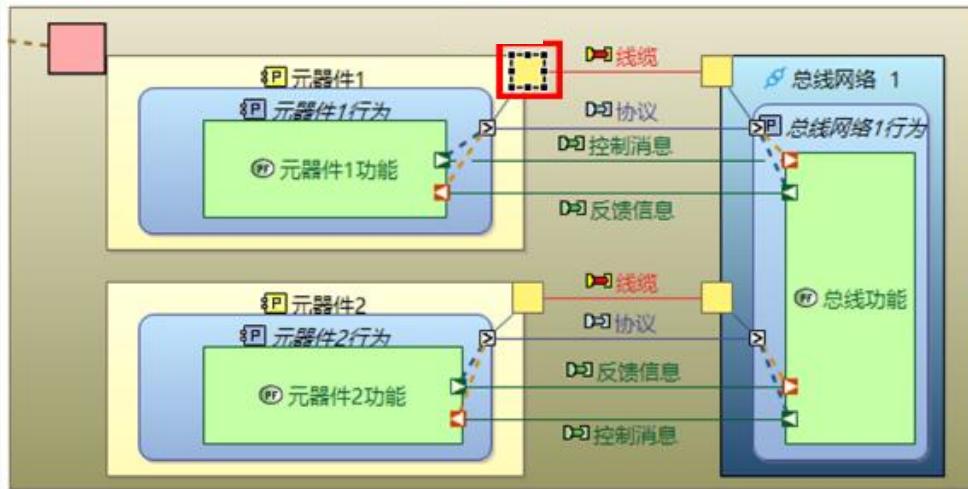
Payload Design (2/2)



All payloads can also be defined and managed on a server, which can also be referenced from Capella model, for quick reuse and standardization.



Preliminary Cable Design (1/6)



This screenshot shows a software interface for managing physical ports. The title bar reads '属性 (ICD 物理端口)' (Properties (Physical Port)). The main area displays a table with port details:

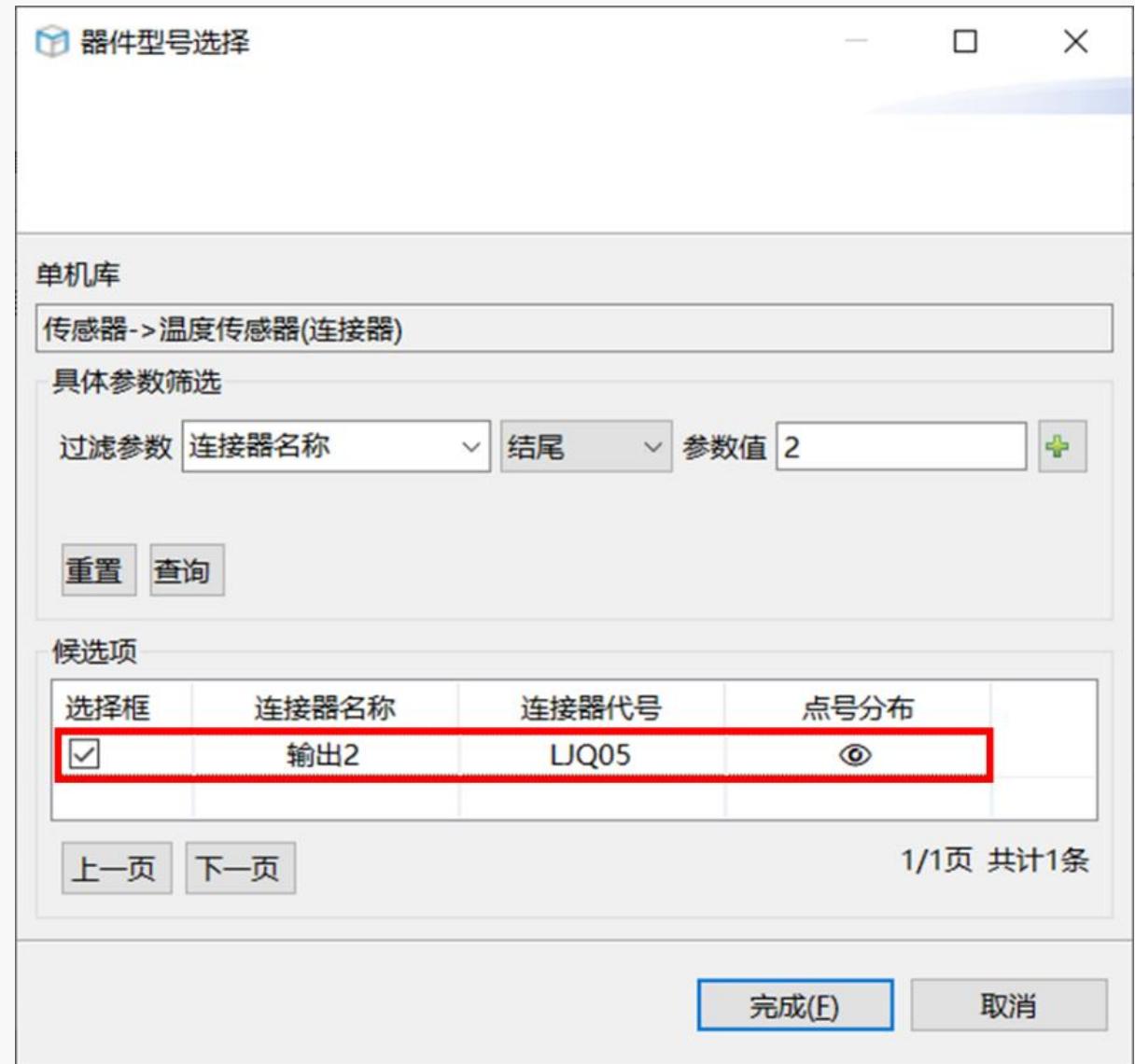
序号	点号	库信号名称	应用信号名称	关联消息	信号类型	说明	删除
1	1	111	-		X
2	2	222	-		X
3	3	333	-		X
4	4	444	-		X

Below the table, there are buttons for '上一页' (Previous Page) and '下一页' (Next Page), and a status bar indicating '1/1页 共计4条' (1/1 page, total 4 items). At the bottom right are '完成(F)' (Finish) and '取消(C)' (Cancel) buttons.

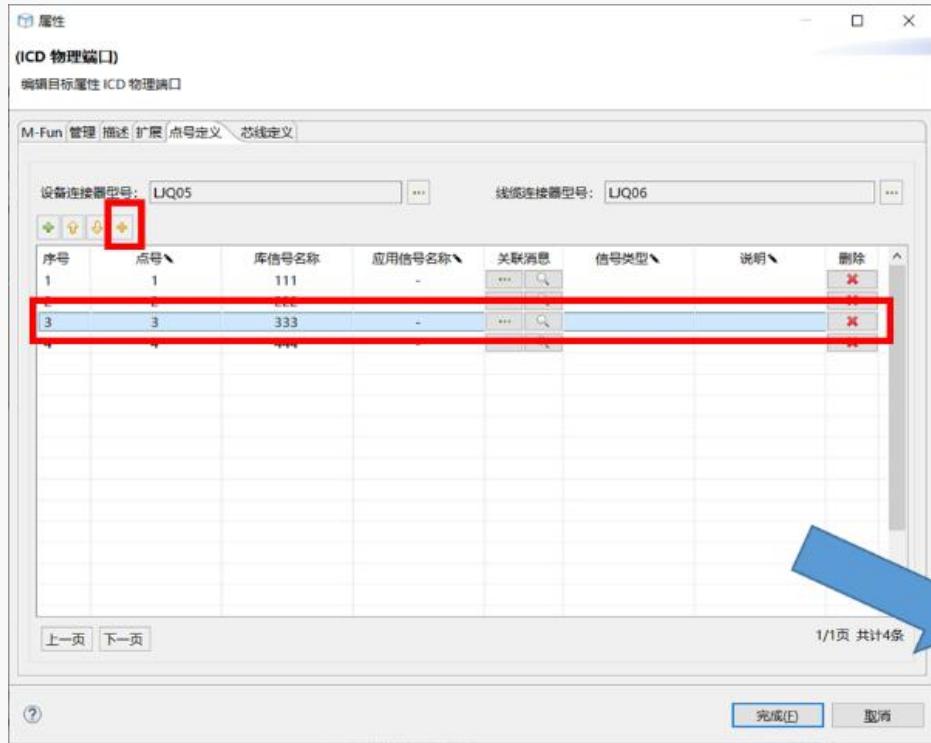
For the physical ports in Capella model, which can represent physical connectors, users can define every pins inside, including pin number, name, type and description.

Preliminary Cable Design (2/6)

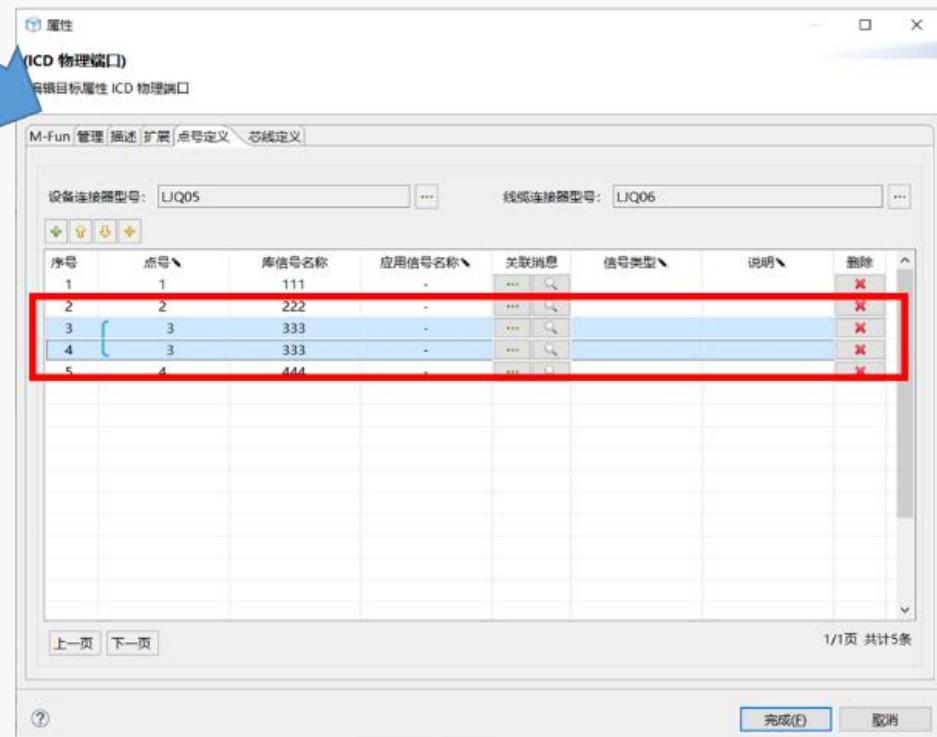
Standard pin information can be predefined in a database. When users choose a standard physical connector from a device library for a physical port, all the predefined pin information will show up.



Preliminary Cable Design (3/6)



If there are differential signals used,
users should define differential pairs
based on physical pins.



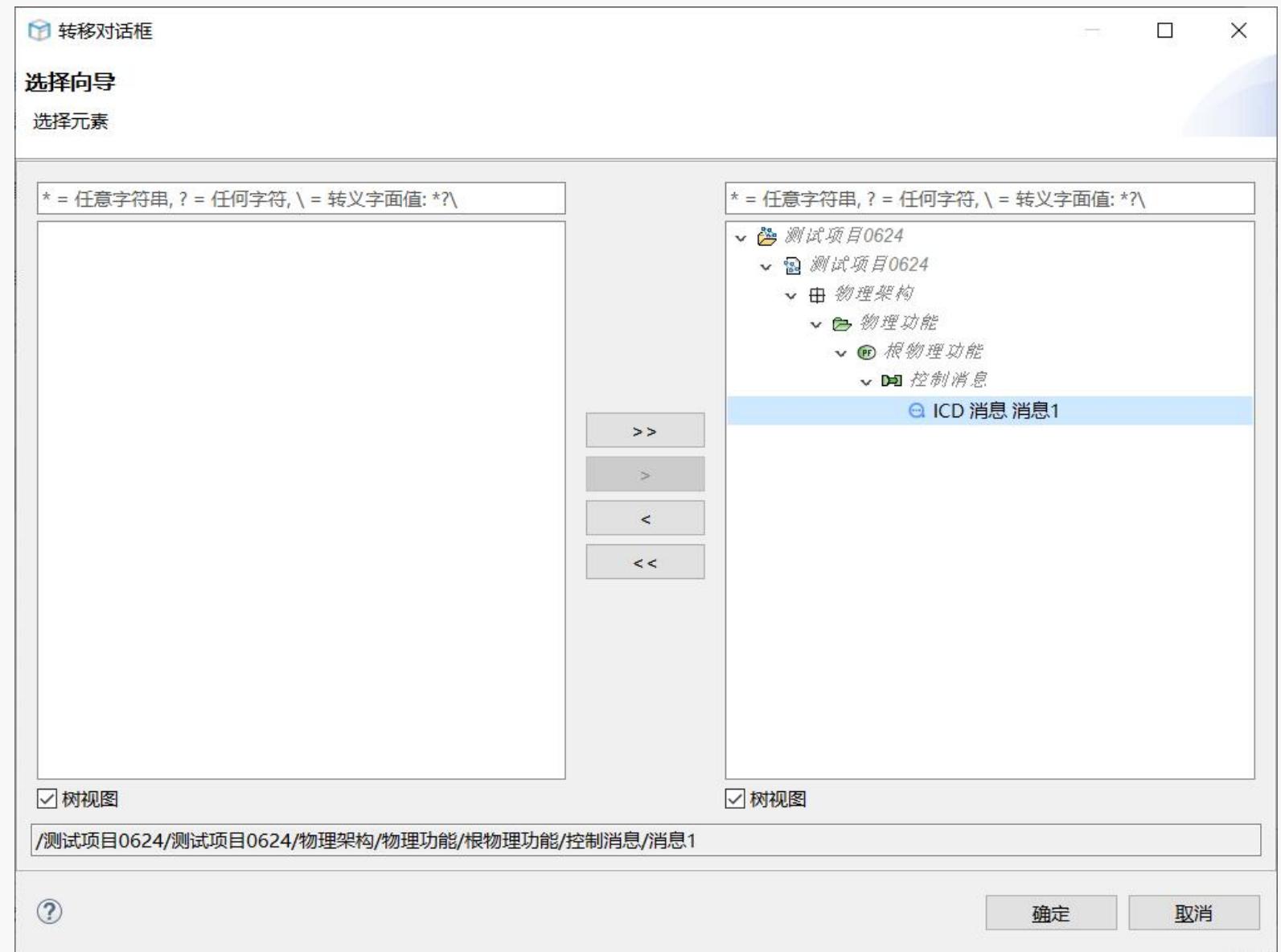
Preliminary Cable Design (4/6)

Cable mapping
can also be
defined based on
physical pins. It
can even be
automatically
done by the
compare of their
names.

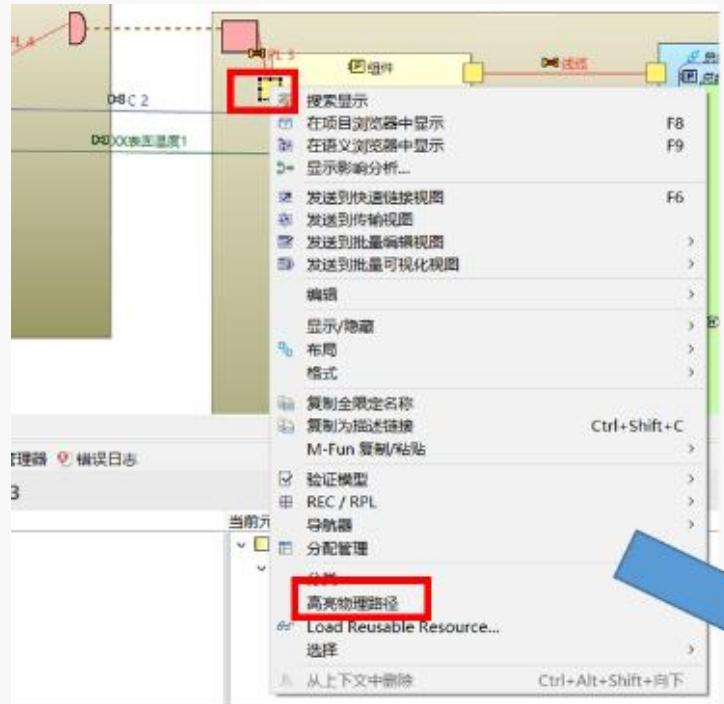
序号	点号	应用信号名称	终端设备名称	终端设备型号	终端线缆连接器名...	终端线缆连接器型号	终端点号	终端应用信号名称	导线截面积	线缆型号	删除
1	2	信号1	组件	TempScensor4	ICDPhysicalPort 3	LJQ05	2	信号1	1	DX01	
2	3	信号2	组件	TempScensor4	ICDPhysicalPort 3	LJQ05	3	信号2	1	DX01	

Preliminary Cable Design (5/6)

Each physical pin or differential pair can be linked to one or more messages (with the right allocation).



Preliminary Cable Design (6/6)

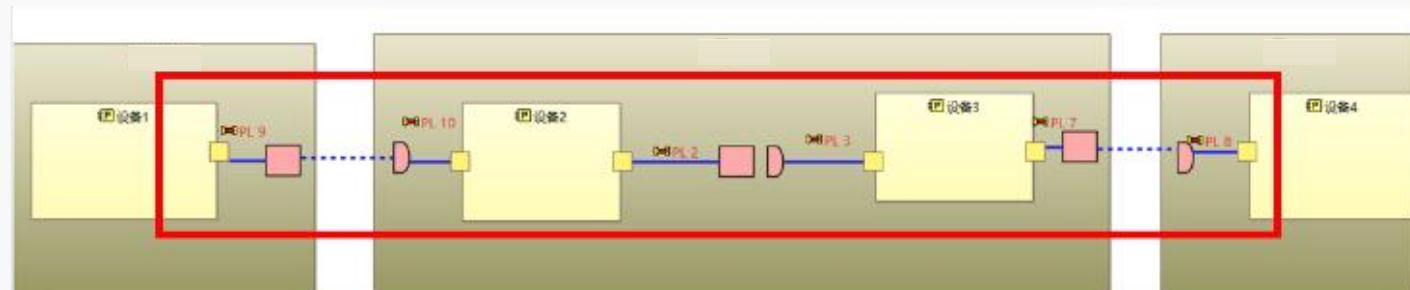


If your model is defined completely, then you can highlight the entire message transmission path within your physical architecture model.

高亮物理路径

— 高亮: 正确
— 高亮: 某一端芯线匹配错误

序...	点号	库信号名称	应用信号...	信号类型	描述	物理路径
1	1	111	-	非电量	11	高亮
2	2	222	信号1	非电量	11	取消高亮
3	3	333	信号2	非电量	22	高亮
4	4	444	-	非电量	22	高亮



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Benefits

Integrated Design Process

Design interface protocol within the architecture model directly



Verification of Correctness

Use pre-defined rules and message path highlight to check the result

Effective Data Control

Control interface data along with architecture model

Easier Collaboration

Collaborate based on structured and fine-grained model

Standardized Design

Use standard process, method and template to design interface

Efficient Data Reuse

Build database of messages, payloads and devices for quick reuse

Conclusion

Capella is a good platform for architecture design. Engineers can use it to define functional exchange, component exchange, physical link, and relative data structures. But it's not enough for interface protocol design. For those who are still using documents to do interface detailed design, or using several separated tools to design protocol and cables, it will be much easier for them to design interface protocol based on architecture model directly. We have developed an extension on Capella to do bus structure definition, message design, signal design, and preliminary cable design. All these information is tightly connected and is traceable.



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