Name Answers

CE-1921 – Dr. Durant – Quiz 8
Spring 2018, Week 8

1. (2 points) Describe how pipelining improves throughput (rate of instruction completion).
2. (2 points) Justify the Harvard organization in pipelined implementations.

For the pipelined architecture discussed in class…

3. (2 points) Write assembly instructions that generate a control hazard, specifically a conditional branch that is taken. Begin by causing the flags to be set as needed.
4. (4 points) Draw a pipeline in-flight diagram for your sequence of instructions, illustrating key details (e.g., stalling, flushing, and/or forwarding) of how the hazard is resolved.

(1) Relative to an SCP the clock can be run faster since it needs to be long enough for the longest steps (IF, ID, EX, MEM, WB), not the total propagation delay.

(2) Similarly, the instruction in MEM may access DMEM while the instruction in IF accesses IMEM. If there is only 1 memory bus, this creates a bottleneck (2 tasks, 1 channel). Having separate busses for IMEM & DMEM eliminates the bottleneck.

(3)
```
movs r0,#1   ← causes Z=0
bne  L1
add  r1,r2,r3
L1: sub  r2,r1,r3
```
You wouldn't really write this since the add never runs. You'd simply movs, sub. But, this demonstrates the hazard.

(4)