MSOE EECS Department – Dr. Durant
CE1921: Wk. 7 Lab Grading Checklist

Name: _____ Section: _____

Item	**Score**
1. fetch: Block diagram for fetch stage (for all CE1921 schematics use comment tool to include title, name and date). Include VHDL for all fetch support components in this section (such as adder, used irom, constantN, reg32 from last week for PC). Document all VHDL files in CE1921. Include general information at top, description of each input and output, description of intended behavior, and how you're solving the problem.	/ 5
2. decode: Block diagram for decode stage and VHDL/BDF for all support components not included earlier	/ 5
3. execute: Block diagram for execute stage and VHDL/BDF for all support components not included earlier	/ 10
5. completed control table	/ 10
6. control: VHDL for single-cycle control.	/ 10
control simulation. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct. Simulate at least about 5 varied instructions, including conditional instructions.	/ 15
4 (note order). toplevel: Block diagram for overall processor.	/ 10
Overall processor simulation	/ 15
Demo : Show professor overall processor simulation in Quartus and answer questions	/ 20
Total	/ 100

- *Staple* this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the ***order*** listed above.
- Your lab packet is due by 10 AM on the day after your lab meets.
- Extra copies of lab checkout sheets are available on my website.