16:4 Priority Encoder from 4:2 Priority Encoders

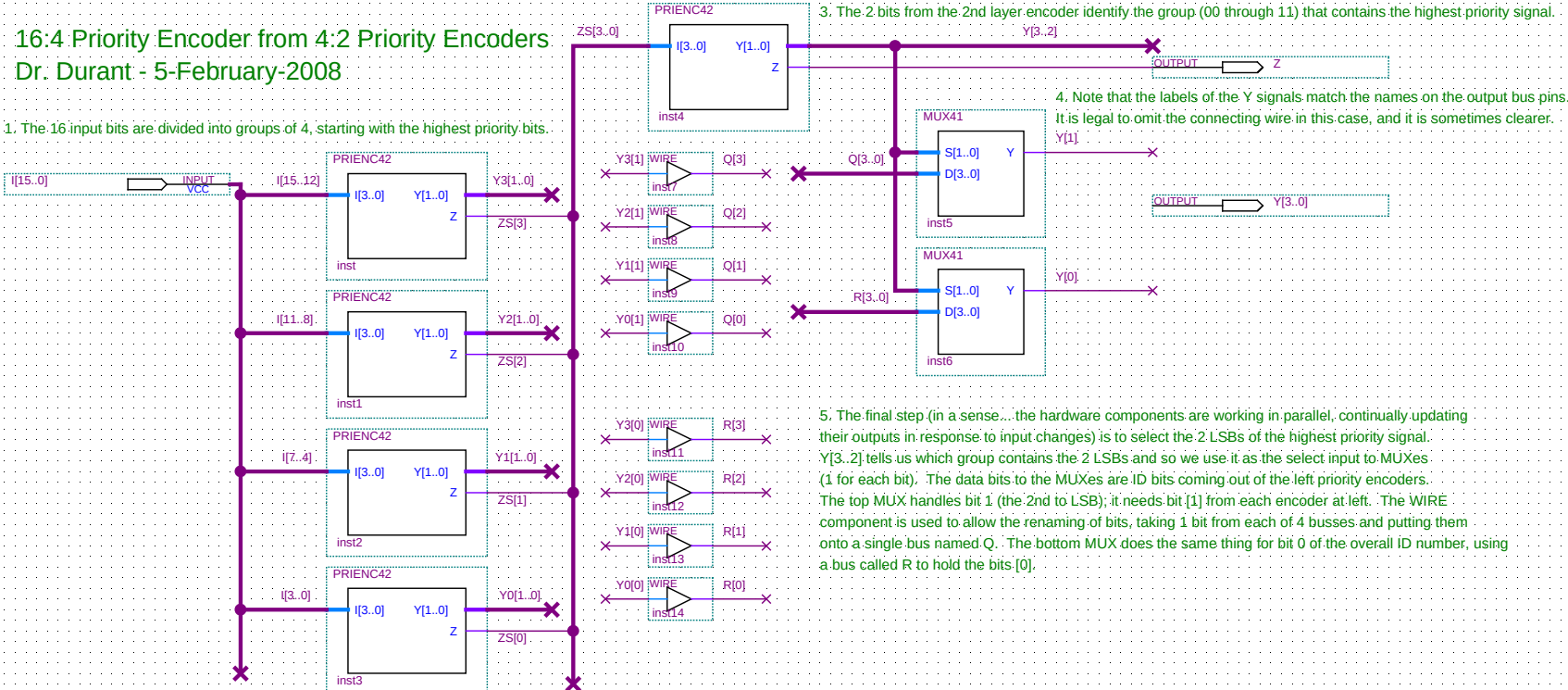
Dr. Durant - 5-February-2008

2. The Z signals from the first 4 priority encoders are passed through another priority encoder so we know which group of 4 contains the highest priority active signal.

3. The 2 bits from the 2nd layer encoder identify the group (00 through 11) that contains the highest priority signal.

4. Note that the labels of the Y signals match the names on the output bus pins. It is legal to omit the connecting wire in this case, and it is sometimes clearer.

1. The 16 input bits are divided into groups of 4, starting with the highest priority bits.



5. The final step (in a sense... the hardware components are working in parallel, continually updating their outputs in response to input changes) is to select the 2 LSBs of the highest priority signal. Y[3..2] tells us which group contains the 2 LSBs and so we use it as the select input to MUXes (1 for each bit). The data bits to the MUXes are ID bits coming out of the left priority encoders. The top MUX handles bit 1 (the 2nd to LSB), it needs bit [1] from each encoder at left. The WIRE component is used to allow the renaming of bits, taking 1 bit from each of 4 busses and putting them onto a single bus named Q. The bottom MUX does the same thing for bit 0 of the overall ID number, using a bus called R to hold the bits [0].