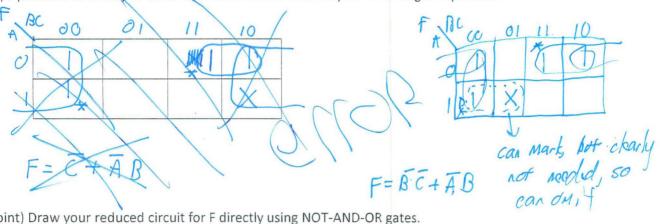
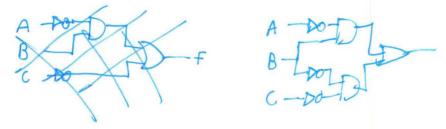
Name	answers

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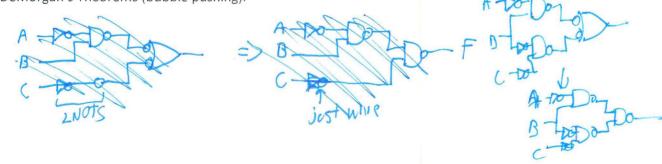
1.5 1. (χ points) Let F(ABC) = $\Sigma_m(0,24) + d(\chi,\chi)$ (d indicates don't care conditions). Derive the simplest SOP expression for F using a K-map. Reminders: adjacent terms in a K-map may differ in the value of only 1 bit. Start with m₀ in the upper left corner, putting m₁ to the right and m₄ below it. Form largest groups possible. It is okay to cover terms more than once as your form larger implicants.



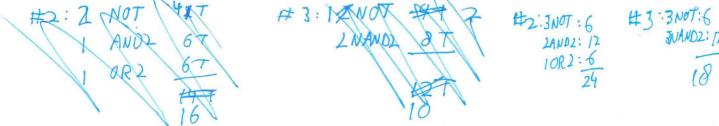
2. (1 point) Draw your reduced circuit for F directly using NOT-AND-OR gates.



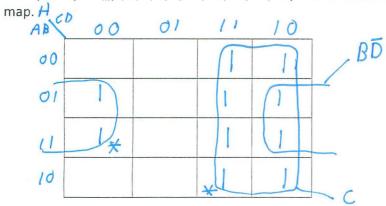
3. (X points) Re-draw it using just NAND and NOT gates based on the most simplified SOP form. Reminders: The first step is to put 2 NOT gates on every input to the OR gate. After that, apply DeMorgan's Theorems (bubble pushing).



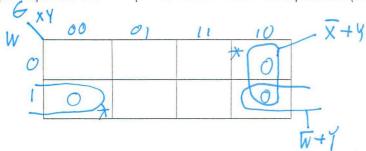
4. (1 point) Calculate the number of transistors needed for each reduced implementation above.



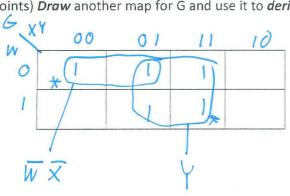
5. Let $H(ABCD) = \Sigma_m(2, 3, 4, 6, 7, 10, 11, 12, 14, 15)$. Derive the simplest SOP expression for H using a K-



6. (2 points) **Draw** the K-map that results in the POS equation G(WXY) = (W'+Y)(X'+Y).



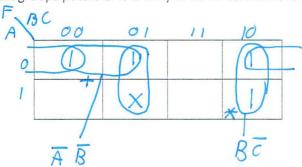
1.5 7. (2 points) *Draw* another map for G and use it to *derive* the simplest SOP expression for G.



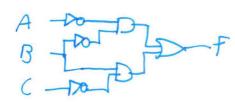
Note: this is also an application of the distributive theorem.

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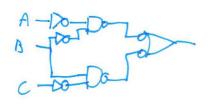
1. (1.5 points) Let $F(ABC) = \Sigma_m(0,1,2,6) + d(5)$ (d indicates don't care conditions). Derive the simplest SOP expression for F using a K-map. **Reminders**: adjacent terms in a K-map may differ in the value of only 1 bit. Start with m_0 in the upper left corner, putting m_1 to the right and m_4 below it. Form largest groups possible. It is okay to cover terms more than once as your form larger implicants.

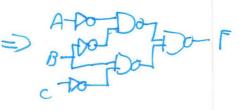


2. (1 point) Draw your reduced circuit for F directly using NOT-AND-OR gates.

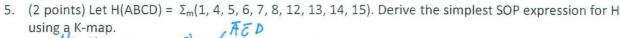


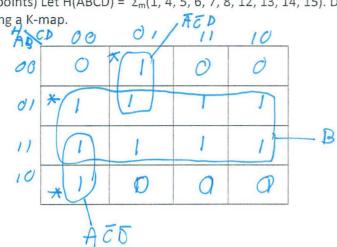
3. (1 point) Re-draw it using just NAND and NOT gates based on the most simplified SOP form. **Reminders:** The first step is to put 2 NOT gates on every input to the OR gate. After that, apply DeMorgan's Theorems (bubble pushing).





4. (1 point) Calculate the number of transistors needed for each reduced implementation above.



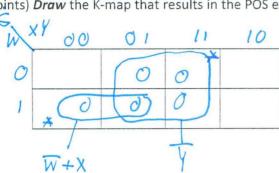


$$F = B + \overline{ACD} + AC\overline{D} = ANSWER$$

$$= B + \overline{C}(\overline{AD} + A\overline{D}) \qquad No \log C$$

$$= B + \overline{C}(A \oplus D) \in SOP$$

6. (2 points) *Draw* the K-map that results in the POS equation G(WXY) = (Y')(W'+X).



7. (1.5 points) *Draw* another map for G and use it to *derive* the simplest SOP expression for G.

