MSOE EECS Department – Dr. Durant
CE1921: Wk. 5 Lab Grading Checklist

Name: _____ Section: _____

Item	**Score**
1. reg32: VHDL for 32-bit register, asynch. reset, sync. load. Document all VHDL files in CE1921. Include general information at top, description of each input and output, description of intended behavior, and how you're solving the problem. Example: https://faculty-web.msoe.edu/durant/courses/ce1901/muxex.vhd)	/ 10
reg32 simulation. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct.	/ 5
2. VHDL for busmux16to1, optionally generic width (default 32)	/ 5
busmux16to1 simulation	/ 5
3. VHDL for decode4to16 with enable. Output may be bus.	/ 5
decode4to16 simulation	/ 5
4. Structural VHDL or schematic for regfile, 2 read ports, 1 write port. Asynch. reset. Optional: generic register width (default 32). Optional (extra challenge): generic register count (hint: let generic parameter be exponent of 2, default to 4 for 16 registers).	/ 10
regfile simulation	/ 10
5. alu (0 add, 1 sub, 2 and, 3 or, 4 xor, 5 a, 6 b, 7 1). NZ implemented. CV may just output 0.	/ 10
alu simulation: all operations, non-trivial inputs	/ 5
6. VHDL for extimm (0: 8-bit unsigned, 1: 12-bit unsigned, 2: 24-bit signed b format)	/ 5
extimm simulation	/ 5
Demo : Show professor requested simulation in Quartus and answer questions	/ 20
Total	/ 100

- *Staple* this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the ***order*** listed above.
- Your lab packet is due by 10 AM on the day after your lab meets.
- Extra copies of lab checkout sheets are available on my website.