MSOE EECS Department – Dr. Durant
CE1921: Wk. 9 Lab Grading Checklist

Name: _____ Section: _____

Item	**Score**
Address decoder. BDF (or structural VHDL) and RTL. Documented.	/ 10
Top level. BDF (or VHDL) and RTL. Documented.	/ 10
Synchronizer. BDF (or VHDL) and RTL. Documented.	/ 5
LED and SEG7 output blocks. BDF (or VHDL) and RTL. Documented.	/ 10
Test program used, VHDL. (Given program and/or your own)	/ 5
Simulations for all completed programs. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently (e.g., key PC values, key intermediate results on WD bus) to convince a reader your results are correct.	/ 20
Optional Appendix: Additional VHDL and schematics as needed to understand your work. Do not include simple, standard components like registers and bus multiplexors.	
Demo: D-level: Partial implementation, simulates at least partially but not necessarily correctly	/ 10
Demo: C-level: Full implementation, simulation is not necessarily complete	/ 10
Demo: B-level: Correct simulation of given test program	/ 10
Demo: A-level: Works on DE10-Lite	/ 10
Total	/ 100

- *Staple* this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the ***order*** listed above.
- Your lab packet is due by 10 AM on the day after your lab meets.
- Extra copies of lab checkout sheets are available on my website.