Name Answers

CE-1921-11 – Dr. Durant – Quiz 7
Spring 2017, Week 7

1. (3 points) Describe the hardware size tradeoff of a multi-cycle processor compared with a single-cycle processor. (Which is smaller? At what cost does the compactness come?)
2. (2 points) Why does a multi-cycle processor need both an instruction register and a data register?
3. (2 points) Review the book's state diagram (on back). Explain why ALUSrcA is 1 for both S0 and S1.
4. (3 points) For the multi-cycle processor designed with the given state diagram, neglecting the speedup of conditional instructions, calculate the average CPI for a program that consists of 80% data processing instructions, 10% load instructions, 5% store instructions, and 5% branch instructions. Show your work.

(1)

MCP	SCP
- small size	- larger
- re-use components (memory, ALUs)	- separate ALU & PC+4/Bdst.
- slow (generally)	- Harvard arch.
- complex design/control	- faster

(-½ if speed not mentioned)
(-½ if size dec.)

(2) Memory is re-used. Need to ensure read values remain available later in instruction

(3) ALUSrcA = 1 indicates PC. Calculate PC+4 & (PC+4)+4 = = PC+8 in these states.

(4)

Type	Share	CPI	Weighted CPI
DP	80%	4	3.2
LDR	10%	5	.5
STR	5%	4	.2
B	5%	3	.15
	100%		4.05

Name Answers

CE-1921-21 – Dr. Durant – Quiz 7
Spring 2017, Week 7

1. (3 points) Describe the hardware size tradeoff of a multi-cycle processor compared with a single-cycle processor. (Which is smaller? At what cost does the compactness come?)
2. (2 points) Give an example of a non-architectural register in the multi-cycle processor and explain why it is classified this way.
3. (2 points) Review the book's state diagram (on back). Explain why RegW is active for only S4 and S8.
4. (3 points) For the multi-cycle processor with the given state diagram, neglecting the speedup of conditional instructions, calculate the average CPI for a program that consists of 60% data processing instructions, 20% load instructions, 10% store instructions, and 10% branch instructions. Show your work.

(1)

MCP	SCP
- small size	- larger
- re-use components (memory, ALUs)	- separate ALU + PC+4/8 adder.
- slow (generally)	- Harvard arch.
- complex design/control	- faster

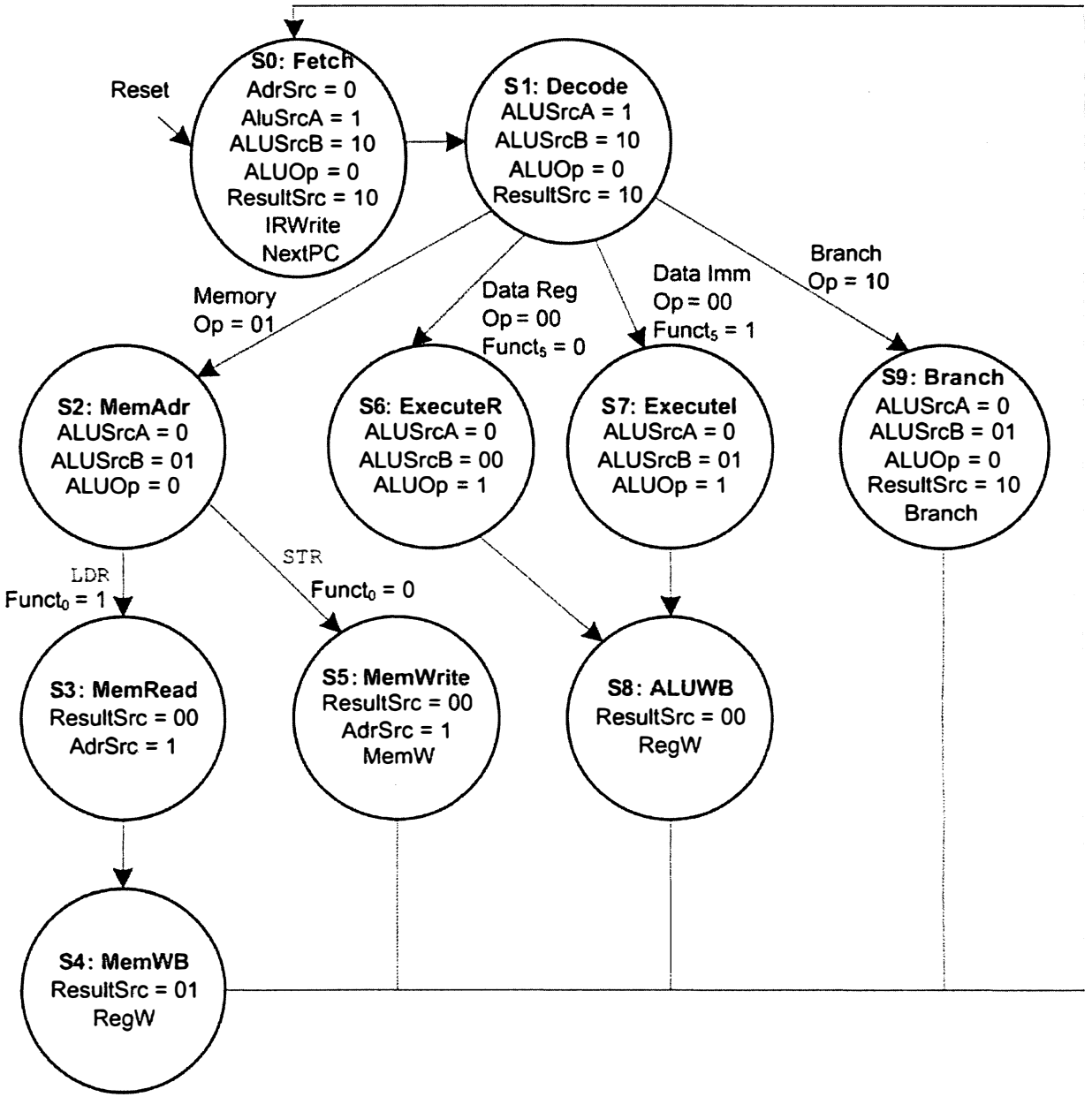
(2) The data register, which holds the LDR memory value, is a non-arch. reg.

Non arch. regs./data are not required by the architecture, but result from microarchitectural implementation decisions.

(3) because data processing instructions + LDR are the only instructions that write to a destination reg. (This ignores TST + other S-type instructions, which have RegW=0.)

(4)

Type	Share	CPI	Weighted CPI
DP	60%	4	2.4
LDR	20%	5	1
STR	10%	4	.4
B	10%	3	.3
	100%		4.1



State	Datapath μOp
Fetch	Instr ← Mem[PC]; PC ← PC+4
Decode	ALUOut ← PC +4
MemAdr	ALUOut ← Rn + Imm
MemRead	Data ← Mem[ALUOut]
MemWB	Rd ← Data
MemWrite	Mem[ALUOut] ← Rd
ExecuteR	ALUOut ← Rn op Rm
ExecuteI	ALUOut ← Rn op Imm
ALUWB	Rd ← ALUOut
Branch	PC ← R15 + offset

5.

6. Figure 7.41: Complete multicycle control FSM