EE 393 **LAB 2**

Design one input of a CMOS inverter chip 74CT04 without protection circuit. Requirement for this device is as follows:
V_{th} = 1.4 V, Output Source and Sinking currents = 2 mA.

Process:

1. Design a CMOS inverter so that V_{th} = 1.4 V ± 10% for input stage
2. Design a CMOS inverter to source and sink 2 mA ± 10% current for the output stage
3. Design an inverter using minimum geometry transistor for the middle stage. L = 2λ, W_n = 4λ. Choose W_p to match current.
4. Combine the circuits given in 1, 2 and 3 to build the one inverter gate for the chip
5. Use microwind 2-7 generate a .msk file for the inverter chip.
6. Extract the stray capacitances and resistances for input, output and the V_{dd} trace. Extract resistance of the ground trace also

   Use AMI T15D process from MOSIS.

   Verify the operation of the circuits using PSPICE simulation

7. Find the maximum frequency of operation of the chip for 2 pF, 10 pF and 50 pF capacitive loads.
8. Add the stray capacitances and resistances in the PSPICE schematic file after the layout and rerun the simulation

Report Requirement:

1. Submit schematics and graphs indicating that design requirement has been met. Display L and W on the schematics for all cases.
2. Show detailed calculations for widths, betas, and all key parameters, similar to the week 2-3 practice problems, for parts 1 and 2. Use Excel or Mathcad, etc. Show how you modified the circuit resulting from your hand calculations to meet the specifications using simulation results.
3. Discuss results.
4. Discuss performance change due to stray capacitances.

Due Week 5