MSOE EECS Department – Dr. Durant
CE1921: Wk. 3 Lab Grading Checklist

Name: _____

Item	**Score**
extender VHDL (0: 8-bit unsigned, 1: 12-bit unsigned, 2: 24-bit signed b format) Document with comments; see example in lab for appropriate level of information, but the format doesn't have to exactly match.	/ 30
extender simulation: all modes, non-trivial inputs and outputs. Do extensions for the MSB of the 8/12/24 bit value is both 0 and 1.	/ 35
extender simulation documentation. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct. You can draw on your simulation and/or add text explanations.	/ 35
Total	/ 100

- Email your PDF and VHDL file to the instructor with a subject of CE1921 Week 3 Lab Submission.
  - PDF: Print all your materials (3 items above) to PDF and add this is the first page. Arrange everything in the ***order*** listed above. You are welcome to use any PDF editing software. If what is available on your MSOE laptop (e.g., Acrobat) turns out to lack any needed features (e.g., combining pages), please mention it in the teams channel and we will figure out an alternative.
    - For the simulation (especially) you may get the best results by taking a screen shot (Alt + Print Screen; on some laptop keyboards you need to also press the fn key to access Print Screen (e.g., on my keyboard fn+rightShift is Print Screen, so I need to press 3 keys)). Then crop it accordingly, perhaps with Windows 10 Paint, although I prefer the free IrfanView program.
  - VHDL: Also include your .VHDL file itself.
- This is due by the end of week 3.