MSOE EECS Department – Dr. Durant
CE1921: Wk. 8 Lab Grading Checklist

Name: _____ Section: _____

Item	**Score**
Indicate any or all that you've completed: ___ S-type; ___ mul; ___ bl/mov pc	/ 0
Control: VHDL. Document all VHDL files in CE1921. Include general information at top, description of each input and output, description of intended behavior, and how you're solving the problem.	/ 20
RTL view: control, decode, ALU, execute, and top-level	/ 10
VHDL or schematic: decode, ALU, execute, top-level (for all CE1921 schematics use comment tool to include title, name and date)	/ 20
Demo : Show professor overall processor simulation in Quartus and answer questions	/ 20
Optional Appendix: Additional VHDL and schematics as needed. Include any components not included above that have changed from previous labs or that you feel are important to understanding operation of your processor. Do not include simple, standard components like registers and bus multiplexors.	/ 0
C-level: S instructions operate correctly (IROMv2 simulation highlighting proper execution of S-extended instructions.) (For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct.)	/ 10
B-level: Multiply ALSO operates correctly (IROMv3 simulation)	/ 10
A-level: BL and MOV PC,LR ALSO operate correctly (IROMv4 simulation)	/ 10
Total	/ 100

- *Staple* this lab cover sheet on top of all the materials you are submitting.
- Submit everything in the ***order*** listed above.
- Your lab packet is due by 10 AM on the day after your lab meets.
- Extra copies of lab checkout sheets are available on my website.