1. Description

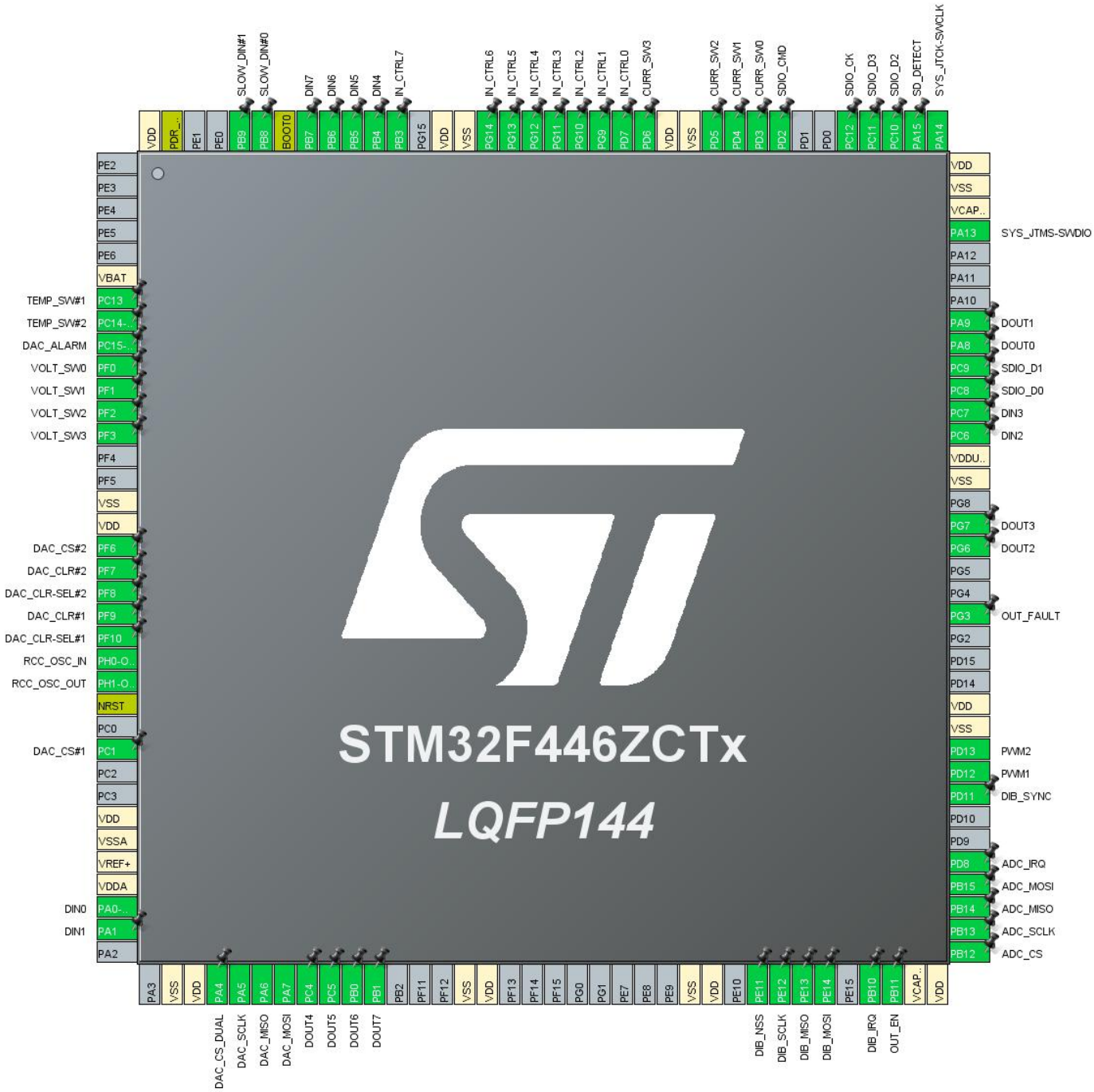
1.1. Project

Project Name	MIO168 r1B2
Board Name	custom
Generated with:	STM32CubeMX 5.6.1
Date	06/11/2020

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446ZCTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

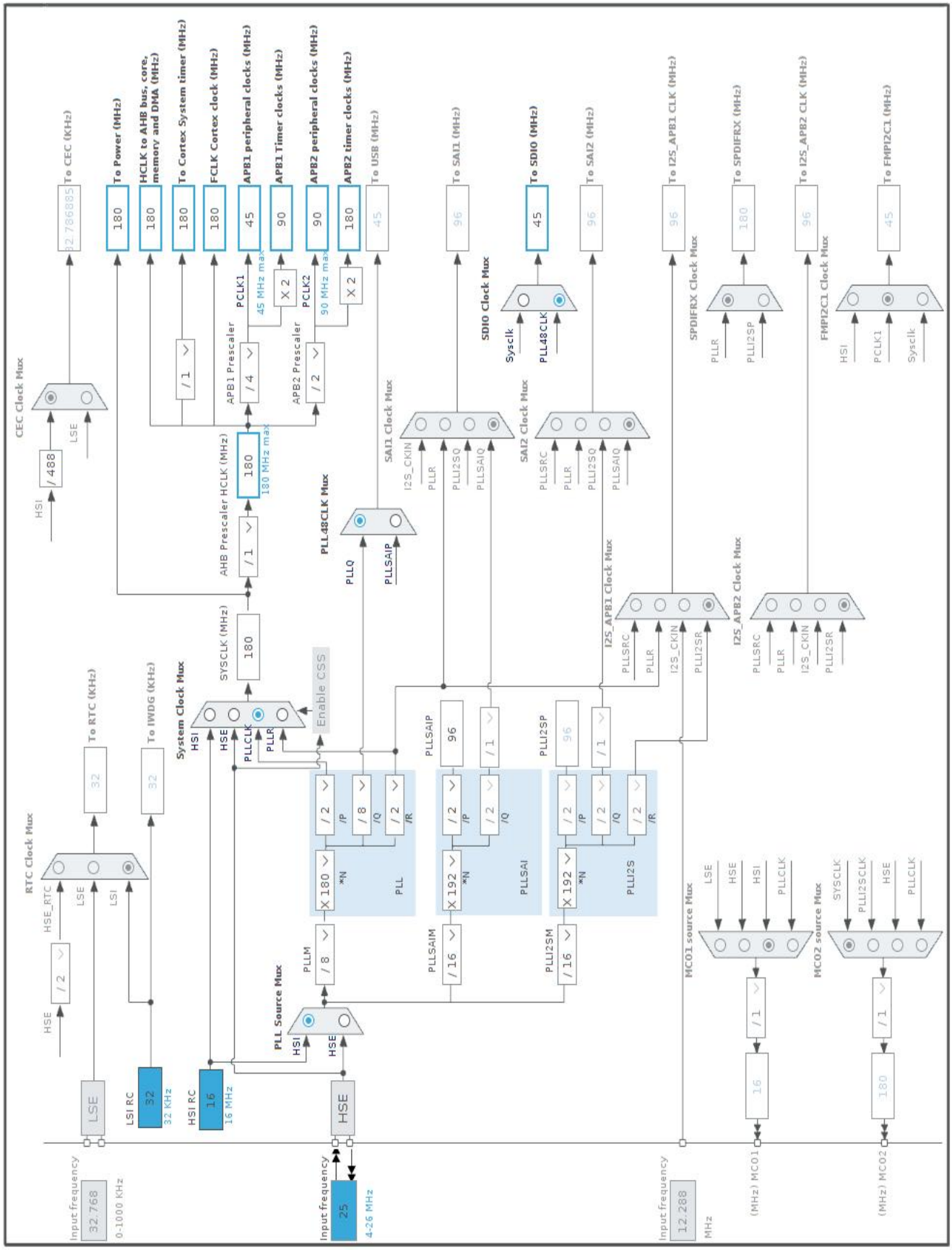
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	TEMP_SW#1
8	PC14-OSC32_IN *	I/O	GPIO_Output	TEMP_SW#2
9	PC15-OSC32_OUT *	I/O	GPIO_Input	DAC_ALARM
10	PF0 *	I/O	GPIO_Output	VOLT_SW0
11	PF1 *	I/O	GPIO_Output	VOLT_SW1
12	PF2 *	I/O	GPIO_Output	VOLT_SW2
13	PF3 *	I/O	GPIO_Output	VOLT_SW3
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	DAC_CS#2
19	PF7 *	I/O	GPIO_Output	DAC_CLR#2
20	PF8 *	I/O	GPIO_Output	DAC_CLR-SEL#2
21	PF9 *	I/O	GPIO_Output	DAC_CLR#1
22	PF10 *	I/O	GPIO_Output	DAC_CLR-SEL#1
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1 *	I/O	GPIO_Output	DAC_CS#1
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	TIM2_CH1	DIN0
35	PA1	I/O	TIM2_CH2	DIN1
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Output	DAC_CS_DUAL
41	PA5	I/O	SPI1_SCK	DAC_SCLK
42	PA6	I/O	SPI1_MISO	DAC_MISO
43	PA7	I/O	SPI1_MOSI	DAC_MOSI
44	PC4 *	I/O	GPIO_Output	DOUT4
45	PC5 *	I/O	GPIO_Output	DOUT5
46	PB0 *	I/O	GPIO_Output	DOUT6
47	PB1 *	I/O	GPIO_Output	DOUT7
51	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	SPI4_NSS	DIB_NSS
65	PE12	I/O	SPI4_SCK	DIB_SCLK
66	PE13	I/O	SPI4_MISO	DIB_MISO
67	PE14	I/O	SPI4_MOSI	DIB_MOSI
69	PB10 *	I/O	GPIO_Output	DIB_IRQ
70	PB11 *	I/O	GPIO_Output	OUT_EN
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	SPI2_NSS	ADC_CS
74	PB13	I/O	SPI2_SCK	ADC_SCLK
75	PB14	I/O	SPI2_MISO	ADC_MISO
76	PB15	I/O	SPI2_MOSI	ADC_MOSI
77	PD8 *	I/O	GPIO_Output	ADC_IRQ
80	PD11 *	I/O	GPIO_Input	DIB_SYNC
81	PD12	I/O	TIM4_CH1	PWM1
82	PD13	I/O	TIM4_CH2	PWM2
83	VSS	Power		
84	VDD	Power		
88	PG3 *	I/O	GPIO_Input	OUT_FAULT
91	PG6 *	I/O	GPIO_Output	DOUT2
92	PG7 *	I/O	GPIO_Output	DOUT3
94	VSS	Power		
95	VDDUSB	Power		
96	PC6 *	I/O	GPIO_Input	DIN2
97	PC7 *	I/O	GPIO_Input	DIN3
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8	I/O	TIM1_CH1	DOUT0
101	PA9	I/O	TIM1_CH2	DOUT1
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15 *	I/O	GPIO_Input	SD_DETECT
111	PC10	I/O	SDIO_D2	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
116	PD2	I/O	SDIO_CMD	
117	PD3 *	I/O	GPIO_Output	CURR_SW0
118	PD4 *	I/O	GPIO_Output	CURR_SW1
119	PD5 *	I/O	GPIO_Output	CURR_SW2
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Output	CURR_SW3
123	PD7 *	I/O	GPIO_Output	IN_CTRL0
124	PG9 *	I/O	GPIO_Output	IN_CTRL1
125	PG10 *	I/O	GPIO_Output	IN_CTRL2
126	PG11 *	I/O	GPIO_Output	IN_CTRL3
127	PG12 *	I/O	GPIO_Output	IN_CTRL4
128	PG13 *	I/O	GPIO_Output	IN_CTRL5
129	PG14 *	I/O	GPIO_Output	IN_CTRL6
130	VSS	Power		
131	VDD	Power		
133	PB3 *	I/O	GPIO_Output	IN_CTRL7
134	PB4 *	I/O	GPIO_Input	DIN4
135	PB5 *	I/O	GPIO_Input	DIN5
136	PB6 *	I/O	GPIO_Input	DIN6
137	PB7 *	I/O	GPIO_Input	DIN7
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	SLOW_DIN#0
140	PB9 *	I/O	GPIO_Output	SLOW_DIN#1
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MIO168 r1B2
Project Folder	/home/denis/BACKUP/EEZ/Digital control/MCU/STM32/Projects/MIO168 r1B2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446ZCTx
Datasheet	027107_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

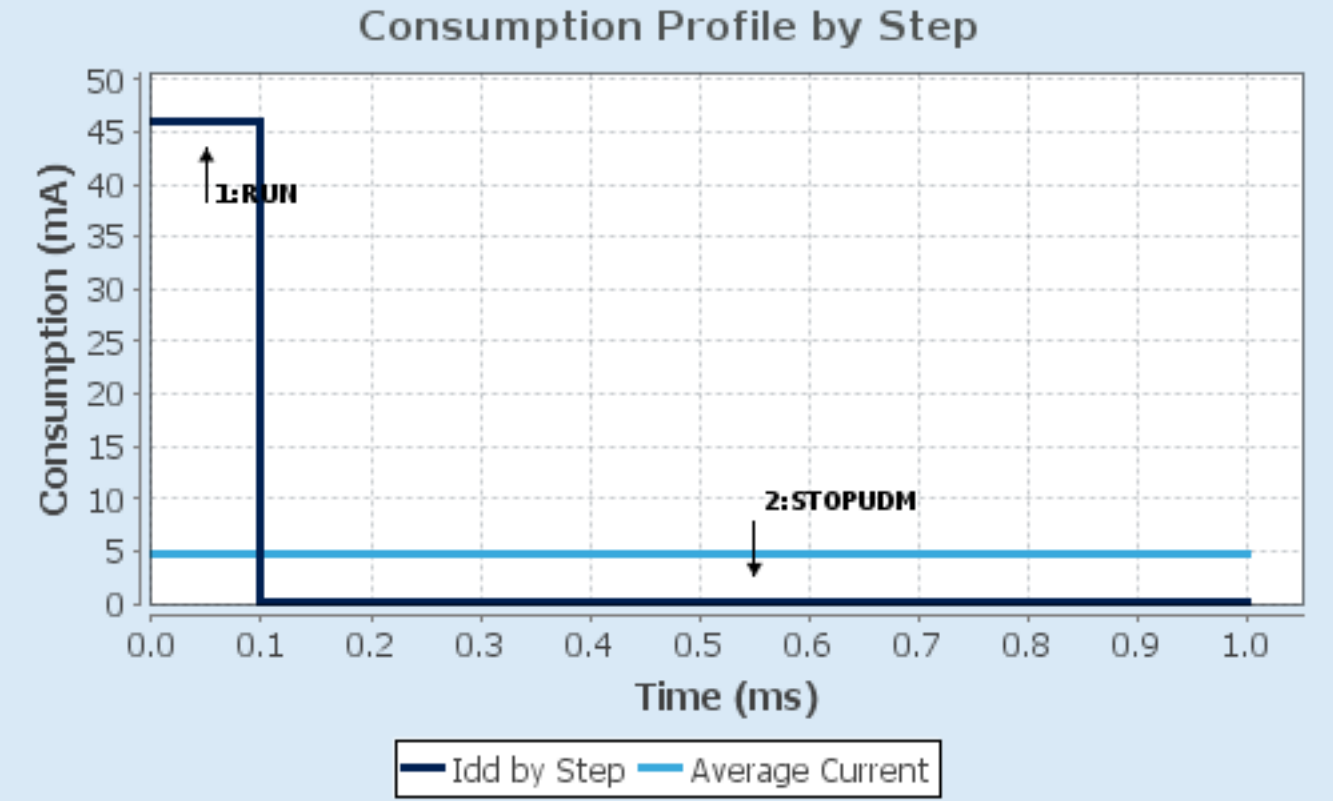
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/PREFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	99.99	104.99
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. CRC

mode: Activated

7.2. GPIO

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

7.4. SDIO

Mode: SD 4 bits Wide bus

7.4.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

7.5. SPI1

Mode: Full-Duplex Slave

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**22.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.7. SPI4

Mode: Full-Duplex Slave

Hardware NSS Signal: Hardware NSS Input Signal

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Input Hardware

7.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.9. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable

BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.10. TIM2

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.11. TIM4

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DAC_SCLK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DAC_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DAC_MOSI
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_CS
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_SCLK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ADC_MOSI
SPI4	PE11	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DIB_NSS
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DIB_SCLK
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DIB_MISO
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	DIB_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DOUT0
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DOUT1
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIN0
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DIN1
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM1
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM2
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEMP_SW#1
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEMP_SW#2
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DAC_ALARM
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VOLT_SW0
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VOLT_SW1
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VOLT_SW2
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VOLT_SW3
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CS#2
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CLR#2
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CLR-SEL#2
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CLR#1
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CLR-SEL#1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CS#1
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC_CS_DUAL
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT4
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT5
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT6
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT7
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIB_IRQ
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUT_EN
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADC_IRQ
	PD11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIB_SYNC
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OUT_FAULT
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT2
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DOUT3
	PC6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN2
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN3
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SD_DETECT
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CURR_SW0
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CURR_SW1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CURR_SW2
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CURR_SW3
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL0
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL1
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL2
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL3
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL4
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL5
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL6
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN_CTRL7
	PB4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN4
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN5
	PB6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN6
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIN7
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SLOW_DIN#0
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SLOW_DIN#1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI4_RX	DMA2_Stream0	Peripheral To Memory	Low
SPI4_TX	DMA2_Stream1	Memory To Peripheral	Low

SPI4_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_TX: DMA2_Stream1 DMA request Settings:

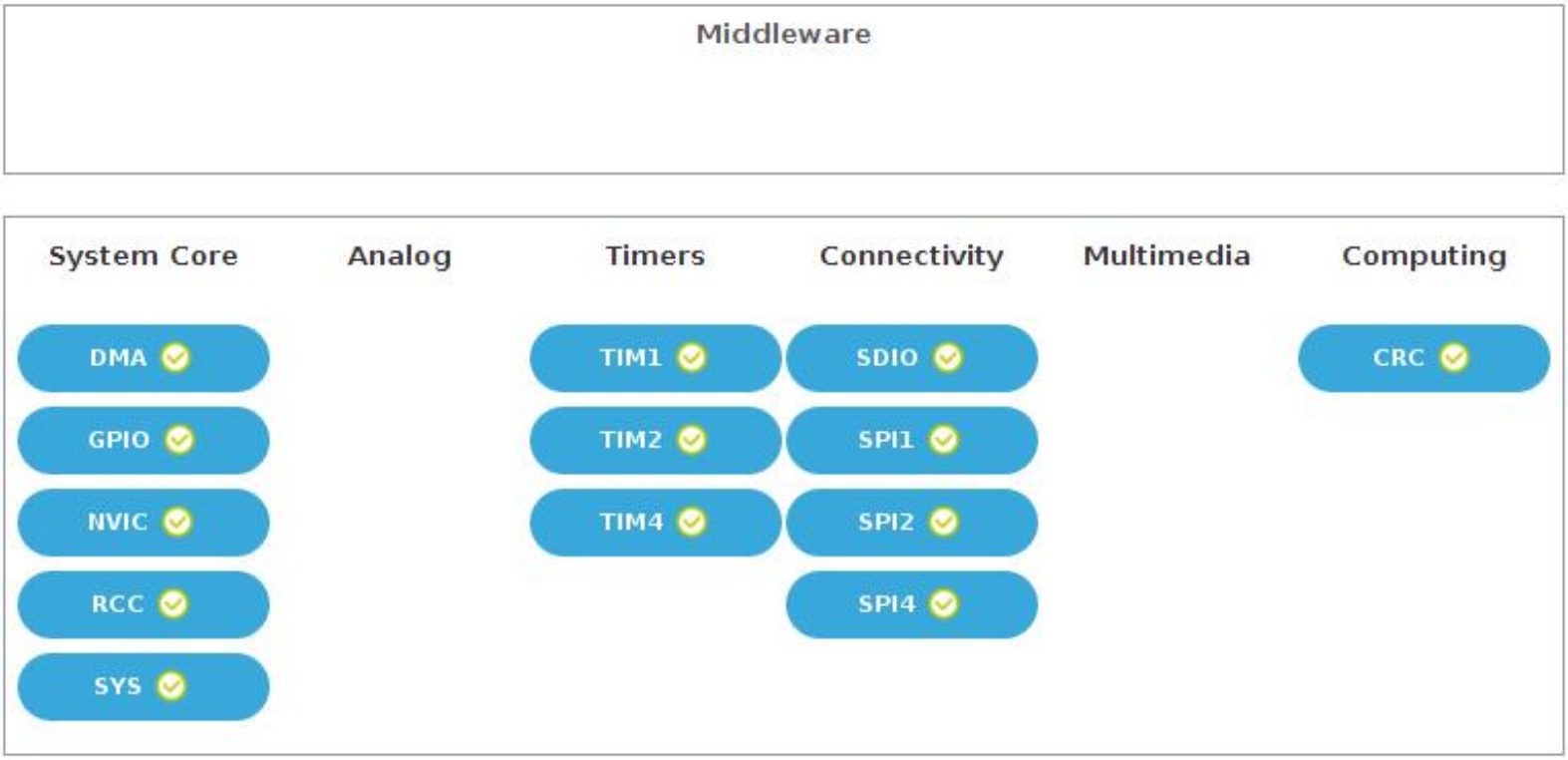
Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
SDIO global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report