Floor Plan of an Implementation of the picoJava-II Core

Data cache tag
(D-Tag)

Data cache tag
(D-Tag)

Phase lock loop
(PLL)

Status RAM

Stack
Manage-
ment Unit
(SMU)

Data
Cache Unit
(DCU)

Hold
logic
(HOLD)

Trap
Control
Unit
(TRAP)

Data cache RAM

Data cache RAM0 Data cache RAM1

Instruction cache RAM

Microcode
(ucode)

Execution (EX)

Register Control Unit
(RCU)

Pipe
Control
Unit
(PIPE)

Instruction
Folding
Unit
(IFU)

Instruction
Cache Unit
(ICU)

Instruction
cache tag
(I-Tag)

FPU ROM0

FPU ROM1

Floating Point Unit (FPU)

Memory, Timer, and I/O Interface Unit