# BrainScaleS Workshop

## 4th HBP School

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# First Section

# Analog Neuromorphic Hardware

1

observations

2

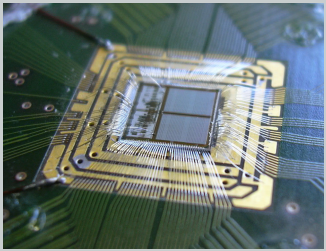
mathematical model

$$C\frac{\mathrm{d}V}{\mathrm{d}t} = -g_\mathrm{L}(V - E_\mathrm{L}) + g_\mathrm{L}\Delta_\mathrm{T}\exp\frac{V - V_\mathrm{T}}{\Delta_\mathrm{T}} - w + I$$

$$\tau_\mathrm{w}\frac{\mathrm{d}w}{\mathrm{d}t} = a(V - E_\mathrm{L}) - w$$

3

hardware realization



# Roadmap

2004

## Spikey

- single chip system
- 384 LIF neurons

2010

## HICANN

- 180 nm CMOS
- 512 AdEx neurons

2015

## 20 Wafer System

- 4 million neurons
- 0.9 billion synapses

2017

## HICANN DLS

- 65 nm CMOS
- PPU: integrated processing unit for advanced plasticity

2022

## 500 Wafer System

- 500 million neurons
- 130 billion synapses

# First Frame

Hello, world!