Hardware Detail of Intel 8088

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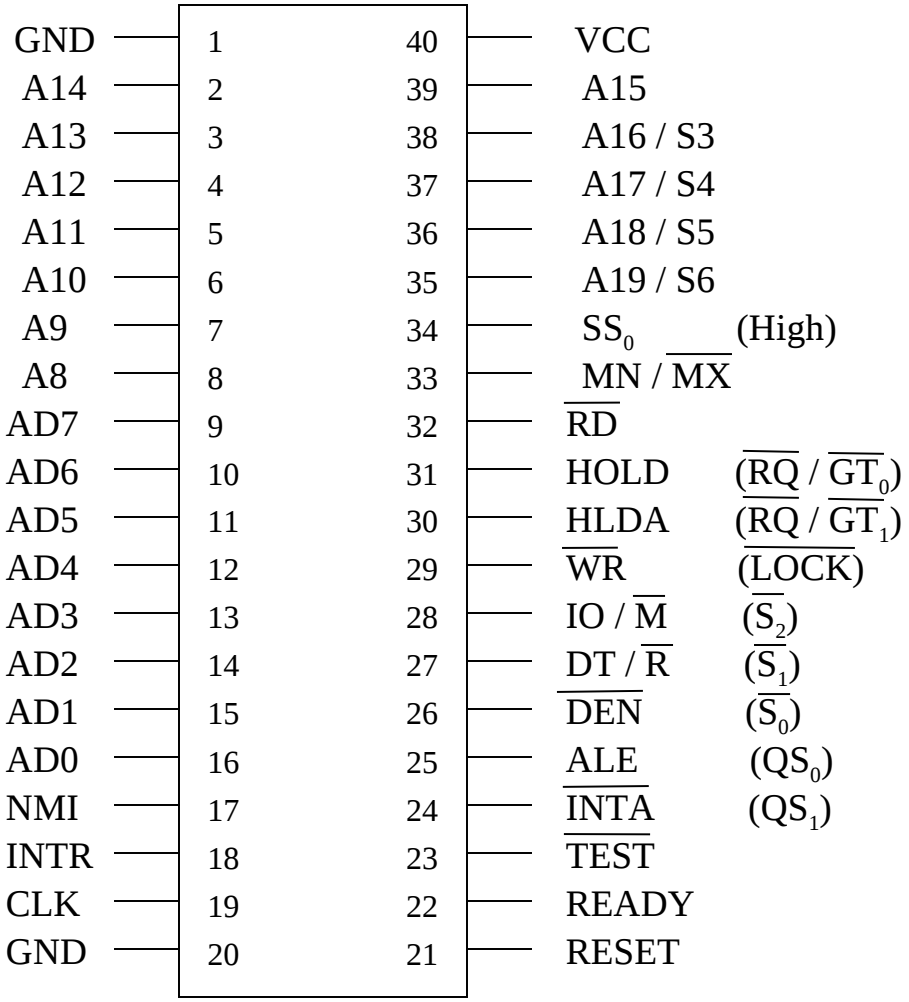
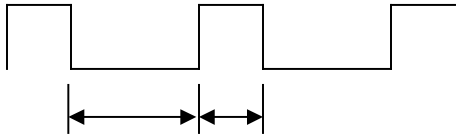
8088 Pin Configuration



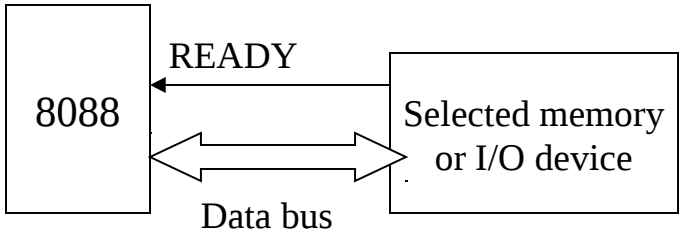
8088 Pin Description

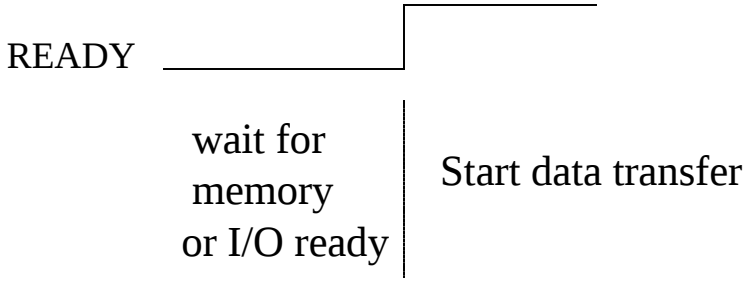
Pin Name	Pin Number	Direction	Description
GND:	1 & 20		Both need to be connected to ground
VCC:	21		VCC = 5V
CLK:	19	Input	33% duty cycle 
MN/$\overline{MX}$:	33	Input	High → Minimum mode Low → Maximum mode
RESET:	21	Input	Reset 8088

- Duration of logic high must be greater than 4*T
- After reset, 8088 fetches instructions starting from memory address FFFF0H

8088 Pin Description

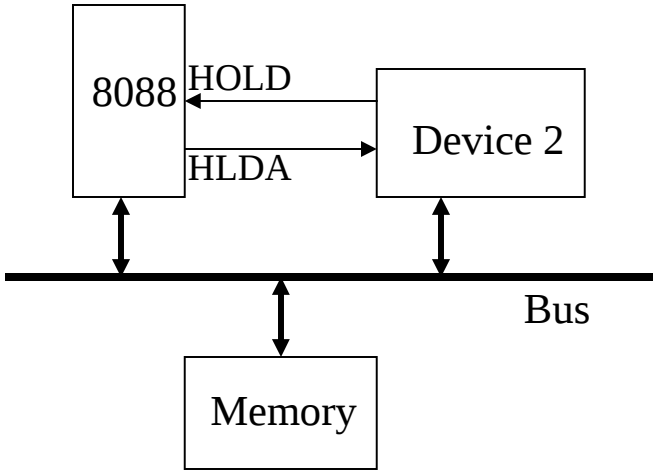
Pin Name	Pin Number	Direction	Description
READY	22	Input	Informs the processor that the selected memory or I/O device is ready for a data transfer





8088 Pin Description

Pin Name	Pin Number	Direction	Description
HOLD	31	Input	The execution of the processor is suspended as long as HOLD is high
HLDA	30	Output	Acknowledges that the processor is suspended

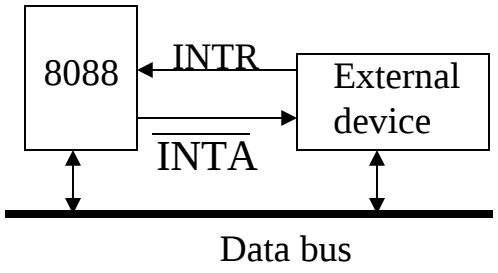


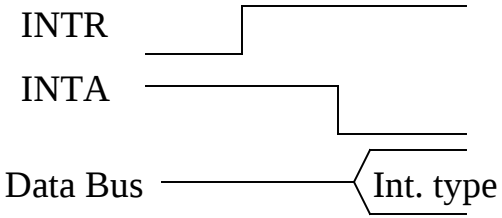
- Procedure for Device 2 to use bus
  - — Drive the HOLD signal of 8088 high
  - — Wait for the HLDA signal of 8088 becoming high
  - — Now, Device2 can send data to bus

8088 Pin Description

Pin Name	Pin Number	Direction	Description
NMI	17	Input	Causes a non-maskable type-2 interrupt
INTR	18	Input	Indicates a maskable interrupt request
$\overline{\text{INTA}}$	24	Output	Indicates that the processor has received an INTR request and is beginning interrupt processing

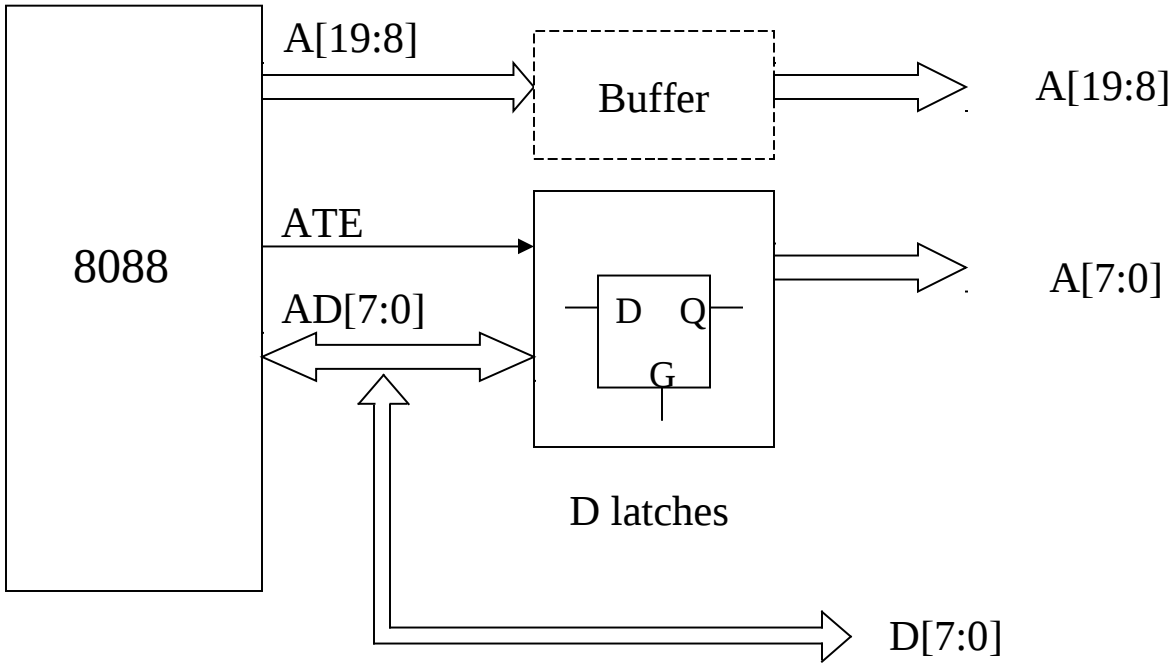
- **NMI (non-maskable interrupt):** a rising edge on NMI causes a type-2 interrupt
- **INTR:** logic high on INTR poses an interrupt request. However, this request can be masked by IF **(Interrupt enable Flag**). The type of interrupt caused by INTR is read from data bus
- **$\overline{\text{INTA}}$:** control when the interrupt type should be loaded onto the data bus





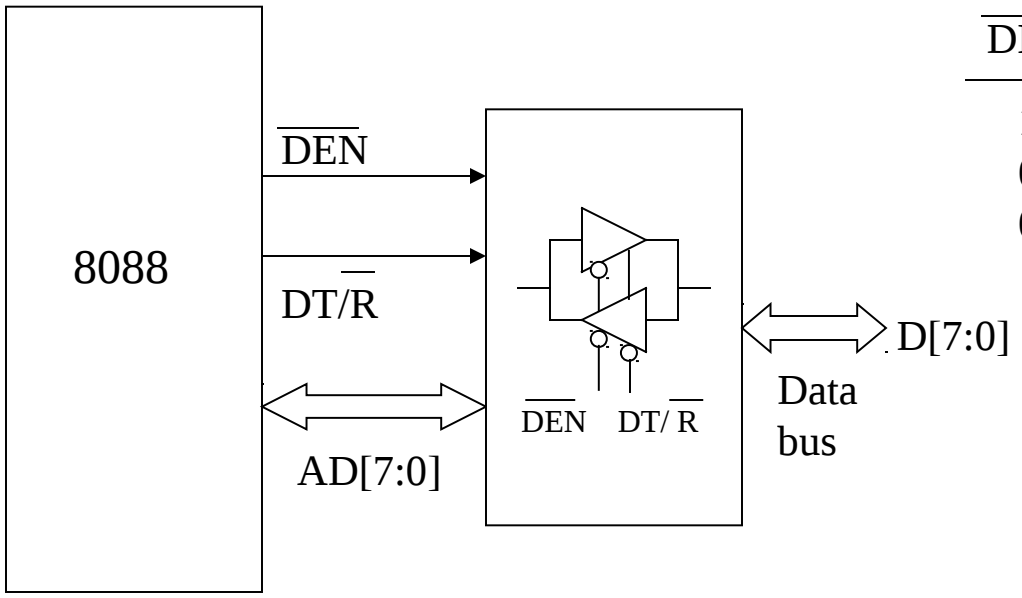
8088 Pin Description

Pin Name	Pin Number	Direction	Description
ALE	25	Output	Indicates the current data on 8088 address/data bus are address



8088 Pin Description

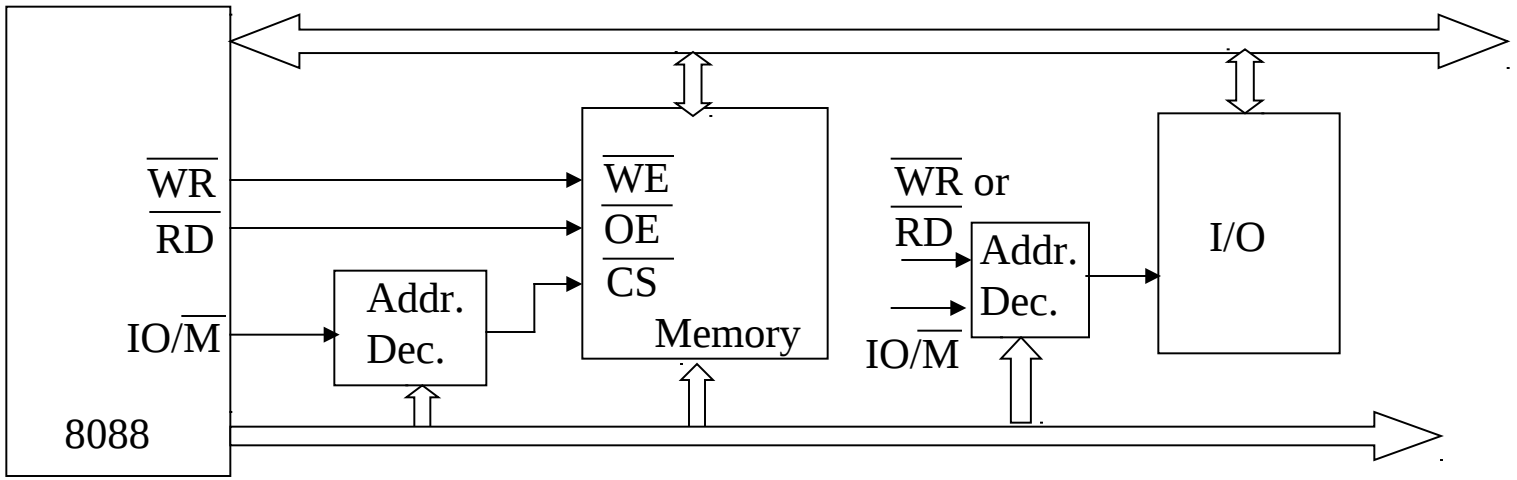
Pin Name	Pin Number	Direction	Description
$\overline{DEN}$	26	Output	Disconnects data bus connection
DT / $\overline{R}$	27	Output	Indicates the direction of data transfer



$\overline{DEN}$	DT/$\overline{R}$	
1	X	Disconnected
0	0	To 8088
0	1	From 8088

8088 Pin Description

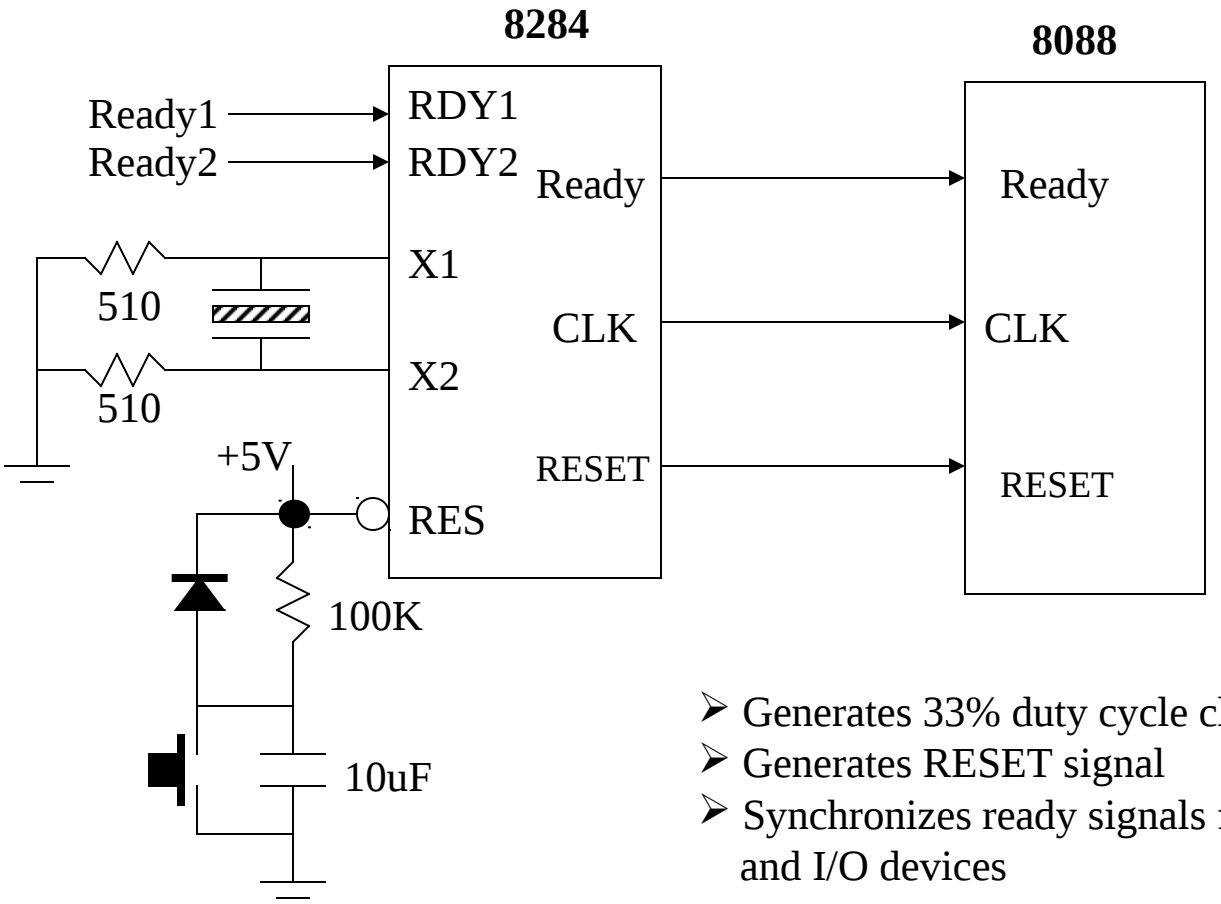
Pin Name	Pin Number	Direction	Description
$\overline{WR}$	29	Output	Indicates that the processor is writing to memory or I/O devices
$\overline{RD}$	32	Output	Indicates that the processor is reading from memory or I/O devices
IO/ $\overline{M}$	28	Output	Indicates that the processor is accessing whether memory (IO/$\overline{M}$=0) or I/O devices (IO/$\overline{M}$=1)



8088 Pin Description

Pin Name	Pin Number	Direction	Description
AD[7:0]	9-16	I/O	Address / Data bus
A[19:8]	2-8, 35-39	Input	Address bus
SS_0	34	Output	Status Output
$\overline{TEST}$	23	Input	It is examined by processor testing instructions

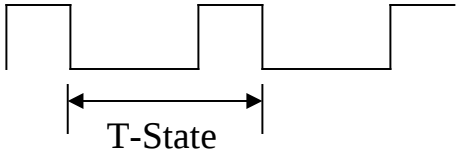
8284 Clock Generator



- Generates 33% duty cycle clock signal
- Generates RESET signal
- Synchronizes ready signals from memory and I/O devices

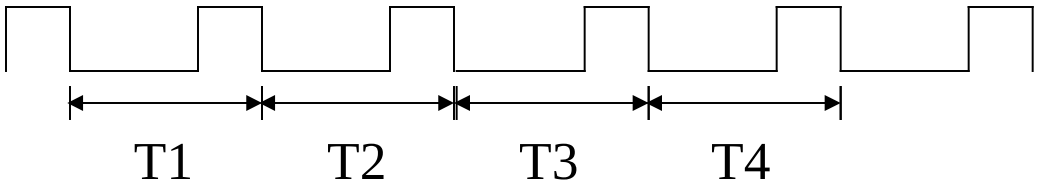
System Timing Diagrams

- T-State:
  - — One clock period is referred to as a T-State

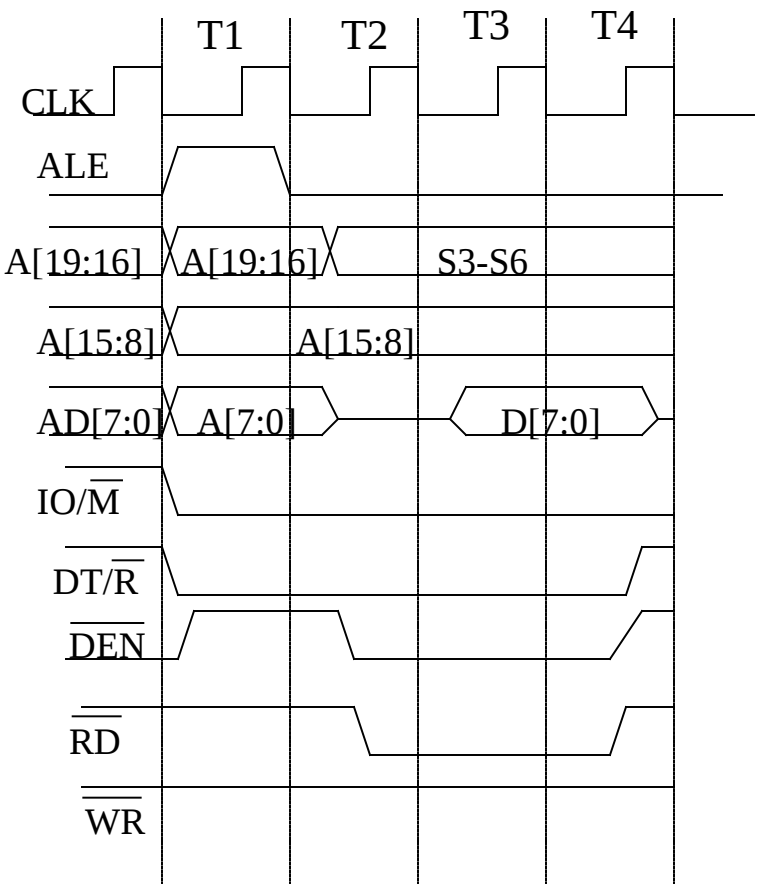


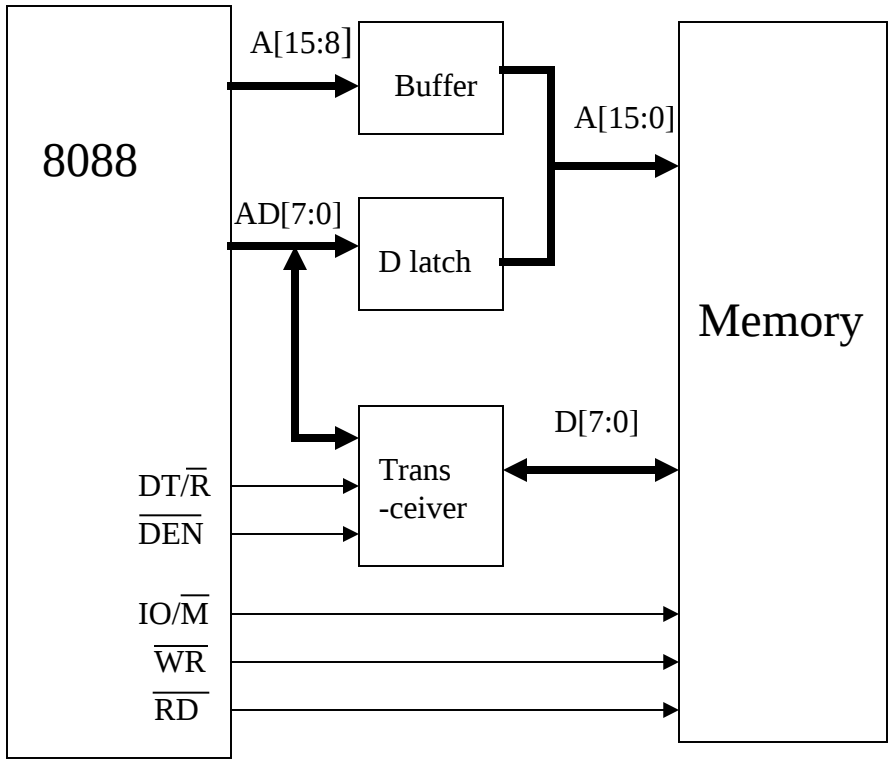
  - — An operation takes an integer number of T-States

- CPU Bus Cycle:
  - — A bus cycle consists of 4 or more T-States

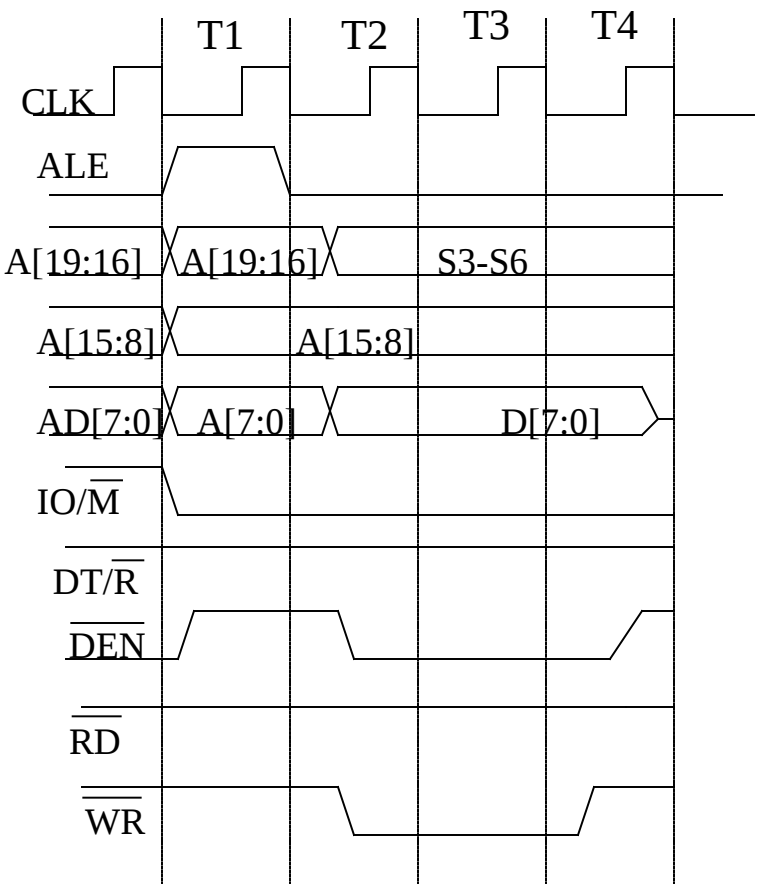


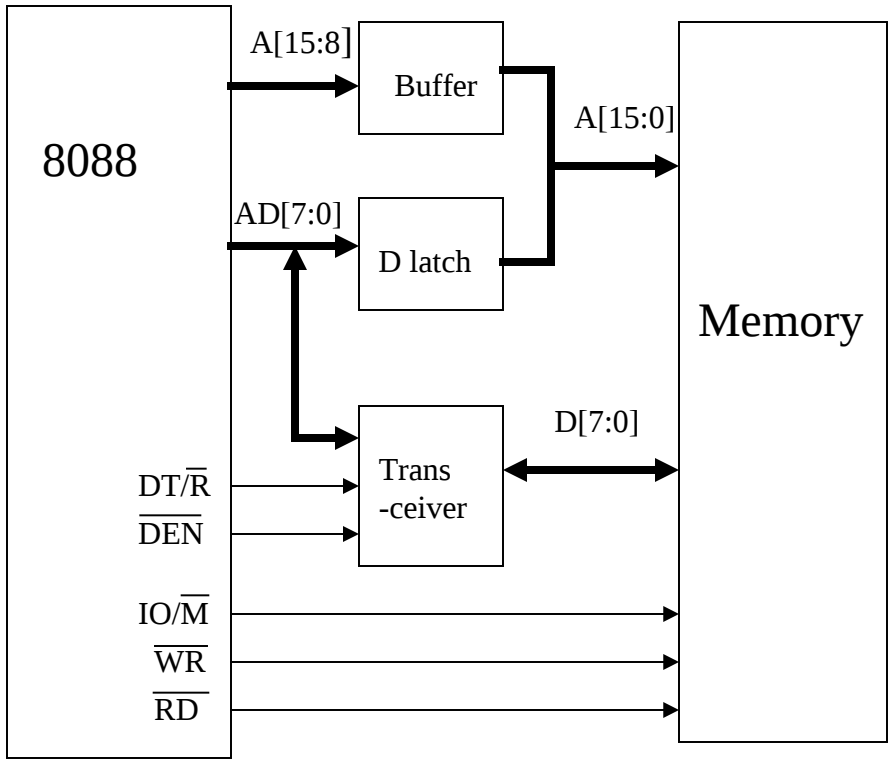
Memory Read Timing Diagrams



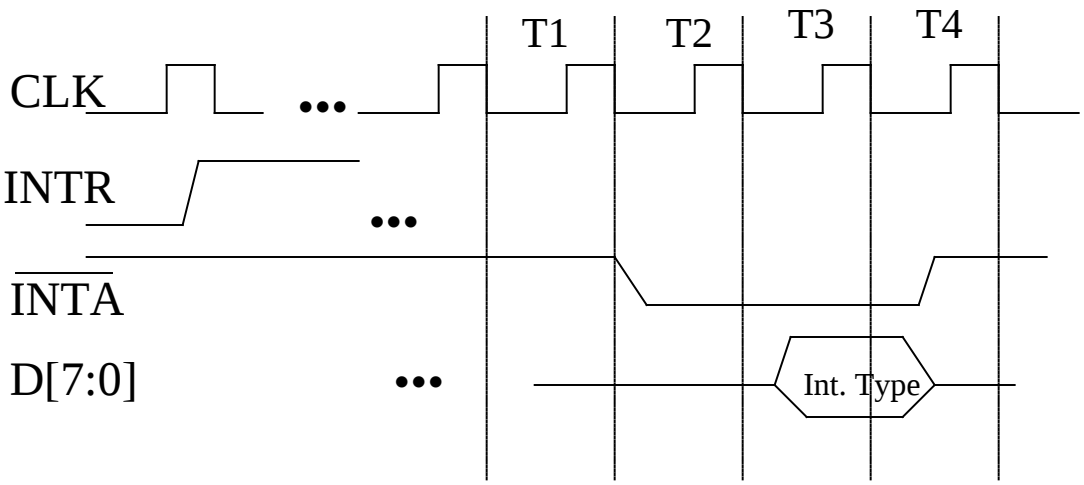


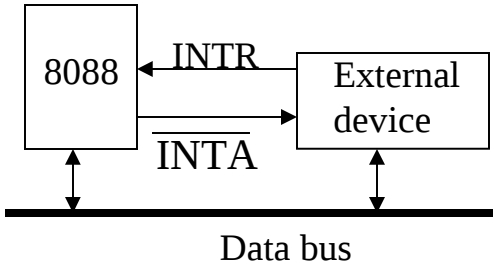
Memory Write Timing Diagrams





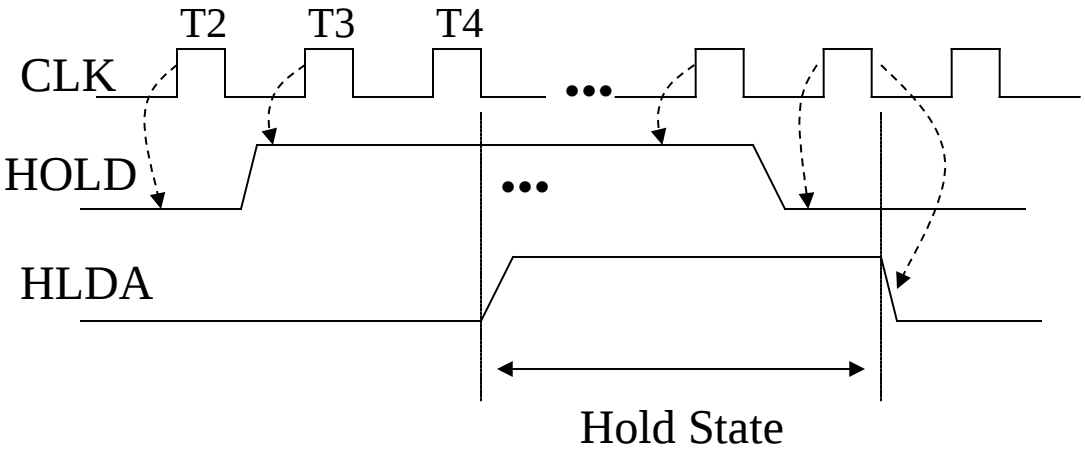
Interrupt Acknowledge Timing Diagrams

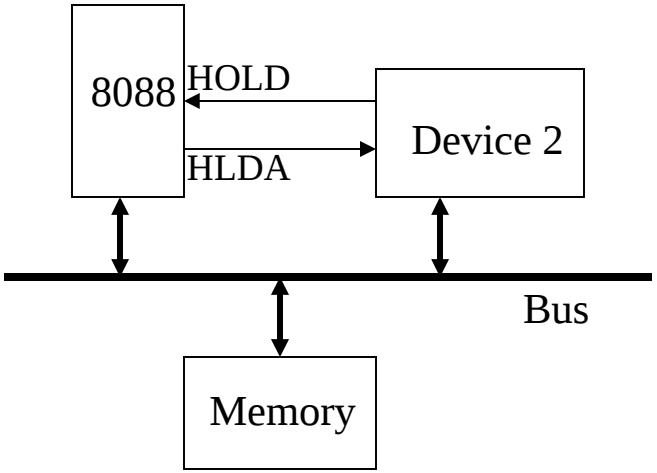




- It takes one bus cycle to perform an interrupt acknowledge
- During T1, the process tri-states the address bus
- During T2, $\overline{\text{INTA}}$ is pulled low and remains low until it becomes inactive in T4
- The interrupting devices places an 8-bit interrupt type during $\overline{\text{INTA}}$ is active

HOLD/HLDA Timing Diagrams





- The processor will examine HOLD signal at every rising clock edge
- If HOLD=1, the processor will pull HLDA high at the end of T4 state (end of the execution of the current instruction) and suspend its normal operation
- If HOLD=0, the processor will pull down HLDA at the falling clock edge and resume its normal operation