

TEAM IBM PC

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1 Full Design Specification

Our IBM PC implementation attempts to follow the original IBM PCs design as closely as possible. As a result, we have based our design on the original circuitry of the IBM PC. However, we have made some modifications that are detailed in this report. Our design specification consists of four primary sections. Section A details the partition between software and hardware. In particular, it covers information about the BIOS that the PC will boot from and the peripherals that allow it more complex software functionality. Section B details the three primary data buses on the IBM PC, including the data bus, the control bus, and the address bus. Section C is a block diagram from the IBM PC hardware specifications that provides a high-level overview of each subsystem. Section D details the subsystems that comprise the IBM PC.

1.1 Software / Hardware Partition

The software on the IBM PC is stored in two hardware areas, the Read Only Memory (ROM) and the Floppy Drive. The ROM stores the IBM PCs BIOS and the Floppy Drive stores the IBM PCs Operating System. The software stored in each area is executed by the Intel 8088 processor. We have obtained the binary file of the IBM PCs BIOS and we will be obtaining a binary file of DOS or another operating system.

1.1.1 ROM and BIOS

The ROM on the IBM PC consists of 64 kilobytes of memory. It contains two important pieces of software, the IBM PCs BIOS and a copy of IBM PC BASIC. The IBM PC starts by reading from its BIOS and determining if its floppy or cassette drive contains an operating system. If they do not, the BIOS starts loading IBM PC BASIC. This BASIC interpreter is very similar to BASIC found on other early computers, such as the Commodore 64.

We have already made use of ISEs CoreGen to obtain block RAM to hold the binary file for our BIOS. We have tested it under simulation and our image can be read from block RAM. Once we have the whole system together, we will be able to test to see if our system boots correctly.

Our first goal on start up is to get the BIOS to run without halting the system. If an error is discovered on startup, the BIOS will halt the system.

Our second goal will be to get the BIOS to boot us into IBM PC BASIC, which is included on the binary file we have obtained.

1.1.2 Floppy Drive and Operating System

The BIOS on the IBM PC tests to see if any peripherals are connected that contain an operating system, such as a cassette drive or diskette drive. For our system, we have chosen to emulate a diskette drive rather than a cassette drive. We plan to use CoreGen to instantiate block RAM to hold our floppy disk image. We have not yet obtained a copy of DOS to run on our PC. However, there are a number of images on the internet which are available for our use. Once we have an image, our next goal will be to run DOS on our IBM PC. Once we know that DOS runs, we plan to get a floppy disk image of a game and run it on the IBM PC.

1.2 Interface Definitions

1.2.1 Control Bus

1.2.2 Address Bus

1.2.3 Data Bus

1.3 System Block Diagram

1.4 Subsystem Definitions

1.4.1 CPU (Intel 8088)

1.4.2 Floppy Drive

1.4.3 Direct Memory Access (Intel 8237A)

1.4.4 BIOS, RAM, and ROM

1.4.4.1 BIOS

1.4.4.2 RAM

1.4.4.3 BIOS

1.4.5 Keyboard and I/O Interface (Intel 8255)

1.4.5.1 Keyboard

1.4.5.2 I/O Interface (Intel 8255)

1.4.6 Programmable Interval Timer (Intel 8253)

1.4.7 Video (VGA)

1.4.8 Speaker (Piezoelectric Speaker)

1.4.9 Programmable Interrupt Controller (Intel 8259)

1.4.10 Timer (Intel 8284)

1.4.11 Bus Controller (Intel 8288)

1.4.12 Motherboard

1.4.12.1 Motherboard Section 1

1.4.12.2 Motherboard Section 2

1.4.12.3 Motherboard Section 3

1.4.12.4 Motherboard Section 4

1.4.12.5 Motherboard Section 5

1.4.12.6 Motherboard Section 6 and 7

1.4.12.7 Motherboard Section 8

1.4.12.8 Motherboard Section 9

1.4.12.9 Motherboard Section 10

2 Schedule / Management Decisions

2.1 Original Schedule Plan

2.2 Revisions Made to Schedule

2.2.1 CPU (Intel 8088)

2.2.2 Floppy Drive

2.2.3 Direct Memory Access (Intel 8237A)

2.3 Revised Schedule Plan