

# DIGITAL LOGIC

## exam 2

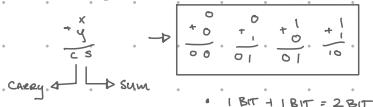
### UNSIGNED

• BITS REPRESENTED BY POSITIVE INT.								
• CANNOT REP RESENT NEG'S								
$z^7 \ z^6 \ z^5 \ z^4 \ z^3 \ z^2 \ z^1 \ z^0$								
<table border="1"> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td> </tr> </table>	0	0	1	0	1	1	0	0
0	0	1	0	1	1	0	0	
$= (+) 44$								

### ADDITION OF UNSIGNED NUMBERS

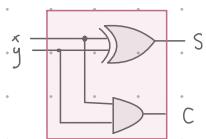
#### SINGLE BIT

##### ADDITION OF 2 BITS



##### TRUTH TABLE

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



HALF ADDER



### MULTIBIT

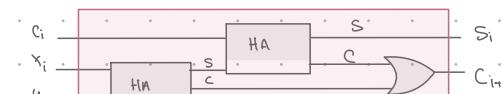
#### C<sub>3</sub> C<sub>2</sub> C<sub>1</sub> C<sub>0</sub>

$$+ x_2 \quad x_1 \quad x_0$$

$$+ y_2 \quad y_1 \quad y_0$$

$$S_2 \quad S_1 \quad S_0$$

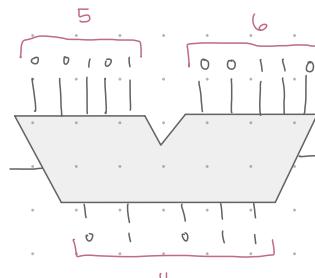
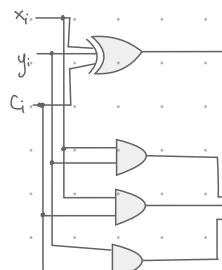
C <sub>i</sub>	X <sub>i</sub>	Y <sub>i</sub>	C <sub>i+1</sub>	S <sub>i</sub>
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



FULL ADDER

$x_i, y_i$	$C_i$	$S_i$	$C_{i+1}$
0, 0	0	0	0
0, 0	1	1	0
0, 1	0	1	1
0, 1	1	0	1
1, 0	0	1	0
1, 0	1	0	1
1, 1	0	1	1
1, 1	1	0	1

FULL ADDER



### SIGNED

#### SIGNED

- LEFTMOST BIT REPRESENTS "SIGN" OF NUMBER
- 0 = POSITIVE
- 1 = NEGATIVE

SIGN	$z^6$	$z^5$	$z^4$	$z^3$	$z^2$	$z^1$	$z^0$
1	0	1	0	1	1	0	0

$= (-) 44$

### SUBTRACTION OF UNSIGNED NUMBERS

you SUBTRACT LOW FROM TOP

BORROW IF NEEDED

OVERFLOW IF GREATEST BIT HAS TO BORROW

$$\begin{array}{r} 0\ 0\ 2 \\ - 1\ 1\ 0 \\ \hline 1\ 1\ 0 \end{array}$$

overflow

bin	DECIMAL	1'S	2'S
0111	+7	+7	+7
0110	+6	+6	+6
0101	+5	+5	+5
0100	+4	+4	+4
0011	+3	+3	+3
0010	+2	+2	+2
0001	+1	+1	+1
0000	0	0	0
1000	-0	-7	-8
1001	-1	-6	-7
1010	-2	-5	-6
1011	-3	-4	-5
1100	-4	-3	-4
1101	-5	-2	-3
1110	-6	-1	-2
1111	-7	-0	-1

### 1'S Complement

INVERT BITS

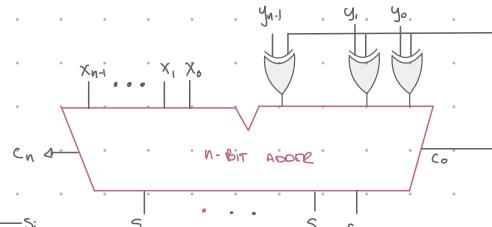
USED IN SUBTRACTION OR ADDITION OF NEG. NUMBERS

### 2'S Complement

NEGATE PROBLEM  
(SUBTRACT+ADD)

$\rightarrow$  8 BIT NEGATED

### ADDER/ SUBTRACTOR UNIT



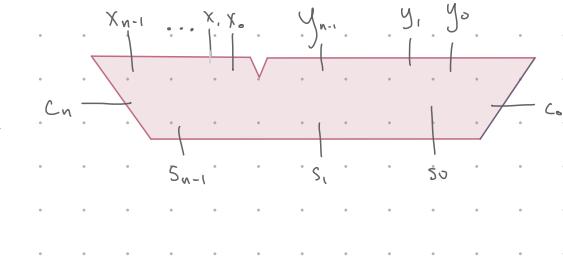
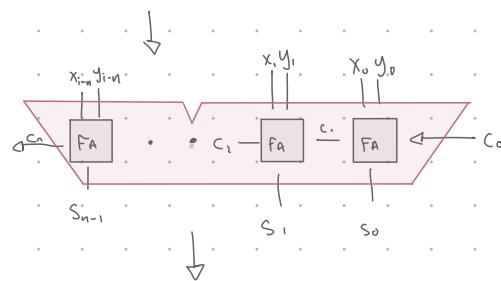
### OVERFLOW

#### ADDITION

WHEN 2 LARGEST BITS DIFFER

SUBTRACTION

IF 2'S Comp ARE SUB.  
+ SIGN IS DIFF

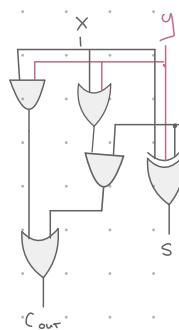


# RIPPLE CARRY ADDER

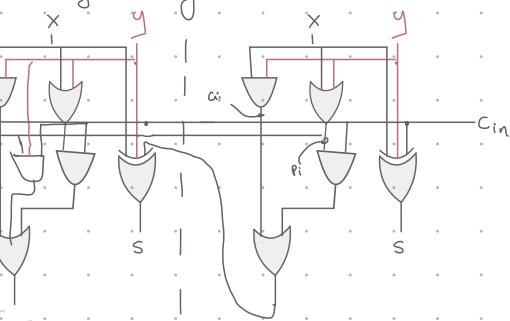
VS

# CARRY-LOOKAHEAD ADDER

Slower by 1 delay  
↳  $2n+1$

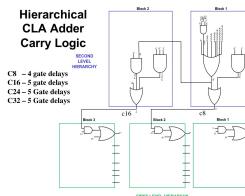


ONLY 4 DELAY!



# HIERARCHICAL

8 GATE DELAYS



# MULTIPLICATION

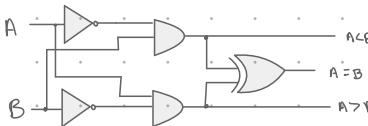
Simply ADD n zeros when multiplied by  $2^n$ .  
↳  $101 \cdot 4 = 101 \cdot 2^2 = 10100$

DIVISION IS SAME CONCEPT BUT REVERSED.

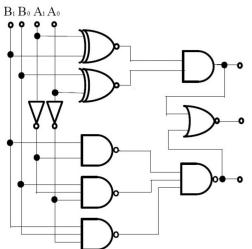
# COMPARATORS

ONE BIT:

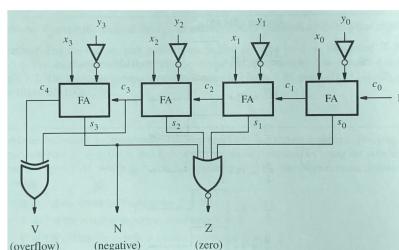
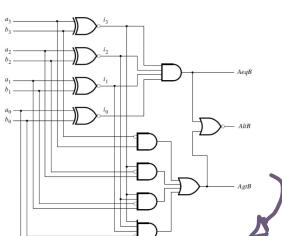
IN PLATS		OUT PLATS		
A	B	$A > B$	$B = A$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



TWO BIT:



Four Bit:



# IEEE CONVERSION

1. SPLIT BOTH SIDES OF DECIMAL + CONVERT TO BINARY
2. PUT DECIMAL LEFT 1<sup>ST</sup> 1 (SCIENTIFIC NOTATION)
3. EXPONENT =  $N \rightarrow 1 \dots 2^n$

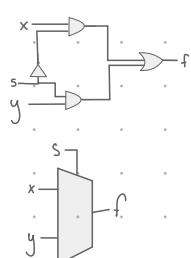
↳  $S = 1 \rightarrow \text{NEG}, 0 \rightarrow \text{POS}$   
 $E = n \text{ OF } 2^n$

$M = \text{AFTER DECIMAL}$

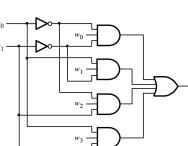


# MUX

2x1 CIRCUIT



4x1



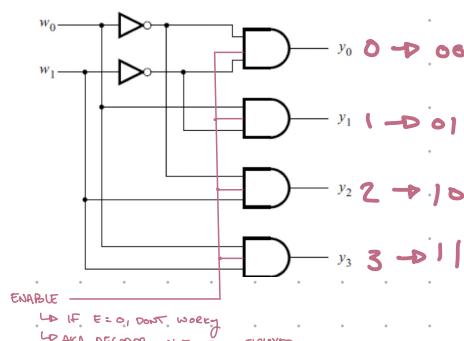
# SHANNON'S EXPANSION

$$f(w_1, w_2, w_3, \dots, w_n) = \bar{w}_1 f(0, w_2, \dots) + w_1 f(1, w_2, \dots)$$

$$\Rightarrow f(w_1, w_2, w_3, \dots) = \bar{w}_1 f_{\bar{w}_1} + w_1 f_{w_1}$$

# DECODERS

The Logic Circuit  
for a 2-to-4 Decoder

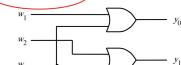


# ENCODER

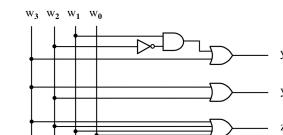
Circuit for a 4-to-2 binary encoder

$w_3$	$w_2$	$w_1$	$w_0$	$y_1$	$y_0$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	0	0	1

It is assumed that the inputs are one hot encoded



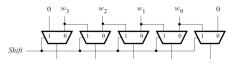
Circuit for the 4-to-2 priority encoder



# CODE CONVERTER

CONVERTS ONE TYPE OF ENCODING TO ANOTHER  
W/O A DON'T CARE output

## SHIFTER Circuit



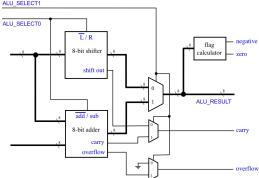
## BARREL SHIFTER

A barrel shifter circuit

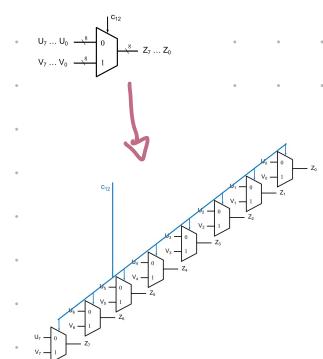
	$w_3$	$w_2$	$w_1$	$w_0$	$y_3$	$y_2$	$y_1$	$y_0$
0	0	0	$w_3$	$w_2$	0	0	0	0
0	1	0	$w_3$	$w_2$	$w_3$	0	0	0
1	0	0	$w_3$	$w_2$	$w_3$	$w_2$	0	0
1	1	0	$w_3$	$w_2$	$w_3$	$w_2$	$w_1$	0

(a) Truth table

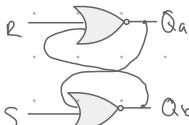
## ALU



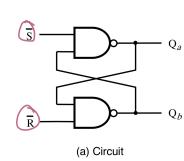
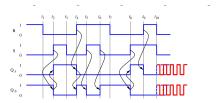
## BUS MUX



## LATCH



S	R	Q <sub>a</sub>	Q <sub>b</sub>
0	0	0	NC
0	1	0	1
1	0	1	0
1	1	0	0



S	R	Q <sub>a</sub>	Q <sub>b</sub>
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	0/1

(a) Circuit

## FLAG ABBREVIATIONS

CF	CARRY FLAG
OF	OVER FLOW
NF	NEGATIVE FLAG
ZF	ZERO FLAG

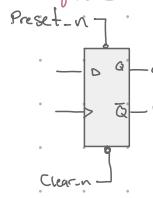
## Comp w/ FLAGS:

EQUAL	$ZF = 1$
NOT EQUAL	$ZF = 0$
GREATER OR EQUAL	$ZF = 0 \& NF = OF$
LESS	$NF = OF$
LESS OR EQUAL	$ZF = 1 \text{ or } NF \neq OF$

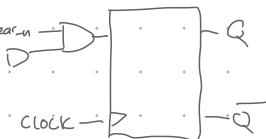
## CLEAR

TRIGGERED + MAKES Q=0

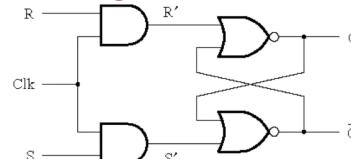
ASYNC



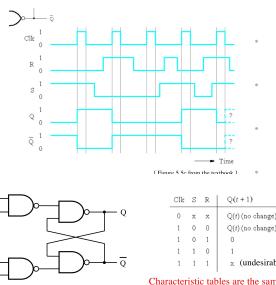
Synch



## GATED SR LATCH

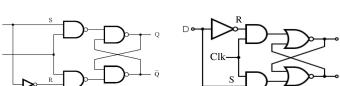


Clk	S	R	Q(t+1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x



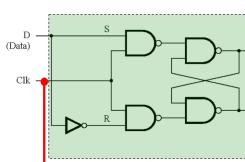
Characteristic tables are the same

## GATED D LATCH

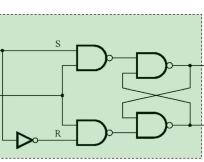


## MASTER SLAVE

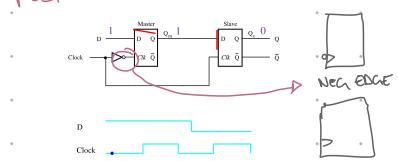
### Master Latch



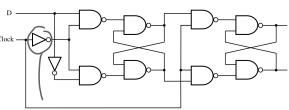
### Slave Latch



## POSITIVE EDGE FLIP FLOP

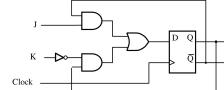


## POSITIVE EDGE



REMOVE TO MAKE NEUT

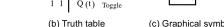
## JK FLIP FLOP



(a) Circuit

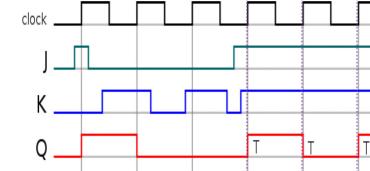


(b) Truth table



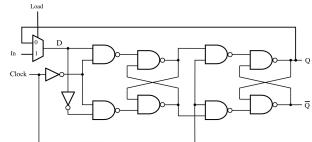
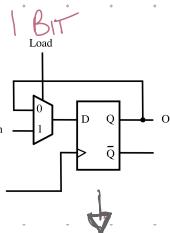
(c) Graphical symbol

[Figure 5.16 from the textbook]

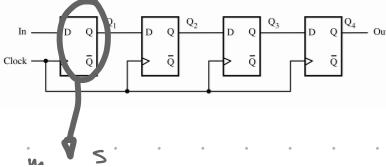


# REGISTER

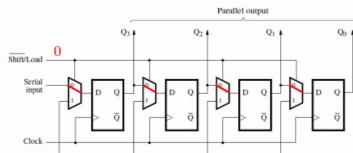
n-bit structure of flipflops



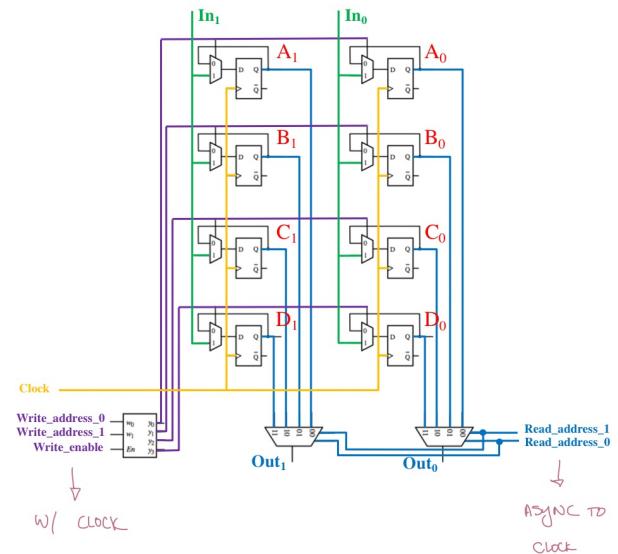
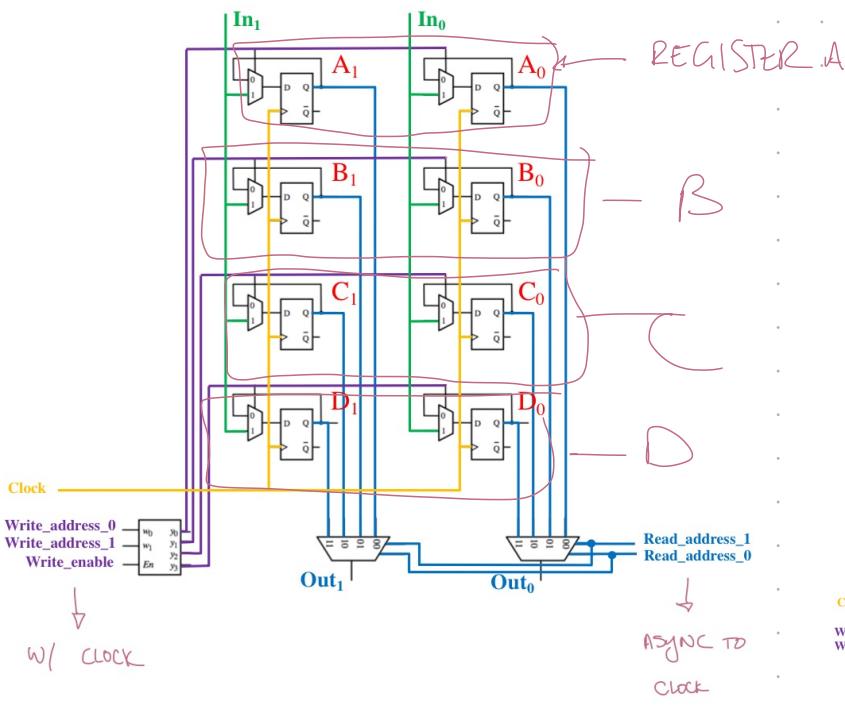
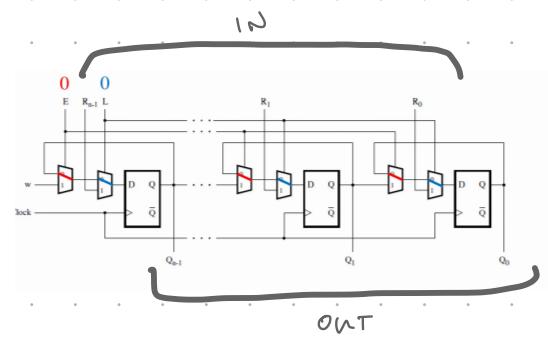
## SHIFTER



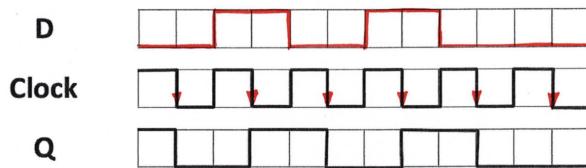
## → PARALLEL



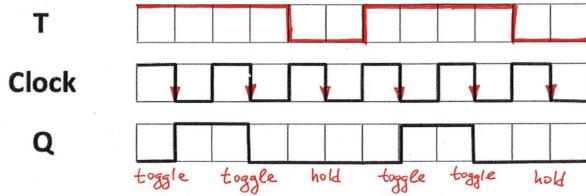
## → LOAD + ENABLE



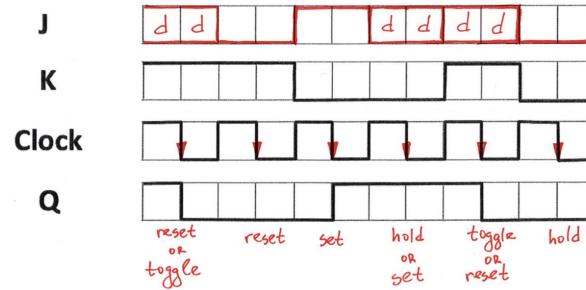
a) Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



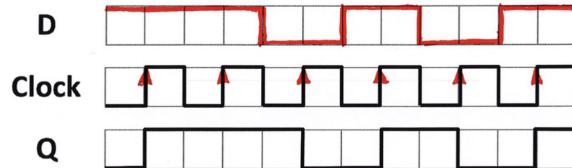
b) Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.



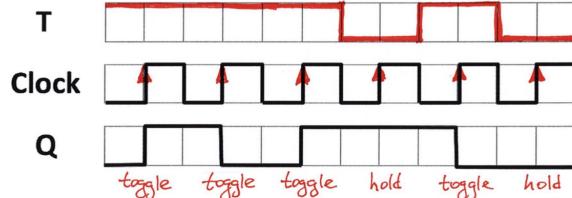
c) Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.



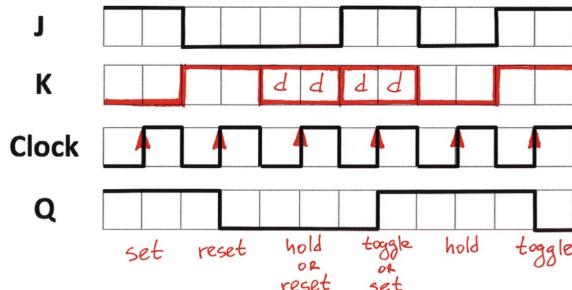
a) Complete the timing diagram for the D input to a positive-edge triggered D flip-flop.



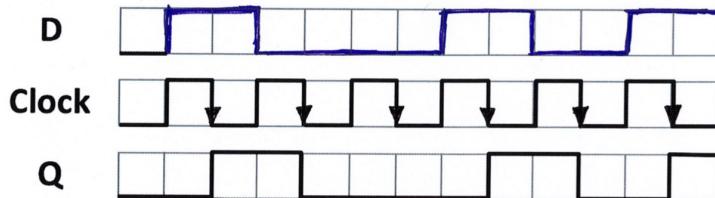
b) Complete the timing diagram for the T input to a positive-edge triggered T flip-flop.



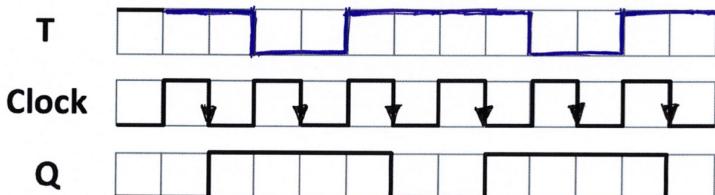
c) Complete the timing diagram for the J input to a positive-edge triggered JK flip-flop.



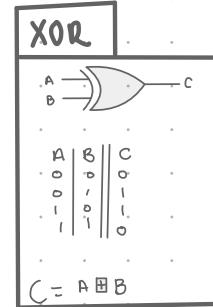
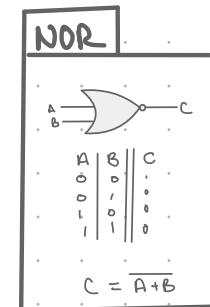
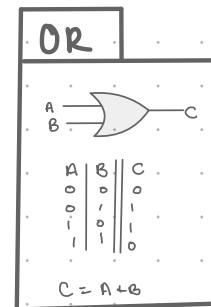
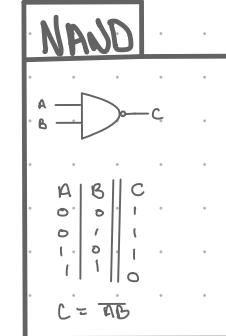
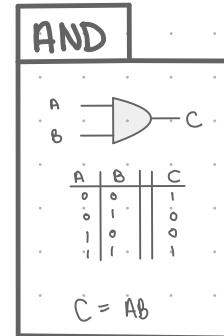
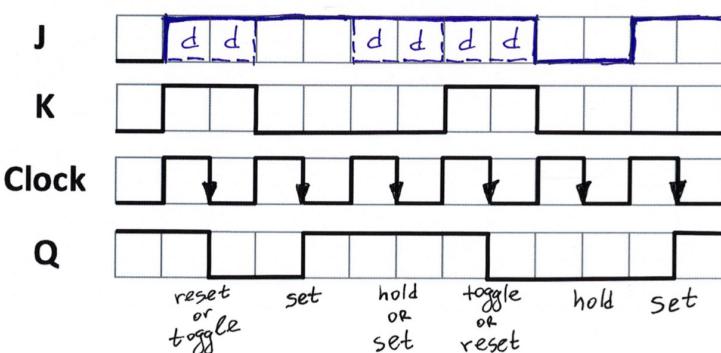
a) Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



b) Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.



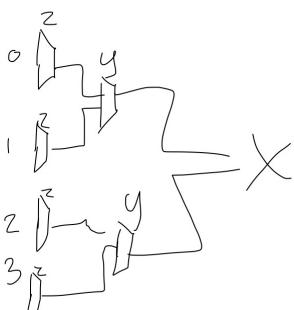
c) Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.



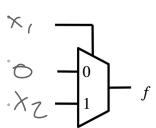
8. Multiplexers (3 x 5p each = 15p)

a) Draw the truth table for the function  $f(x, y, z) = \overline{x} \overline{y} z + \overline{x} y \overline{z} + x \overline{y} \overline{z}$ .

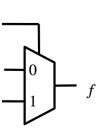
x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



AND



OR



NOT

