1. Description

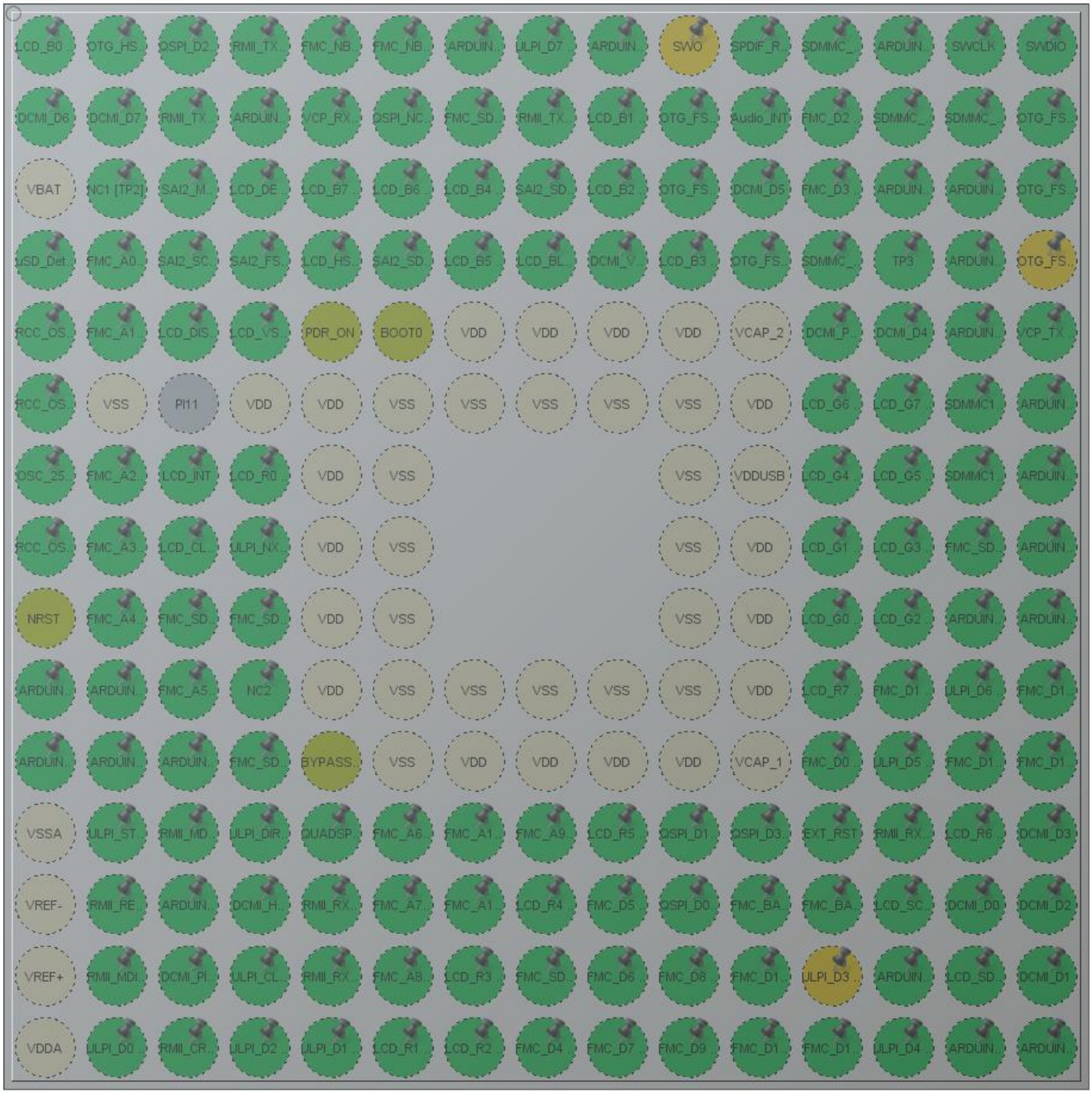
1.1. Project

Project Name	stm32f746g-discovery-project-stub
Board Name	32F746GDISCOVERY
Generated with:	STM32CubeMX 5.2.1
Date	07/18/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	LTDC_B0	LCD_B0 [RK043FN48H-CT672B_B0]
A2	PE3 *	I/O	GPIO_Input	OTG_HS_OverCurrent [STMPS2151STR_FAULT]
A3	PE2	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2]
A4	PG14	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
A5	PE1	I/O	FMC_NBL1	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
A6	PE0	I/O	FMC_NBL0	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
A7	PB8	I/O	I2C1_SCL	ARDUINO SCL/D15
A8	PB5	I/O	USB_OTG_HS_ULPI_D7	ULPI_D7 [USB3320C-EZK_D7]
A9	PB4	I/O	TIM3_CH1	ARDUINO PWM/D3
A10	PB3 **	I/O	SYS_JTDO-SWO	SWO
A11	PD7	I/O	SPDIFRX_IN0	SPDIF_RX0 [74LVC1G04SE_4]
A12	PC12	I/O	SDMMC1_CK	SDMMC_CK
A13	PA15	I/O	TIM2_CH1	ARDUINO PWM/D9
A14	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
A15	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
B1	PE5	I/O	DCMI_D6	DCMI_D6
B2	PE6	I/O	DCMI_D7	DCMI_D7
B3	PG13	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
B4	PB9	I/O	I2C1_SDA	ARDUINO SDA/D14
B5	PB7	I/O	USART1_RX	VCP_RX [STM32F103CBT6_PA2]
B6	PB6	I/O	QUADSPI_BK1_NCS	QSPI_NCS [N25Q128A13EF840E_S]
B7	PG15	I/O	FMC_SDNCAS	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
B8	PG11	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
B9	PJ13	I/O	LTDC_B1	LCD_B1 [RK043FN48H-CT672B_B1]
B10	PJ12 *	I/O	GPIO_Input	OTG_FS_VBUS
B11	PD6	I/O	GPIO_EXTI6	Audio_INT
B12	PD0	I/O	FMC_D2	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
B13	PC11	I/O	SDMMC1_D3	SDMMC_D3
B14	PC10	I/O	SDMMC1_D2	SDMMC_D2
B15	PA12	I/O	USB_OTG_FS_DP	OTG_FS_P
C1	VBAT	Power		
C2	PI8	I/O	RTC_TS	NC1 [TP2]
C3	PI4	I/O	SAI2_MCLK_A	SAI2_MCLKA [WM8994ECS/R_MCLK1]
C4	PK7	I/O	LTDC_DE	LCD_DE [RK043FN48H-CT672B_DE]
C5	PK6	I/O	LTDC_B7	LCD_B7 [RK043FN48H-CT672B_B7]
C6	PK5	I/O	LTDC_B6	LCD_B6 [RK043FN48H-CT672B_B6]
C7	PG12	I/O	LTDC_B4	LCD_B4 [RK043FN48H-CT672B_B4]
C8	PG10	I/O	SAI2_SD_B	SAI2_SDB [WM8994ECS/R_ADCDAT1]
C9	PJ14	I/O	LTDC_B2	LCD_B2 [RK043FN48H-CT672B_B2]
C10	PD5 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn [STMPS2141STR_EN]
C11	PD3	I/O	DCMI_D5	DCMI_D5
C12	PD1	I/O	FMC_D3	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
C13	PI3 *	I/O	GPIO_Output	ARDUINO D7
C14	PI2 *	I/O	GPIO_Output	ARDUINO D8
C15	PA11	I/O	USB_OTG_FS_DM	OTG_FS_N
D1	PC13 *	I/O	GPIO_Input	uSD_Detect
D2	PF0	I/O	FMC_A0	FMC_A0 [MT48LC4M32B2B5-6A_A0]
D3	PI5	I/O	SAI2_SCK_A	SAI2_SCKA [WM8994ECS/R_BCLK1]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D4	PI7	I/O	SAI2_FS_A	SAI2_FSA [WM8994ECS/R_LRCLK1]
D5	PI10	I/O	LTDC_HSYNC	LCD_HSYNC [RK043FN48H-CT672B_HSYNC]
D6	PI6	I/O	SAI2_SD_A	SAI2_SDA [WM8994ECS/R_DACDAT1]
D7	PK4	I/O	LTDC_B5	LCD_B5 [RK043FN48H-CT672B_B5]
D8	PK3 *	I/O	GPIO_Output	LCD_BL_CTRL [STLD40DPUR_EN]
D9	PG9	I/O	DCMI_VSYNC	DCMI_VSYNC
D10	PJ15	I/O	LTDC_B3	LCD_B3 [RK043FN48H-CT672B_B3]
D11	PD4 *	I/O	GPIO_Input	OTG_FS_OverCurrent [STMPS2141STR_Fault]
D12	PD2	I/O	SDMMC1_CMD	SDMMC_CMD
D13	PH15 *	I/O	GPIO_Input	TP3
D14	PI1	I/O	SPI2_SCK	ARDUINO SCK/D13
D15	PA10 **	I/O	USB_OTG_FS_ID	OTG_FS_ID
E1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	RCC_OSC32_IN
E2	PF1	I/O	FMC_A1	FMC_A1 [MT48LC4M32B2B5-6A_A1]
E3	PI12 *	I/O	GPIO_Output	LCD_DISP [RK043FN48H-CT672B_DISP]
E4	PI9	I/O	LTDC_VSYNC	LCD_VSYNC [RK043FN48H-CT672B_VSYNC]
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13 *	I/O	GPIO_Output	DCMI_PWR_EN
E13	PH14	I/O	DCMI_D4	DCMI_D4
E14	PI0	I/O	TIM5_CH4	ARDUINO PWM/CS/D5
E15	PA9	I/O	USART1_TX	VCP_TX [STM32F103CBT6_PA3]
F1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	RCC_OSC32_OUT

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	PK1	I/O	LTDC_G6	LCD_G6 [RK043FN48H-CT672B_G6]
F13	PK2	I/O	LTDC_G7	LCD_G7 [RK043FN48H-CT672B_G7]
F14	PC9	I/O	SDMMC1_D1	
F15	PA8	I/O	TIM1_CH1	ARDUINO PWM/D10
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	OSC_25M [NZ2520SB-25.00M_OUT]
G2	PF2	I/O	FMC_A2	FMC_A2 [MT48LC4M32B2B5-6A_A2]
G3	PI13	I/O	GPIO_EXTI13	LCD_INT
G4	PI15	I/O	LTDC_R0	LCD_R0 [RK043FN48H-CT672B_R0]
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	PJ11	I/O	LTDC_G4	LCD_G4 [RK043FN48H-CT672B_G4]
G13	PK0	I/O	LTDC_G5	LCD_G5 [RK043FN48H-CT672B_G5]
G14	PC8	I/O	SDMMC1_D0	
G15	PC7	I/O	USART6_RX	ARDUINO RX/D0
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	FMC_A3 [MT48LC4M32B2B5-6A_A3]
H3	PI14	I/O	LTDC_CLK	LCD_CLK [RK043FN48H-CT672B_CLK]
H4	PH4	I/O	USB_OTG_HS_ULPI_NXT	ULPI_NXT [USB3320C-EZK_NXT]
H5	VDD	Power		
H6	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H10	VSS	Power		
H11	VDD	Power		
H12	PJ8	I/O	LTDC_G1	LCD_G1 [RK043FN48H-CT672B_G1]
H13	PJ10	I/O	LTDC_G3	LCD_G3 [RK043FN48H-CT672B_G3]
H14	PG8	I/O	FMC_SDCLK	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
H15	PC6	I/O	USART6_TX	ARDUINO TX/D1
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	FMC_A4 [MT48LC4M32B2B5-6A_A4]
J3	PH5	I/O	FMC_SDNWE	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
J4	PH3	I/O	FMC_SDNE0	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J12	PJ7	I/O	LTDC_G0	LCD_G0 [RK043FN48H-CT672B_G0]
J13	PJ9	I/O	LTDC_G2	LCD_G2 [RK043FN48H-CT672B_G2]
J14	PG7 *	I/O	GPIO_Output	ARDUINO D4
J15	PG6 *	I/O	GPIO_Output	ARDUINO D2
K1	PF7	I/O	ADC3_IN5	ARDUINO A4
K2	PF6	I/O	ADC3_IN4	ARDUINO A5
K3	PF5	I/O	FMC_A5	FMC_A5 [MT48LC4M32B2B5-6A_A5]
K4	PH2 *	I/O	GPIO_Input	NC2
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
K12	PJ6	I/O	LTDC_R7	LCD_R7 [RK043FN48H-CT672B_R7]
K13	PD15	I/O	FMC_D1	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]
K14	PB13	I/O	USB_OTG_HS_ULPI_D6	ULPI_D6 [USB3320C-EZK_D6]
K15	PD10	I/O	FMC_D15	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
L1	PF10	I/O	ADC3_IN8	ARDUINO A1
L2	PF9	I/O	ADC3_IN7	ARDUINO A2
L3	PF8	I/O	ADC3_IN6	ARDUINO A3
L4	PC3	I/O	FMC_SDCKE0	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]
L13	PB12	I/O	USB_OTG_HS_ULPI_D5	ULPI_D5 [USB3320C-EZK_D5]
L14	PD9	I/O	FMC_D14	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
L15	PD8	I/O	FMC_D13	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
M1	VSSA	Power		
M2	PC0	I/O	USB_OTG_HS_ULPI_STP	ULPI_STP [USB3320C-EZK_STP]
M3	PC1	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ-TR_MDC]
M4	PC2	I/O	USB_OTG_HS_ULPI_DIR	ULPI_DIR [USB3320C-EZK_DIR]
M5	PB2	I/O	QUADSPI_CLK	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
M6	PF12	I/O	FMC_A6	FMC_A6 [MT48LC4M32B2B5-6A_A6]
M7	PG1	I/O	FMC_A11	FMC_A11 [MT48LC4M32B2B5-6A_A11]
M8	PF15	I/O	FMC_A9	FMC_A9 [MT48LC4M32B2B5-6A_A9]
M9	PJ4	I/O	LTDC_R5	LCD_R5 [RK043FN48H-CT672B_R5]
M10	PD12	I/O	QUADSPI_BK1_IO1	QSPI_D1 [N25Q128A13EF840E_DQ1]
M11	PD13	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3]
M12	PG3 *	I/O	GPIO_Output	EXT_RST
M13	PG2 *	I/O	GPIO_Input	RMII_RXER
M14	PJ5	I/O	LTDC_R6	LCD_R6 [RK043FN48H-CT672B_R6]
M15	PH12	I/O	DCMI_D3	DCMI_D3
N1	VREF-	Power		
N2	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
N3	PA0/WKUP	I/O	ADC3_IN0	ARDUINO A0
N4	PA4	I/O	DCMI_HSYNC	DCMI_HSYNC
N5	PC4	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
N6	PF13	I/O	FMC_A7	FMC_A7 [MT48LC4M32B2B5-6A_A7]
N7	PG0	I/O	FMC_A10	FMC_A10 [MT48LC4M32B2B5-6A_A10]
N8	PJ3	I/O	LTDC_R4	LCD_R4 [RK043FN48H-CT672B_R4]
N9	PE8	I/O	FMC_D5	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]
N10	PD11	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0]
N11	PG5	I/O	FMC_BA1	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]

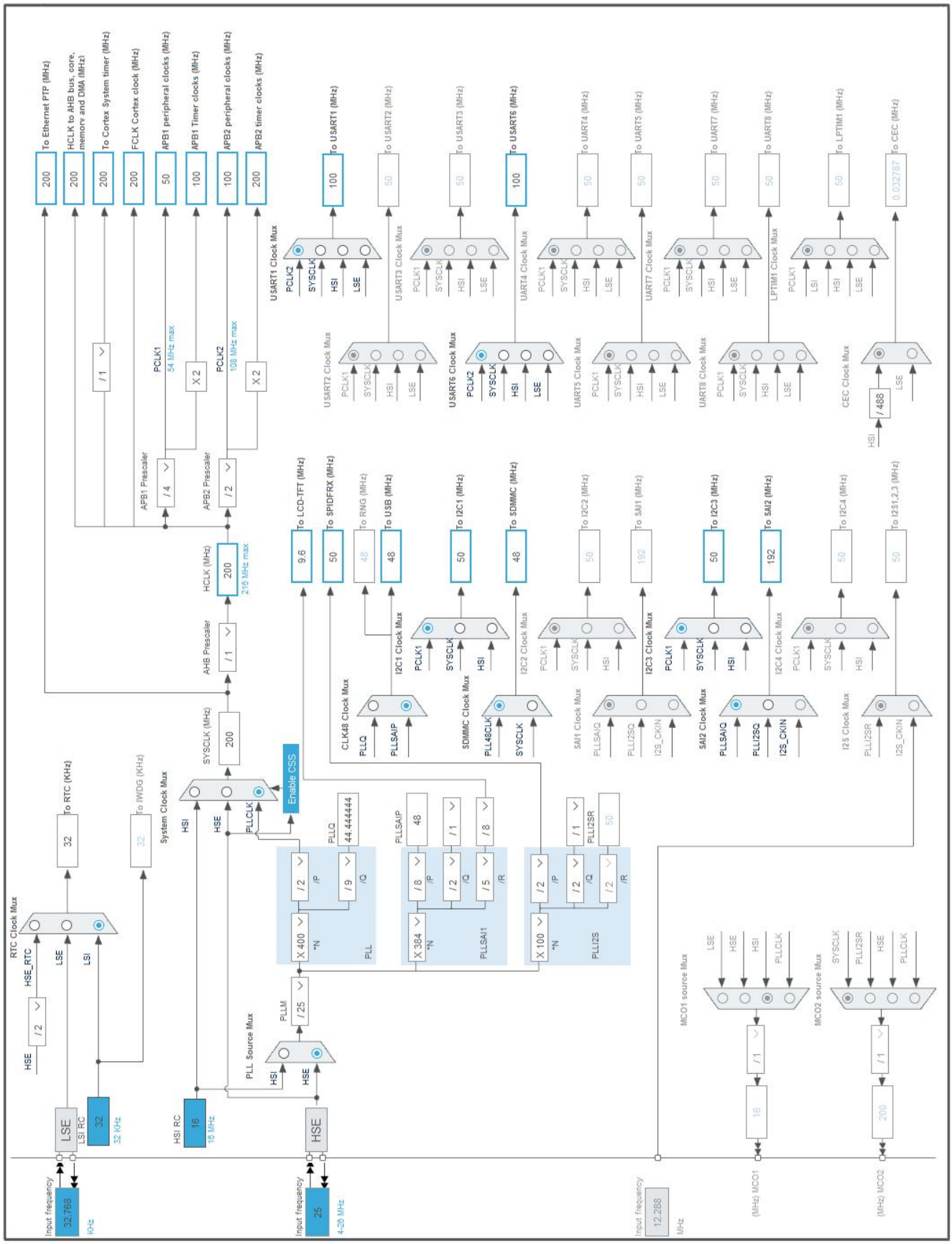
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N12	PG4	I/O	FMC_BA0	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
N13	PH7	I/O	I2C3_SCL	LCD_SCL [RK043FN48H-CT672B_SCL]
N14	PH9	I/O	DCMI_D0	DCMI_D0
N15	PH11	I/O	DCMI_D2	DCMI_D2
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
P3	PA6	I/O	DCMI_PIXCLK	
P4	PA5	I/O	USB_OTG_HS_ULPI_CK	ULPI_CLK [USB3320C-EZK_CLKOUT]
P5	PC5	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
P6	PF14	I/O	FMC_A8	FMC_A8 [MT48LC4M32B2B5-6A_A8]
P7	PJ2	I/O	LTDC_R3	LCD_R3 [RK043FN48H-CT672B_R3]
P8	PF11	I/O	FMC_SDNRAS	FMC_SDNRAS [MT48LC4M32B2B5-6A_RAS]
P9	PE9	I/O	FMC_D6	FMC_D6 [MT48LC4M32B2B5-6A_DQ6]
P10	PE11	I/O	FMC_D8	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
P11	PE14	I/O	FMC_D11	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
P12	PB10 **	I/O	USB_OTG_HS_ULPI_D3	ULPI_D3 [USB3320C-EZK_D3]
P13	PH6	I/O	TIM12_CH1	ARDUINO PWM/D6
P14	PH8	I/O	I2C3_SDA	LCD_SDA [RK043FN48H-CT672B_SDA]
P15	PH10	I/O	DCMI_D1	DCMI_D1
R1	VDDA	Power		
R2	PA3	I/O	USB_OTG_HS_ULPI_D0	ULPI_D0 [USB3320C-EZK_D0]
R3	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R4	PB1	I/O	USB_OTG_HS_ULPI_D2	ULPI_D2 [USB3320C-EZK_D2]
R5	PB0	I/O	USB_OTG_HS_ULPI_D1	ULPI_D1 [USB3320C-EZK_D1]
R6	PJ0	I/O	LTDC_R1	LCD_R1 [RK043FN48H-CT672B_R1]
R7	PJ1	I/O	LTDC_R2	LCD_R2 [RK043FN48H-CT672B_R2]
R8	PE7	I/O	FMC_D4	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
R9	PE10	I/O	FMC_D7	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
R10	PE12	I/O	FMC_D9	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]
R11	PE15	I/O	FMC_D12	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
R12	PE13	I/O	FMC_D10	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
R13	PB11	I/O	USB_OTG_HS_ULPI_D4	ULPI_D4 [USB3320C-EZK_D4]
R14	PB14	I/O	SPI2_MISO	ARDUINO MISO/D12
R15	PB15	I/O	SPI2_MOSI	ARDUINO MOSI/PWM/D11

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32f746g-discovery-project-stub
Project Folder	C:\work\stm32f746g-discovery-project-stub
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	027590_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC3

mode: IN0

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN8

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 4 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. CRC

mode: Activated

7.3.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.4. DCMI

DCMI: Slave 8 bits External Synchro

7.4.1. Parameter Settings:

Mode Config:

Pixel clock polarity	Active on Falling edge
Vertical synchronization polarity	Active Low
Horizontal synchronization polarity	Active Low
Frequency of frame capture	All frames are captured
JPEG mode	Disabled

Interface Capture Config:

Byte Select Mode	Interface captures all received bytes
Line Select Mode	Interface captures all received lines

7.5. DMA2D

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

7.6. ETH

Mode: RMII

7.6.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.6.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x00000FFF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.7. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

7.7.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits

Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.8. GFXSIMULATOR

7.8.1. Simulator Graphic:

7.9. I2C1

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00C0EAFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. I2C3

I2C: I2C

7.10.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00C0EAFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.11. LTDC

Display Type: RGB888 (24 bits)

7.11.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**41 ***
Horizontal Back Porch	**13 ***
Active Width	**480 ***
Horizontal Front Porch	**32 ***
HSync Width	40
Accumulated Horizontal Back Porch Width	53
Accumulated Active Width	533
Total Width	565

Synchronization for Height:

Vertical Synchronization Height	**10 ***
Vertical Back Porch	2
Active Height	**272 ***

Vertical Front Porch	2
VSync Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283
Total Height	285

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.11.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	**1 layer ***

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**272 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB565 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 0 - Blending Factor2	**Alpha constant x Pixel Alpha ***

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	**0xC0000000 ***
Layer 0 - Color Frame Buffer Line Length (Image Width)	**480 ***

Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**272 ***

7.12. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.12.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.13. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.13.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.14. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

Alarm B: Internal Alarm B

mode: Timestamp

7.14.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset
Hours	0
Minutes	0
Seconds	0

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Alarm B:

Hours	0
Minutes	0
Seconds	0

Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Time Stamp:

Time Stamp Pin Edge	Time Stamp occurs on the Rising edge

7.15. SAI2

Mode: Master with Master Clock Out

Mode: Synchronous Slave

7.15.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Basic Parameters	
Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	8 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Parameters	
Master Clock Divider	Enabled

Audio Frequency	192 KHz
Real Audio Frequency	0
Error between Selected	0
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

SAI B:

Synchronization Inputs	**Synchronous with other block of same SAI ***
Basic Parameters	
Protocol	Free
Audio Mode	Slave Receive
Frame Length (only Even Values)	24
Data Size	8 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Parameters	
Real Audio Frequency	0
Error between Selected	0
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

7.16. SDMMC1

Mode: SD 4 bits Wide bus

7.16.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.17. SPDIFRX

mode: IN0 Selection

7.17.1. Parameter Settings:

Pinout Selection:

Selected Input	IN0

IP Clocking and Limitation:

SPDIF Clock	5.0E7
Max Frequency Supported for Incoming Audio Stream	71023

Synchronization Configuration:

Wait For Activity	The SPDIF-RX does not wait for activity on SPDIF_IN line before performing the synchronization
Retries	No re-try is allowed (only one attempt)

Channel Status Register Formatting:

Channel Selection	The control flow will take the channel status from channel A

Data Register Formatting : Data Format:

Data Format	Data samples are aligned in the right (LSB)
Stereo Mode (used in case of overrun to handle misalignement)	The peripheral is in MONO mode

Data Register Formatting : Mixing Data and Control:

Preamble Type Mask	The preamble type bits are copied into the SPDIF_DR
Channel Status Mask	The channel status and user bits are copied into the SPDIF_DR
Validity Bit Mask	The validity bit is copied into the SPDIF_DR
Parity Error Mask	The parity error bit is copied into the SPDIF_DR

7.18. SPI2

Mode: Full-Duplex Master

7.18.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.19. SYS

Debug: Serial Wire

Timebase Source: TIM6

7.20. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable

BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.21. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.22. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.23. TIM5

mode: Clock Source

Channel4: PWM Generation CH4

7.23.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0

Fast Mode	Disable
CH Polarity	High

7.24. TIM8

Clock Source : Internal Clock

7.24.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

7.25. TIM12

Channel1: PWM Generation CH1

7.25.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.26. USART1

Mode: Asynchronous

7.26.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.27. USART6

Mode: Asynchronous

7.27.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.28. USB_OTG_FS

Mode: Host_Only

7.28.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Signal start of frame	Disabled

7.29. FATFS

mode: User-defined

7.29.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8

FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

7.30. FREERTOS

Interface: CMSIS_V1

7.30.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	

	Enabled *
USE_COUNTING_SEMAPHORES	**Enabled ***
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	**Enabled ***
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**32768 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.30.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled

vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.31. USB_HOST

Class for FS IP: Communication Host Class (Virtual Port Com)

7.31.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	2
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Enabled
USBH_PROCESS_PRIO (The CMSIS-RTOS osPriority value specifies the priority for the USB Host thread)	priority: normal (default)
USBH_PROCESS_STACK_SIZE (The CMSIS-RTOS stack size requirements in words)	128

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PF7	ADC3_IN5	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A4
	PF6	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A5
	PF10	ADC3_IN8	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A1
	PF9	ADC3_IN7	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A2
	PF8	ADC3_IN6	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A3
	PA0/WKUP	ADC3_IN0	Analog mode	No pull-up and no pull-down	n/a	ARDUINO A0
DCMI	PE5	DCMI_D6	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D6
	PE6	DCMI_D7	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D7
	PD3	DCMI_D5	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D5
	PG9	DCMI_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_VSYNC
	PH14	DCMI_D4	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D4
	PH12	DCMI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D3
	PA4	DCMI_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_HSYNC
	PH9	DCMI_D0	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D0
	PH11	DCMI_D2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D2
	PA6	DCMI_PIXCLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	DCMI_D1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DCMI_D1
ETH	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_MDIO [LAN8742A-CZ-TR_MDIO]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	RMII_CRS_DV

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	[LAN8742A-CZ-TR_CRS_DV]
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A0 [MT48LC4M32B2B5-6A_A0]
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A1 [MT48LC4M32B2B5-6A_A1]
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A2 [MT48LC4M32B2B5-6A_A2]
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A3 [MT48LC4M32B2B5-6A_A3]
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A4 [MT48LC4M32B2B5-6A_A4]
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A5 [MT48LC4M32B2B5-6A_A5]
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A6 [MT48LC4M32B2B5-6A_A6]
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A11 [MT48LC4M32B2B5-6A_A11]
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A9 [MT48LC4M32B2B5-6A_A9]
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A7 [MT48LC4M32B2B5-6A_A7]
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A10 [MT48LC4M32B2B5-6A_A10]
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A8 [MT48LC4M32B2B5-6A_A8]
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNRAS [MT48LC4M32B2B5-6A_RAS]
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D6 [MT48LC4M32B2B5-

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						6A_DQ6]
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	ARDUINO SCL/D15
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	ARDUINO SDA/D14
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	LCD_SCL [RK043FN48H-CT672B_SCL]
	PH8	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	LCD_SDA [RK043FN48H-CT672B_SDA]
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B0 [RK043FN48H-CT672B_B0]
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B1 [RK043FN48H-CT672B_B1]
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_DE [RK043FN48H-CT672B_DE]
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B7 [RK043FN48H-CT672B_B7]
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B6 [RK043FN48H-CT672B_B6]
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B4 [RK043FN48H-CT672B_B4]
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B2 [RK043FN48H-CT672B_B2]
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_HSYNC

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						[RK043FN48H-CT672B_HSYNC]
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B5 [RK043FN48H-CT672B_B5]
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B3 [RK043FN48H-CT672B_B3]
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_VSYNC [RK043FN48H-CT672B_VSYNC]
	PK1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G6 [RK043FN48H-CT672B_G6]
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G7 [RK043FN48H-CT672B_G7]
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R0 [RK043FN48H-CT672B_R0]
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G4 [RK043FN48H-CT672B_G4]
	PK0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G5 [RK043FN48H-CT672B_G5]
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_CLK [RK043FN48H-CT672B_CLK]
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G1 [RK043FN48H-CT672B_G1]
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G3 [RK043FN48H-CT672B_G3]
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G0 [RK043FN48H-CT672B_G0]
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G2 [RK043FN48H-CT672B_G2]
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R7 [RK043FN48H-CT672B_R7]
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R5 [RK043FN48H-CT672B_R5]
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R6 [RK043FN48H-CT672B_R6]
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R4 [RK043FN48H-CT672B_R4]
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R3 [RK043FN48H-CT672B_R3]
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R1 [RK043FN48H-CT672B_R1]
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R2 [RK043FN48H-CT672B_R2]
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D2 [N25Q128A13EF840E_DQ

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						2]
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_NCS [N25Q128A13EF840E_S]
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D1 [N25Q128A13EF840E_DQ1]
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D3 [N25Q128A13EF840E_DQ3]
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D0 [N25Q128A13EF840E_DQ0]
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	RCC_OSC32_IN
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	RCC_OSC32_OUT
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_25M [NZ2520SB-25.00M_OUT]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
RTC	PI8	RTC_TS	n/a	n/a	n/a	NC1 [TP2]
SAI2	PI4	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_MCLKA [WM8994ECS/R_MCLK1]
	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SDB [WM8994ECS/R_ADCDAT1]
	PI5	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SCKA [WM8994ECS/R_BCLK1]
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_FSA [WM8994ECS/R_LRCLK1]
	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SDA [WM8994ECS/R_DACDAT1]
SDMMC1	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_CK
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_D3
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_D2
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_CMD
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPDIFRX	PD7	SPDIFRX_IN0	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPDIF_RX0 [74LVC1G04SE_4]
SPI2	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO SCK/D13

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO MISO/D12
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO MOSI/PWM/D11
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/D10
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/D9
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/D3
TIM5	PI0	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/CS/D5
TIM12	PH6	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARDUINO PWM/D6
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	VCP_RX [STM32F103CBT6_PA2]
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	VCP_TX [STM32F103CBT6_PA3]
USART6	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARDUINO RX/D0
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARDUINO TX/D1
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OTG_FS_P
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OTG_FS_N
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OTG_FS_ID
	PB10	USB_OTG_HS_ULPI_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ULPI_D3 [USB3320C-EZK_D3]
GPIO	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_HS_OverCurrent [STMPS2151STR_FAULT]
	PJ12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_VBUS
	PD6	GPIO_EXTI6	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	Audio_INT
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn [STMPS2141STR_EN]
	PI3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARDUINO D7
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARDUINO D8
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	uSD_Detect

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PK3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_CTRL [STLD40DPUR_EN]
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent [STMPS2141STR_Fault]
	PH15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TP3
	PI12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DISP [RK043FN48H-CT672B_DISP]
	PH13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DCMI_PWR_EN
	PI13	GPIO_EXTI13	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	LCD_INT
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARDUINO D4
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARDUINO D2
	PH2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	NC2
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXT_RST
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RMII_RXER

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
USB On The Go FS global interrupt	true	5	0
LTDC global interrupt	true	5	0
DMA2D global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
RTC tamper and timestamp interrupts through EXTI line 21	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
RTC alarms (A and B) interrupt through EXTI line 17	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
FMC global interrupt	unused		
SDMMC1 global interrupt	unused		
TIM5 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
DCMI global interrupt	unused		
FPU global interrupt	unused		
LTDC global error interrupt	unused		
SAI2 global interrupt	unused		
QUADSPI global interrupt	unused		
SPDIF-RX global interrupt	unused		

*** User modified value**

9. Software Pack Report