# Design Example: CMOS Differential-pair with Constant-gm Biasing, FREEPDK45

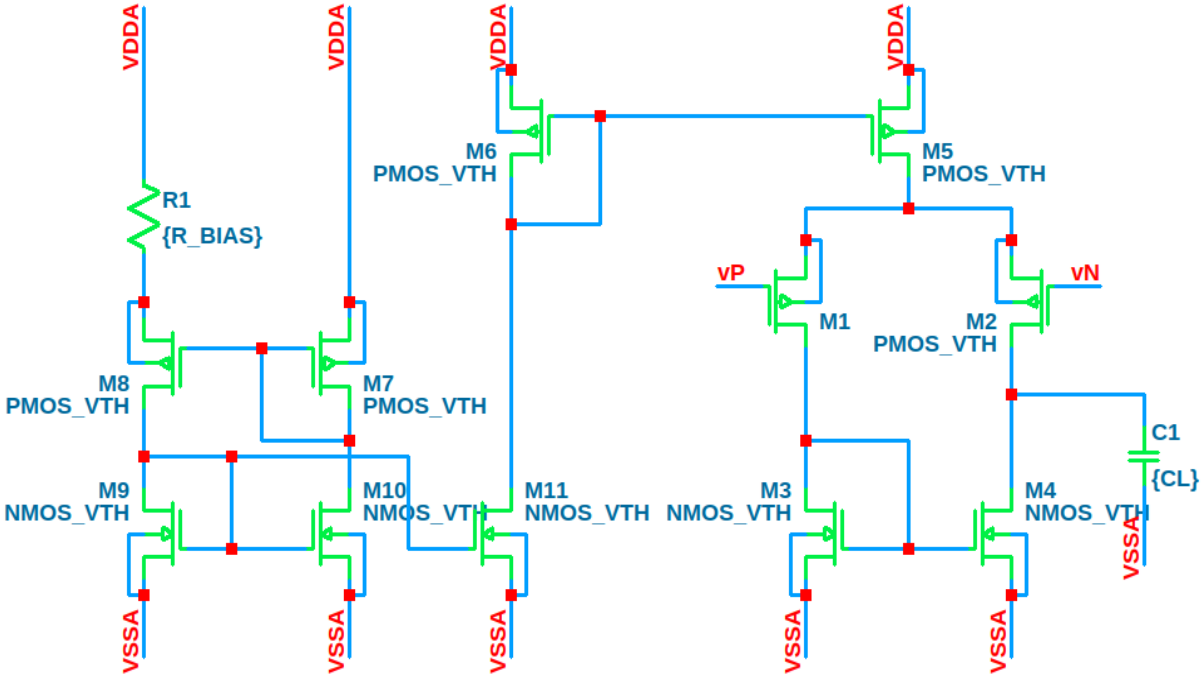


*Figure 1: Diff-pair with Constant-gm Biasing*

Specifications:

VDD = 1.8V, GBW = 120e6 Hz, $C_L$ = 10 pF, with freePDK45 process node technology

$$-V_P - V_{SG} - V_{SDsat} + V_{DDA} = 0 \text{ and } -V_P - V_{SG} + V_{SDsat} + V_{GS} = 0$$

$$V_{GS} - V_{SG} + V_{SDsat} < V_{\text{IN,CM}} < V_{DDA} - V_{SG} - V_{SDsat}$$

→ Start with M1 (and M2)

- From $C_L$ and GBW: $g_{\text{m,M1}} = 2\pi f_u(1+0.2)C_L = 2\pi \cdot 120\text{e}6 \cdot 1.2 \cdot 10\text{e-}12 = 9.04\text{e-}3\,S$ , where the factor 0.2 is to capture some parasitic capacitance

- Since we don't have a specific power consumption spec here, we pick $g_m/I_D = 15$ (MI) for M1 since it is a gain stage

$$I_D = \frac{g_{\text{m,M1}}}{g_m/I_D} = \frac{9\text{e-}3}{15} = 603.18\,uA$$

- From $I_D/W \; vs \; g_m/I_D \; plot(LUT)$ of PMOS, we determine (there could be some other different candidates)

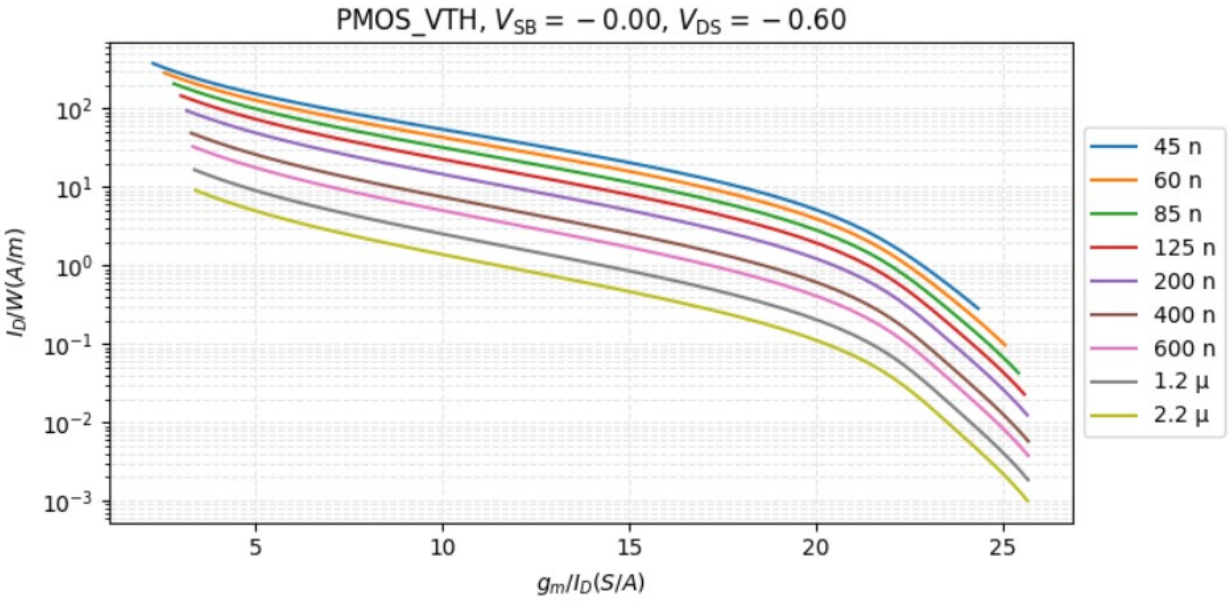


*Figure 2:* $I_D/W$ *vs* $g_m/I_D$ *plot* $(LUT)$ *of PMOS*

$$for\ L=125\,nm, g_m/I_D=15\ we\ have \frac{I_D}{W}=7.96$$

$$W_{M1}=\frac{I_D}{J_D}=\frac{603\text{e-}6}{7.96}=75.75\,um$$

(If you have any DC gain requirement, you can increase $L_{M1}$ by looking at $g_m/g_{ds}\ vs.\ g_m/I_D\ plot$ , which will give you a new $W_{M1}$.)

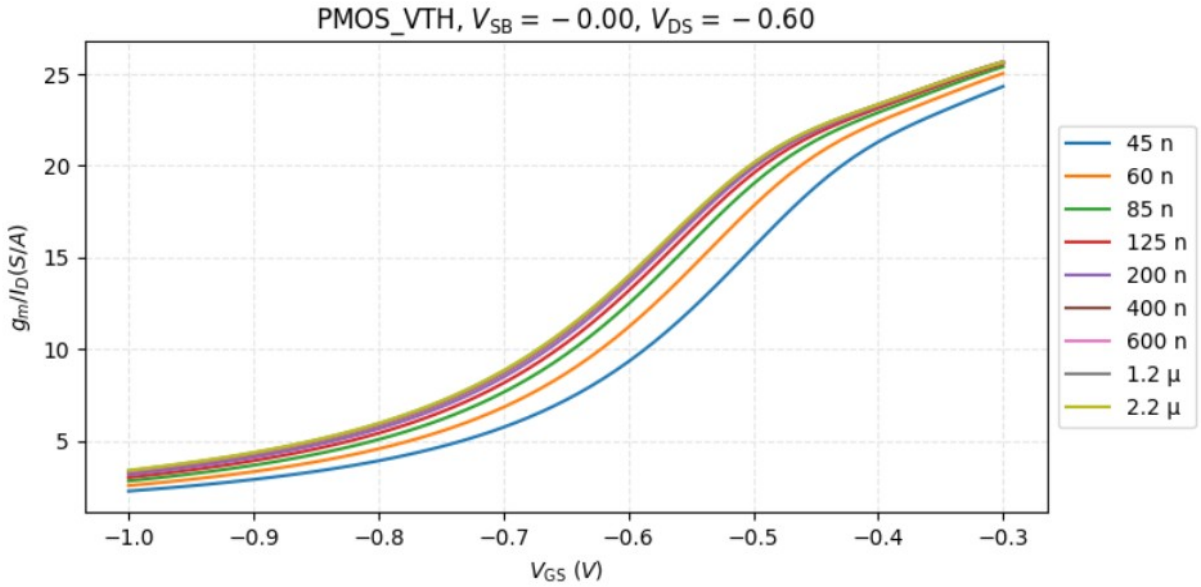


*Figure 3:* $g_m/I_D\ vs\ V_{SG}$

$$\text{from } g_m/I_D=15\ vs\ V_{GS}\ for\ L=125\,nm \rightarrow V_{GS}=-0.572\,V$$

→ Second, we design M3 (and M4)

- Since we don't have a specific power consumption spec here, we pick $g_m/I_D=10$ for M3 since it is an active load (source), so it should be smaller

- Since we know $I_{D,M3}=I_{D,M1}=603\,uA$ already from the calculation of M1, from $I_D/W\,vs\,g_m/I_D\,plot\,(LUT)\,of\,NMOS$, we determine (there could be some other candidates)

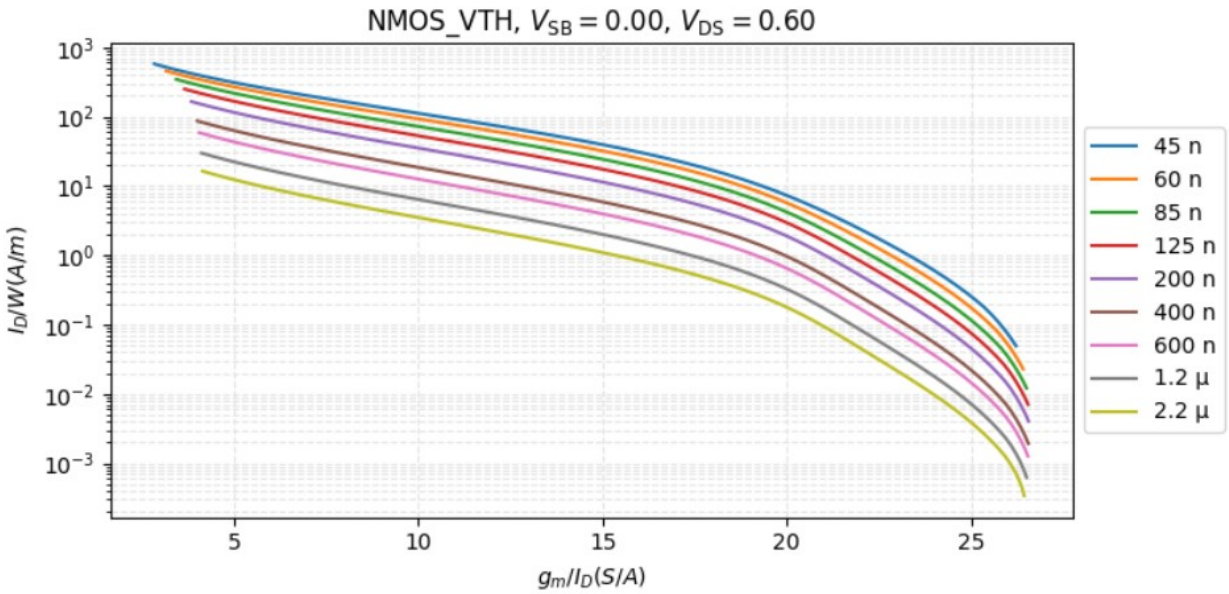


*Figure 4:* $I_D/W\,vs\,g_m/I_D\,plot\,(LUT)\,of\,NMOS$

$$for\,L=600\,nm, g_m/I_D=10, we\,have\,I_D/W=12.54$$

$$W_{M3}=\frac{I_D}{J_D}=\frac{603\text{e-}6}{12.54}=48.08\,um$$

The active load and current source should have larger output impedance, therefore L is intentionally picked larger value.

→ Third, we design current mirror M5 (and M6)

- For simplicity here, we assume M5 and M6 have the same dimension (can be scaled down later for reducing power consumption(

- Since we don't have a specific power consumption here, we pick $g_m/I_D=4\,for$ M5 since it is active load (source), a device whose $g_m$ does not contribute to gain and should have a good matching we pick the transonductance effficeiency in SI (The mismatch is independent of transistor width in strong inversion. The only way to improve the matching is to employ a longer channel.)

The $g_m/I_D$ is even smaller than M3's since here, $I_{D,M5}=2I_{D,M3}$, smaller $g_m/I_D$ can give larger L values, which is desirable for current mirror design

- Since we know $I_{D,M5}=2I_{D,M1}=1.2\text{e-}3\,A$, already from the calculation of M1, from $I_D/W\,vs\,g_m/I_D\,plot\,(LUT)\,of\,PMOS$ Figure 2 we determine (there could be some other different candidates)

$for\ L = 1.2\text{e-}6, g_m/I_D = 4\ we\ have\ I_D/W = 12.93$

$$W_{M5,6} = \frac{I_D}{J_D} = \frac{1.2\text{e-}3}{12.93} = 92.8\ um$$

Now, we can start designing the constant-gm biasing block

Analysis:

## → NMOS implementation of constant-$g_m$ biasing circuit

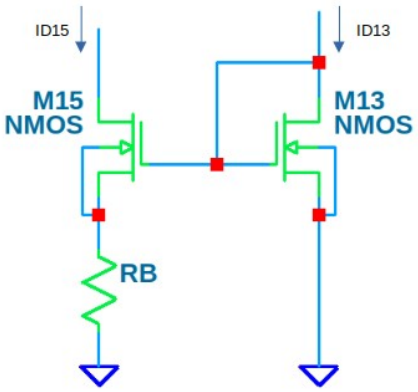


*Figure 5: NMOS implementation*

## → PMOS implementation of constant-$g_m$ biasing

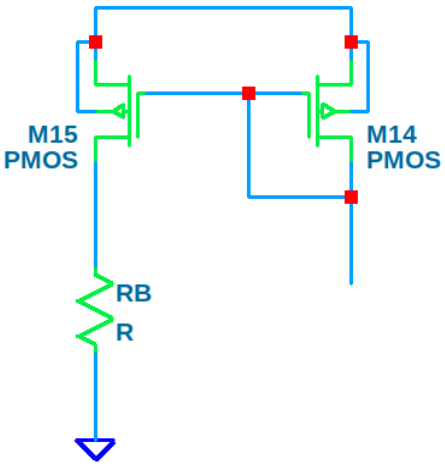


*Figure 6: PMOS implentation*

## Analysis:

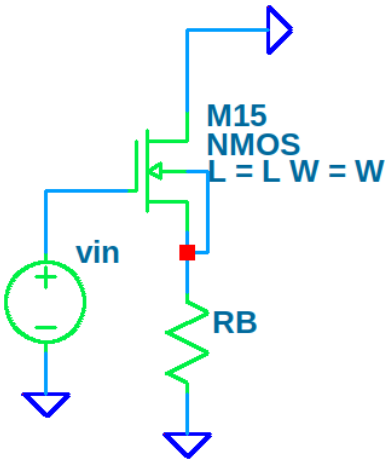


*Figure 7: $G_m$ of NMOS with $R_B$ in source*

→ an analysis of the M15 and $R_B$ subcircuit from Figure 5, shown in Figure 7 will show that $G_m$ of this circuit is equal to $1/R_B$

$$G_m = \frac{i_{out}}{v_{in}}$$

$$i_{out} - gmv_{gs} = 0 \rightarrow i_{out} = gmv_{gs}$$

$$-R_B i_{out} - v_{gs} + v_{in} = 0 \rightarrow v_{in} = R_B i_{out} + v_{gs}$$

$$\rightarrow G_m = \frac{gmv_{gs}}{R_B i_{out} + v_{gs}} = \frac{gmv_{gs}}{R_B gmv_{gs} + v_{gs}} \approx 1/R_B$$

→ **to keep gm constant in Figure 5 we need** $gm_{13} = 1/R_B$ **, this way if we can select gm through** $g_m/I_D$ **, we can set $R_B$ to give us a specific current for biasing our amplifier**

Now we will analyse Figure 5, to get the needed aspect ratios to have $gm_{13} = 1/R_B$ :

$$-R_B I_{D15} - V_{GS15} + V_{GS13} = 0$$

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}}, strong\,inversion, square-law\,design$$

$$if\ I_{D15} = I_{D13}$$

$$R_B I_D = \sqrt{\frac{2 I_D}{k_n' \frac{W_{13}}{L_{13}}}} - \sqrt{\frac{2 I_D}{k_n' \frac{W_{15}}{L_{15}}}}$$

*we need* $g_m = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D} = \frac{1}{R_B}$ in *strong inversion , with square − law design*

$$R_B I_D = \sqrt{2 I_D} \left| \frac{1}{\sqrt{k_n' \frac{W_{13}}{L_{13}}}} - \frac{1}{\sqrt{k_n' \frac{W_{15}}{L_{15}}}} \right|^2$$

$$\rightarrow R_B^2 I_D^2 = 2 I_D \left| \frac{1}{k_n' \frac{W_{13}}{L_{13}}} + \frac{1}{k_n' \frac{W_{15}}{L_{15}}} - 2 \frac{1}{k_n' \sqrt{\frac{W_{13}}{L_{13}} \frac{W_{15}}{L_{15}}}} \right| \cdot k_n'$$

$$\rightarrow k_n' R_B^2 I_D = 2 \left( \frac{1}{\frac{W_{13}}{L_{13}}} + \frac{1}{\frac{W_{15}}{L_{15}}} - 2 \frac{1}{\sqrt{\frac{W_{13}}{L_{13}} \frac{W_{15}}{L_{15}}}} \right)$$

*here the* right *hand element , i . e .,* $2 \left( \frac{1}{\frac{W_{13}}{L_{13}}} + \frac{1}{\frac{W_{15}}{L_{15}}} - 2 \frac{1}{\sqrt{\frac{W_{13}}{L_{13}} \frac{W_{15}}{L_{15}}}} \right)$ *, must be equal* to $\frac{1}{2 \frac{W_{13}}{L_{13}}}$

*so that* $g_m = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D} = \frac{1}{R_B}$

$$\rightarrow 2 \left( \frac{1}{\frac{W_{13}}{L_{13}}} + \frac{1}{\frac{W_{15}}{L_{15}}} - 2 \frac{1}{\sqrt{\frac{W_{13}}{L_{13}} \frac{W_{15}}{L_{15}}}} \right) = \frac{1}{2 \frac{W_{13}}{L_{13}}}$$

and *after furher algebraic analysis we find* $4 \frac{W_{13}}{L_{13}} = \frac{W_{15}}{L_{15}}$

$$\rightarrow k_n' R_B^2 I_D = 2 \left( \frac{1}{\frac{W_{13}}{L_{13}}} + \frac{1}{4 \frac{W_{13}}{L_{13}}} - 2 \frac{1}{\sqrt{\frac{W_{13}}{L_{13}} 4 \frac{W_{13}}{L_{13}}}} \right)$$

$$\rightarrow k_n' R_B^2 I_D = 2 \left( \frac{4+1}{4 \frac{W_{13}}{L_{13}}} - 2 \frac{1}{2 \frac{W_{13}}{L_{13}}} \right) = \frac{10}{4 \frac{W_{13}}{L_{13}}} - \frac{2}{\frac{W_{13}}{L_{13}}} = \frac{10-8}{4 \frac{W_{13}}{L_{13}}} = \frac{1}{2 \frac{W_{13}}{L_{13}}}$$

$$\rightarrow 2 k_n' \frac{W_{13}}{L_{13}} I_D = \frac{1}{R_B^2} \Big|^{\sqrt{2}} \rightarrow \sqrt{2 k_n' \frac{W_{13}}{L_{13}} I_D} = \frac{1}{R_B}$$

We arrive at, $g_{\mathrm{m,M7}} = 1/R_{BIAS}$ *if* $W_{M8} = 4 W_{M7}$ , where this were calculated as with long channels and strong-inversion equations.

If we let M1 and M7 have the same size, and if we can somehow let M1 and M7 have the same $g_m$, then their $I_D$ will also be the same.

Design $R_{BIAS}$:

Letting $g_{m1}=g_{m7}: g_{m1}=g_m/I_D \cdot I_{d,M1}=9e\text{-}3\,S$

$$R_{BIAS}=\frac{1}{g_{m7}}=111\,\Omega$$

→ Design M7 (and M8)

- Simply copying M1 to M7: $W_{M1}=W_{M7}=75.75\,um\,; L_{M1}=L_{M7}=125\,nm$

- Rather than making $W_{M8}=4\,W_{M7}$, we can let $W_{M8}=W_{M7}$ and use multiplier $M_{M8}=4\,M_{M7}$ (you can aproximate its value by SPICE simulations, as the equations used for this example are not accurate)

→ Design M9 (M10 and M11)

- Simply copying M3 to M9, M10

- For M11 we simply double the width of M9

- If necessary you can increase L of M9, M10 and M11 to increase the output resistance of current mirror, ensuring you are always operating them in saturation region.

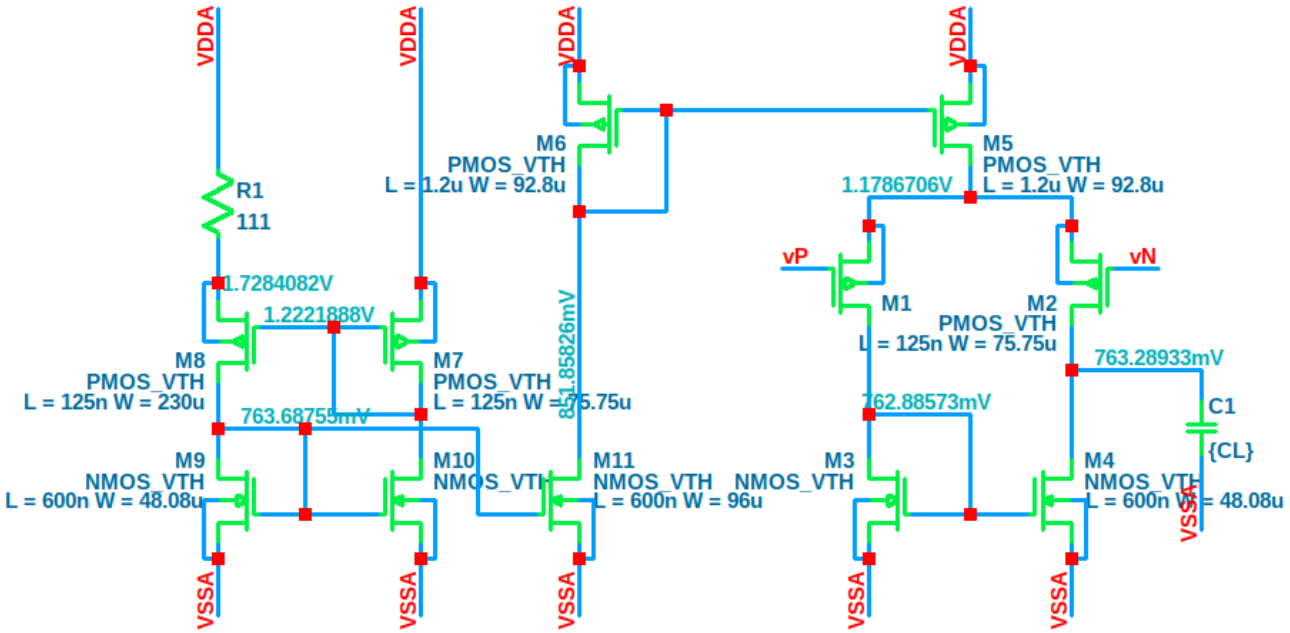


*Figure 8: Diff-Amp with Aspect Ratios for GBW ~120 MHz with freePDK45*

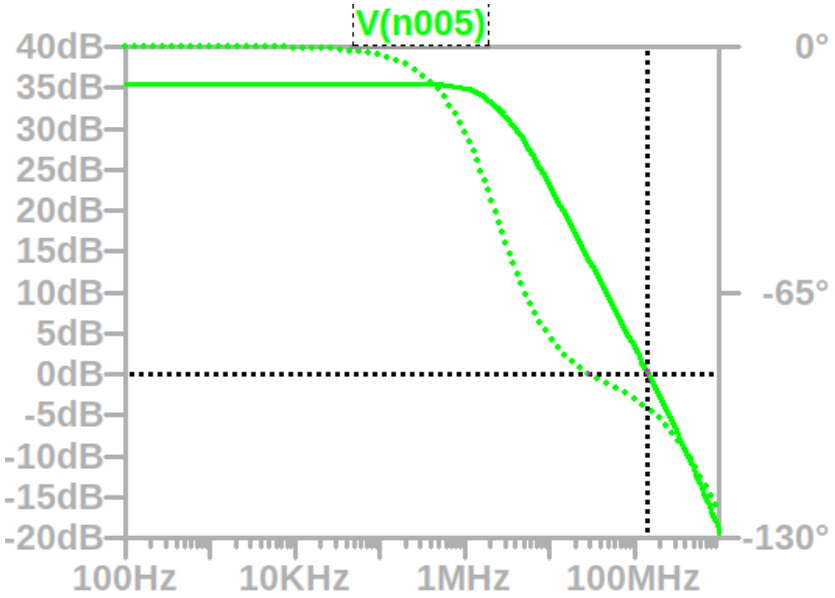


*Figure 9: GBW representation ~ 120 MHz*

# Appendix

Note: If you are designing by Av0 as a specification parameter, then L and $g_m/I_D$ will play a significant role as seen in Figure 10, where

$$A_{v0}=\frac{g_{m1}}{g_{ds2}+g_{ds4}}$$

$$\rightarrow A_{v0}=\frac{g_{m1}/I_D}{\frac{g_{ds2}}{I_D}+\frac{g_{ds4}}{I_D}}$$

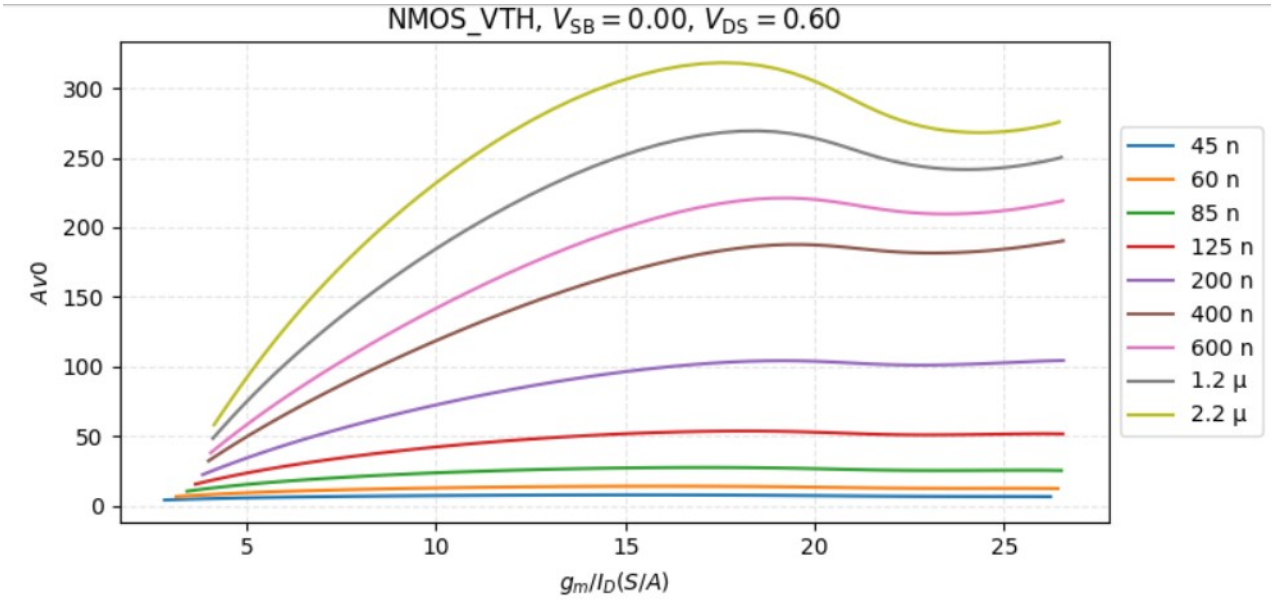


*Figure 10:* $A_{v0}$ *vs* $(g_m/I_D)$

Av0 will also tradeoff with ft Figure 11, and implicitly fu of the circuit:

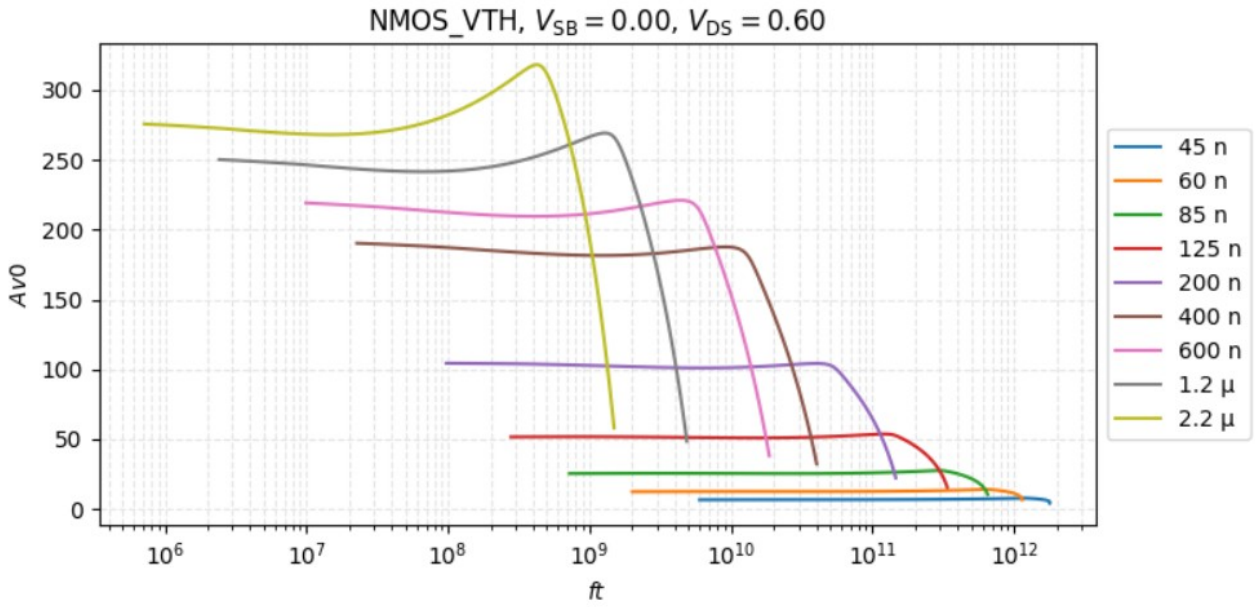


*Figure 11:* $A_{v0} vs f_t$