

## **Analysis**

 $V_A$  -  $V_B$  potential difference is given by:

$$-V_{A}-V_{GS3}+V_{GS4}+V_{B}=0$$

$$then V_A - V_B = V_{GS4} - V_{GS3} = \left(V_T + \sqrt{\frac{2I_{D4}}{K_4}}\right) - \left(V_T + \sqrt{\frac{2I_{D3}}{K_3}}\right) = \sqrt{\frac{2I_{D4}}{K_4}}\left(1 - \sqrt{\frac{I_{D3}}{I_{D4}}}\frac{K_4}{K_3}\right)$$

where 
$$K = \mu C_{ox} \frac{W}{L}$$

Because of the current mirror M5 – M6 we can write:

$$\frac{I_{D3}}{I_{D4}} = \frac{I_{D5}}{I_{D6}} = \frac{K_5}{K_6}$$

so 
$$V_A - V_B = \sqrt{\frac{2I_{D4}}{K_4}} \left( 1 - \sqrt{\frac{K_5}{K_6} \frac{K_4}{K_3}} \right)$$

The condition to make the  $V_A - V_B$  difference equal to zero is:

$$K_4 K_5 = K_3 K_6$$

equivalent with:

$$\left(\frac{W}{L}\right)_{4} \left(\frac{W}{L}\right)_{5} = \left(\frac{W}{L}\right)_{3} \left(\frac{W}{L}\right)_{6}$$

Because  $K_4K_5=K_3K_6$ ,  $V_A=V_B$  we get:

$$-V_{EB1} + I_3 R_3 = 0 \rightarrow I_3 = I_4 = \frac{V_{EB1}}{R_{3,4}}$$

I<sub>1</sub> current expression is given by:

$$-V_{EB2} - I_1 R_1 + V_{EB1} = 0 \Rightarrow I_1 = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{kT}{q R_1} \ln \left( \frac{I_{S2}}{I_{S1}} \frac{I_{C1}}{I_{C2}} \right)$$

Knowing:

$$I_{D5} - I_3 - I_{C1} = 0 \rightarrow I_{C1} = I_{D5} - I_3$$

and:

$$I_{D6} - I_4 - I_{C2} = 0 \rightarrow I_{C2} = I_{D6} - I_4$$

with  $T_5$  and  $T_6$  being identical,  $I_{D5} = I_{D6}$  so  $I_{C1} = I_{C2}$ , resulting:

$$I_1 = \frac{kT}{qR_1} \ln \left( \frac{I_{S2}}{I_{S1}} \right)$$

The reference voltage Vref is:

$$\begin{split} V_{\mathit{Ref}}(T) &= (I_1 + I_4) R_2 = \frac{R_2}{R_1} \frac{kT}{q} \ln \left( \frac{I_{\mathit{S2}}}{I_{\mathit{S1}}} \right) + \frac{R_2}{R_4} V_{\mathit{EB1}}(T) \\ V_{\mathit{Ref}}(T) &= \frac{R_2}{R_1} \frac{kT}{q} \ln \left( \frac{I_{\mathit{S2}}}{I_{\mathit{S1}}} \right) + \frac{R_2}{R_4} \left[ E_{\mathit{G0}} + \frac{V_{\mathit{BE}}(T_0) - E_{\mathit{G0}}}{T_0} T + (1 - \eta) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right) \right] \end{split}$$

To produce a correction of first order on the temperature characteristic voltage reference, implies to cancel the linear temperature dependent parameters:

$$\frac{k}{q R_1} \ln \left( \frac{I_{S2}}{I_{S1}} \right) + \frac{V_{BE}(T_0) - E_{G0}}{R_4 T_0} = 0$$

Giving us:

$$V_{Ref}(T) = \frac{R_2}{R_4} \left[ E_{G0} + (1 - \eta) \frac{kT}{q} \ln \left( \frac{T}{T_0} \right) \right]$$

## Design

All MOS transistors have identical aspect ratios, the bipolar saturation currents ratio  $I_{S2}/I_{S1}=100,\ V_{EB1}(T_0)=0.6\ V,\ R_3=R_4.$ 

The linear temperature correction characteristic of Vref implies respecting the following relation:

$$\begin{split} \frac{k}{q\,R_1} \ln\!\left(\!\frac{I_{S2}}{I_{S1}}\!\right) + & \frac{V_{BE}(T_0) - E_{G0}}{R_4 T_0} \! = \! 0 \\ \text{from which we get} & \frac{R_4}{R_1} \! = \! \frac{E_{G0} \! - \! V_{\text{BE}}(T_0)}{\frac{k\,T_0}{q} \ln\!\left(\!\frac{I_{S2}}{I_{S1}}\!\right)} \! = \! \frac{1.2 \! - \! 0.6}{\frac{1.38 \text{e-} 23 \! \cdot \! 273}{1.6 \text{e-} 19} \ln(100)} \! = \! 5.54 \end{split}$$

Selecting  $R_1 = 8k$  we get

$$R_4 = 5.54 \cdot 8e3 = 44e3 \Omega$$

From the voltage – current relationship of MOS transistors in saturation we get:

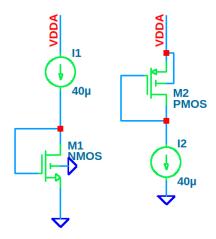
$$I_{D3,4} = \frac{Kn'}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_{D5,6} = \frac{Kp'}{2} \frac{W}{L} (V_{SG} - |V_T|)^2$$

$$\frac{W}{L} = \frac{2I_D}{K'(V_{GS} - V_T)^2}$$

## → an easier way to design is by using NMOS and PMOS references

We will start by using the following reference set (MOSFET model file 180 nm TSMC process):



The references have been selected to have the following characteristics:

	NREF	PREF
L [m]	180e-9	180e-9
W [m]	2e-6	6e-6
ID [A]	40e-6	40e-6
Vov [V]	127e-3	153e-3
Vth [V]	486e-3	520e-3
Gm [A/V]	496e-6	447e-6
Rds [Ohm]	80.6e3	108e3

We want to design for:

	NMOS	PMOS
L [m]	2e-6	2e-6
ID	32e-6	32e-6
Vov	140e-3	140e-3

Using our references we get the following parameters:

	NMOS	PMOS
L [m]	2e-6	2e-6
W [m]	14.6e-6	63.7e-6
ID [A]	32e-6	32e-6
Vov [V]	140e-3	140e-3
Gm [A/V]	360e-6	390e-6

## SPICE simulation gives us:

	NMOS	PMOS
L [m]	2e-6	2e-6
W [m]	14.6e-6	63.7e-6
ID [A]	34e-6	34.7e-6
Vov [V]	161e-3	156e-3
Gm [A/V]	365e-6	358e-6

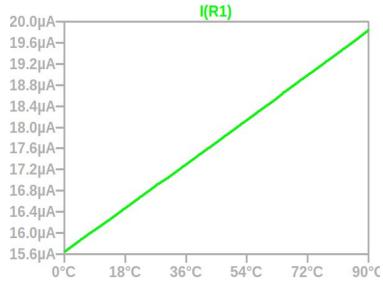
Note that here we will use for all transistors the same aspect ratio. (PMOS or NMOS transistor width can be further refined to have identical dc currents)

From I<sub>1</sub> equation we can see that the temperature dependence of it is linear:

$$I_1(T) = AT$$

'A' being a constant of value:

from 
$$I_1 = \frac{kT}{qR_1} \ln \left( \frac{I_{S2}}{I_{S1}} \right)$$
 we have  $A = \frac{k}{qR_1} \ln \left( \frac{I_{S2}}{I_{S1}} \right) = \frac{1.38e-23}{1.6e-19\cdot8e3} \ln (100) = 49.6 \, nA/K$ 



From the simulation we get A = 47.97 nA/K. ( $I_1$  is PTAT, whereas  $I_4$  is CTAT and both cancel each other)

Selecting the  $R_4/R_1$  ratio derived earlier, from simulation we can also see that the temperature dependence of the voltage reference will depend only on the logarithmic equation:

