LDO_A (FREEPDK45) Design using LUT

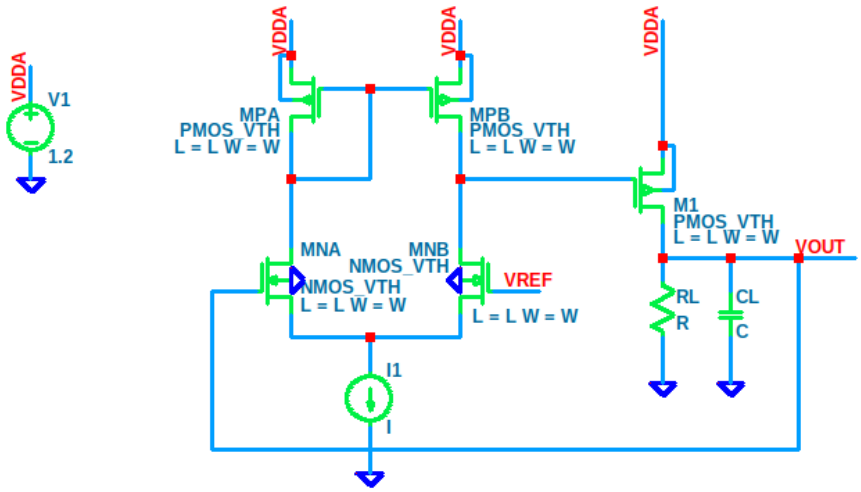

Figure 1: LDO with series-transistor

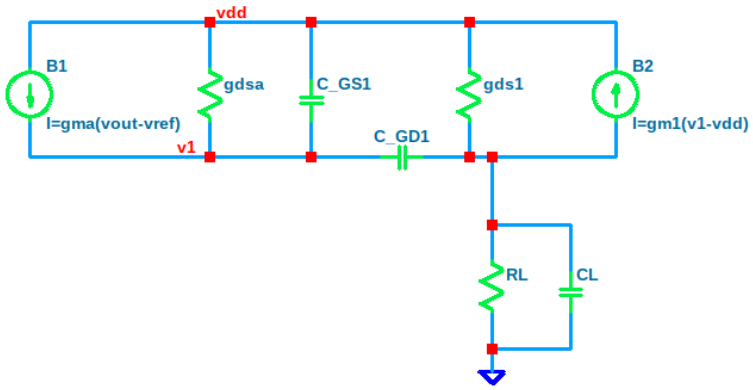

Figure 2: LDO SS

low-frequency analysis

This LDO have a series-shunt feedback loop (with the first termen referring to the input), with a feedback transfer function f of 1, and the closed-loop transfer function is:

$\frac{v_{out}}{v_{ref}} = \frac{A_1 A_a}{1 + A_1 A_{ref} f}$, where A1 and Aa are the voltage gains of the CS series transistor and the differential amplifier, respective.

$loop - gain = 1 + A_1 A_{ref} f$

Specifications

$I_{DC} = 10\,mA\,, V_{OUT} = .9\,V\,, VDD = 1.2\,V$ size for $the\ highest\ loop - gain$

Matlab

```
VDD = 1.2;          % supply voltage
V = .9;             % desired regulated voltage
ID = .01;           % desired current (RL = V/ID)
L = 100e-9;
Lp = 400e-9;
Ln = 400e-9;
```

Solution

CS

$$A_{1DC} = \frac{g_{m1}}{Y_L + g_{ds1}} = \frac{\left(\frac{gm}{id}\right)_1}{\frac{1}{V_{OUT}} + \left(\frac{gds}{id}\right)_1}$$

$V_{Dsat} = \frac{2}{\frac{g_m}{id}}$, we need to keep gm/id larger than 6.6 S/A to keep Vdsat of M1 smaller than the dropout voltage (0.3 V).

Matlab

```
for i = 7:12
  gm_id = i;

  VDS = V-VDD;
  gds_id = lookup_data(my_mat.pmos, 'gds_id', 'gm_id', gm_id, 'vds', VDS, 'lengths', L);
  JD = lookup_data(my_mat.pmos, 'id_width', 'gm_id', gm_id, 'vds', VDS, 'lengths', L);
  A = gm_id./(1/V + gds_id);

  W = ID/JD;
  Cgs = abs(W*lookup_data(my_mat.pmos, 'cgs_width', 'gm_id', gm_id, 'vds', VDS',
'lengths', L));
  Cgd = abs(W*lookup_data(my_mat.pmos, 'cgd_width', 'gm_id', gm_id, 'vds', VDS',
'lengths', L));
  VGS = lookupVGS(my_mat.pmos, 'gm_id', gm_id, 'vds', VDS, 'lengths', L);

  gm = gm_id*ID;
  gds = gds_id*ID;
  YL = ID/V;

  %disp("gm_id");
  %disp(gm_id); % and so on
end
```

To select $(gm/id)_1$ we will have to enumerate the gains of the stage for different values of (gm/id)1 between 7 S/A and 12 S/A/. In the following table the top entries are for L_1 = 100nm, the bottom entries for L_1 = 200 nm.

$(gm/id)_1 S/A$	7	8	9	10	11	12
A_1	4.5	5.34	6.09	6.8	7.4	8.1
	4.97	5.95	6.88	7.78	8.65	9.5
W_1(um)	198	244	299	365	445	542
	373	465	575	709	870	1069
V_{GS1}	-.72	-.69	-.67	-.65	-.63	-.61
	-.74	-.71	-.68	-.664	-.644	-.626
C_{gs1}	3.7e-13	4.5e-13	5.3e-13	6.2e-13	7.2e-13	8.3e-13
	1.4e-13	1.7e-13	2e-12	2.4e-12	2.8e-12	3.3e-12
C_{gd1}	3.6e-15	4.55e-15	5.6e-15	6.7e-15	8e-15	9.4e-15
	2.8e-15	1.76e-15	e-16	3.6e-15	1.4e-15	2.6e-15

Going to 200nm improves the gain very little and is very costly as far as layout area is concerned. We conclude that a gm/id of 10 with L1 = 100nm gives a good compromise.

Differential-Pair Amplifier Sizing

$$A_a = \frac{\left(\frac{g_m}{id}\right)_n}{\left(\frac{g_{ds}}{id}\right)_n + \left(\frac{g_{ds}}{id}\right)_p}$$

The drain to source and the gate-to source voltages of the p-channel mirror devices are fixed by VGS1 and hence the gate length is the only degree of freedom for their sizing. Since we value gain more than bandwidth in this sub-circuit, we opt for 400nm channel length, and this allow us to find (gds/id)p.

```
gds_idp = lookup_data(my_mat.pmos, 'gds_id', 'vgs', VGS, 'vds', VGS, 'lengths', Lp);
```

For the diff-pair, for high gain we assume L = 400nm, and to find the maximum Aa we will use the following Matlab script in which we iterate over available VS the gain of the differential pair:

Matlab

```
VD = VDD - abs(VGS);
US = (.2: .015: .5)'; zn = length(US);
for k=1:zn
  VS = US(k);
  gm_idn(k,1) = lookup_data(my_mat.nmos, 'gm_id', 'vgs', V-VS, 'vds', VD-VS, 'vsb', VS,
'lengths', Ln);
  gds_idn(k,1) = lookup_data(my_mat.nmos, 'gds_id', 'vgs', V-VS, 'vds', VD-VS, 'vsb', VS,
'lengths', Ln);
end

Aa = gm_idn./(gds_idn + gds_idp);
```

And now we can plot the loop-gain:

```
f = 1;
loop_gain = Aa.*A*f;

plot(gm_idn, loop_gain)
xlabel('gm/idn');
ylabel('loop-gain');
```

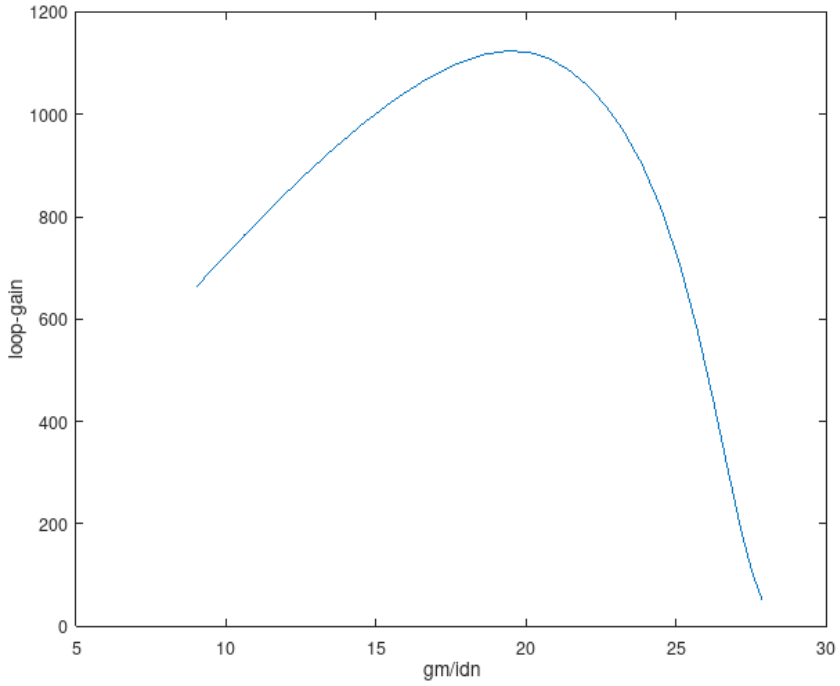

Figure 3: Loop-gain vs $(gm/id)_n$

From Figure 3 we see that the maximum loop-gain that we get with this circuit can be achieved by using $(gm/id)_n$ equal to 20.

By interpolation we can find Aa and Vs (the source voltage):

```
value_of_Aa_for_gm_idn_20 = interp1(gm_idn, Aa, 20)

VS = interp1(gm_idn, US, 20)

gds_IDN = interp1(gm_idn, gds_idn, 20)
```

Where we get Aa = 164.82, VS = 0.27V. Based on the data, we make the following design choices:

- series transistor L1 = 100nm, (gm/id)1 = 10 S/A

- differential amplifier Ln = 400nm with (gm/id) = 20 S/A

- the loop-gain is 1121 with A1 = 6.8 and Aa =164.82

Now we need to decide for the tail current.

The amplifier bias curent is normally a small fraction of the LDO's output current. We push 2% in this example, which leads to 2IDn = 0.2 mA. This choice lets us finalize the sizing for the SPICE verification.

Matlab

```
IDN = 100e-6;
JDP = lookup_data(my_mat.pmos, 'id_width', 'vgs', VGS, 'vds', VGS, 'lengths', Lp);
Wp = IDN/JDP;
JDN = lookup_data(my_mat.nmos, 'id_width', 'vgs', V-VS, 'vds', VD-VS, 'vsb', VS, 'lengths', Ln);
Wn = IDN/JDN;

gda = (gds_idp + gds_IDN)*IDN;                %output conductance of diff ampifier
gma = gm_IDN*IDN;
```

The resulting widths are:

Wn = 102 um

Wp = 15.8 um, for the following lengths:

Ln = Lp = 400 nm

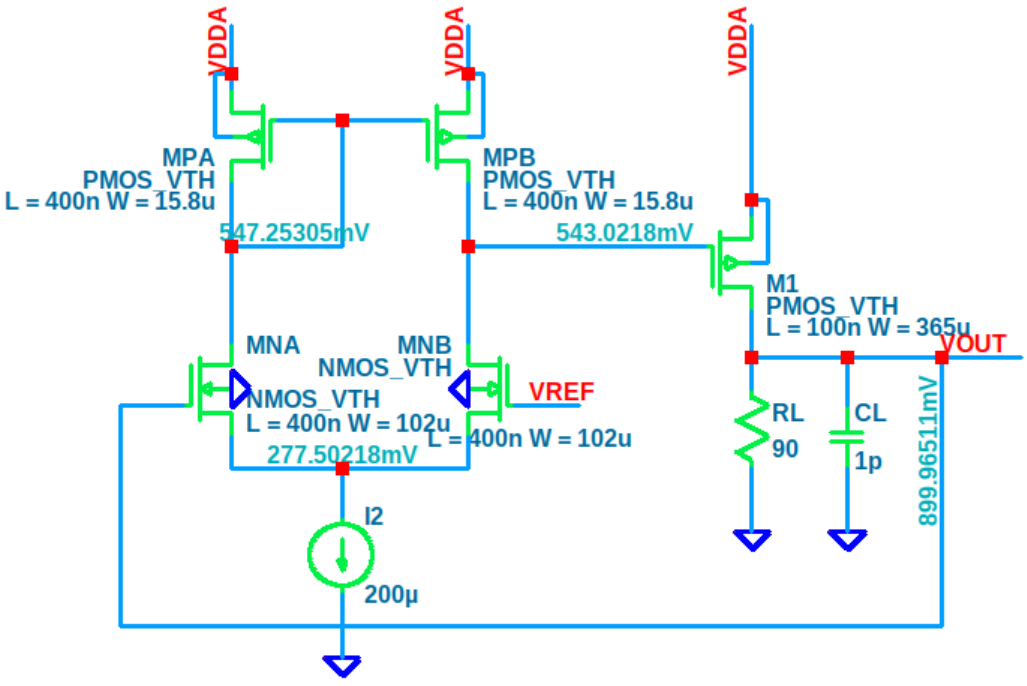

Figure 4: low-frequency analysis - final circuit without bias

SPICE Analysis

	VS(mV)	VD(mV)	A1	Aa

Analysis	0.27	0.547	6.8	164.82
SPICE	0.277	0.543	6.78	163.29

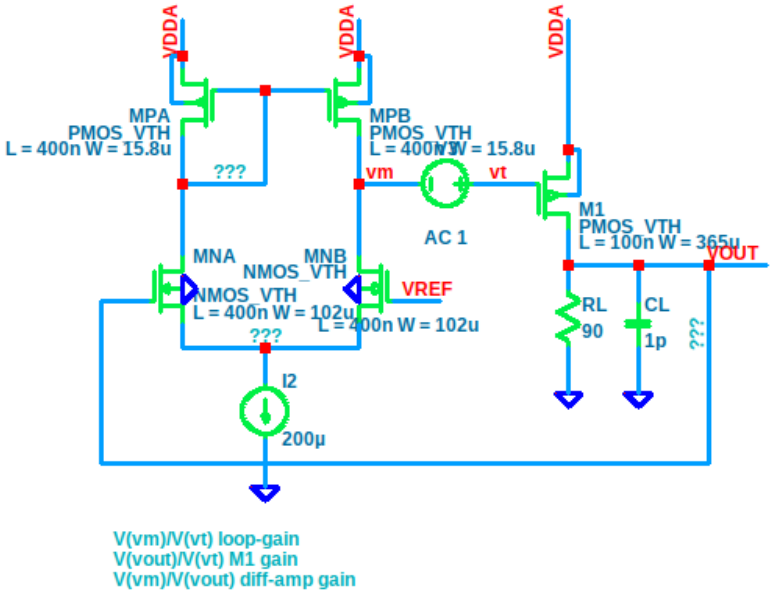

Figure 5: TB AC analysis

high-frequency analysis

$$ao = G_{m1} R_1 G_{m2} R_2$$

$$\frac{1}{\omega_{pd}} = R_1 (G_{m2} R_2) C_c$$

$$f_{p2} = \frac{G_{m2}}{2\pi C_L}$$

$$\frac{1}{\omega_{zp}} = \frac{C_c}{G_{m2}}$$

if we are using dominant pole compensations with Miller C_c

where $R_1 = 1/g_{dsa}$ *output resistance of the differential amplifier*

and $R_2 = 1/(Y_L + g_{ds1})$ *the resistance at the output node*

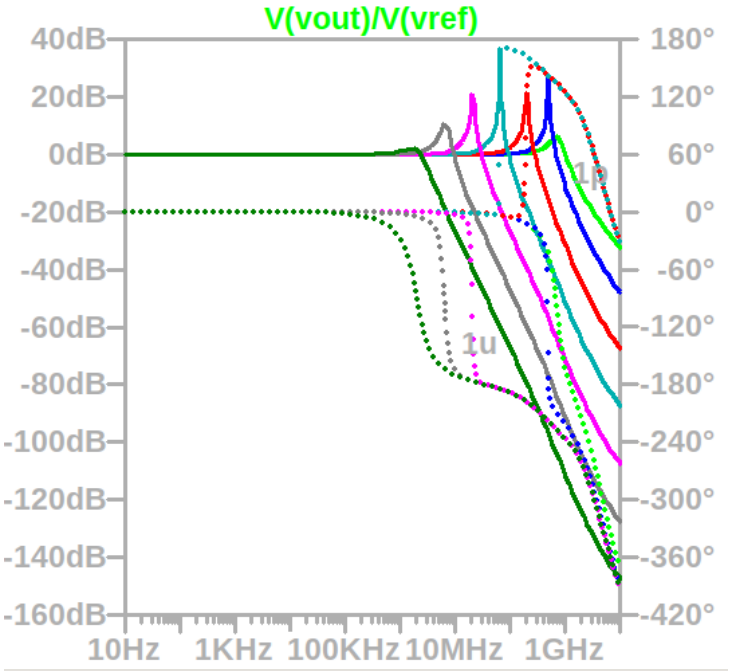

Figure 6: Closed-loop frequency response as CL is varied from 1pF to 1uF

From Figure 6 we can see that, when CL is very small or very large, the LDO behaves like a first-order circuit, but when the two poles get close, the amplifier behaves like a second-order system that has poor phase margin.

In the loop-gain AC analysis in Figure 7 we can see a complex-zero determined by the transfer-function of the differential amplifier Figure 8.

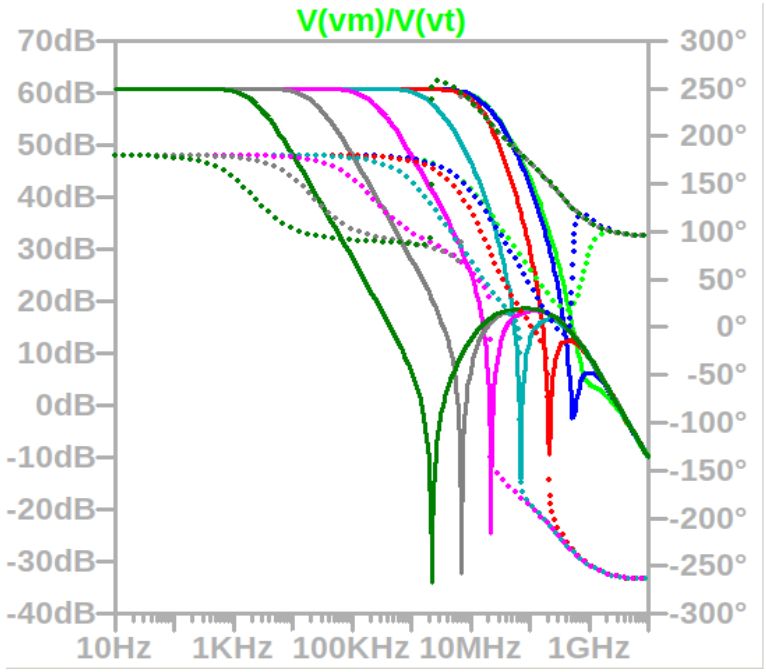

Figure 7: loop-gain

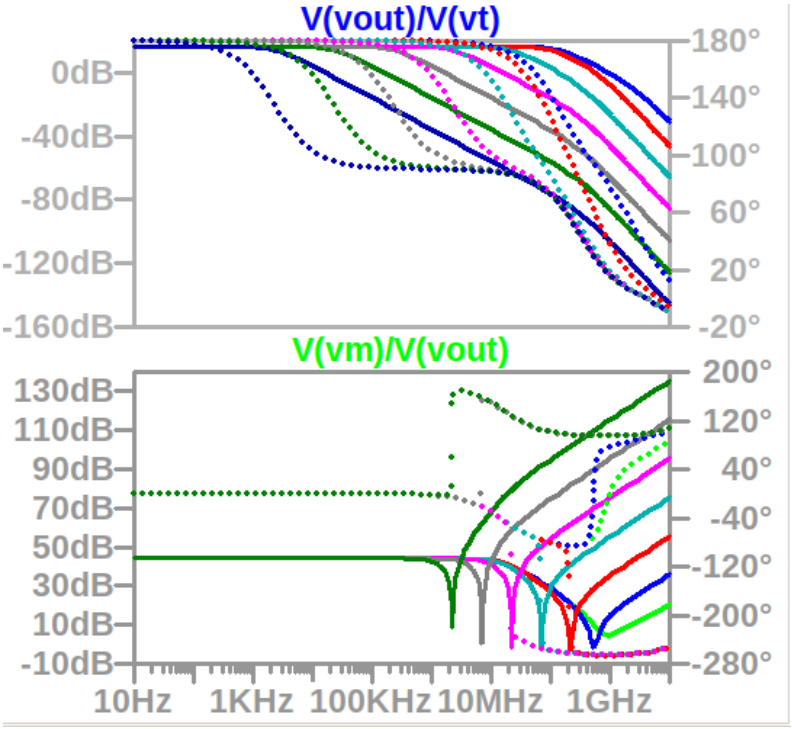

Figure 8: Top-to-botom CS M1, and the differential amplifier transfer functions respectively

For example with CL = 10pF, and Miller capacitor across drain-gate of M1, Cc = 1pF our regulator loop-gain is inherently stable, Figure 9.

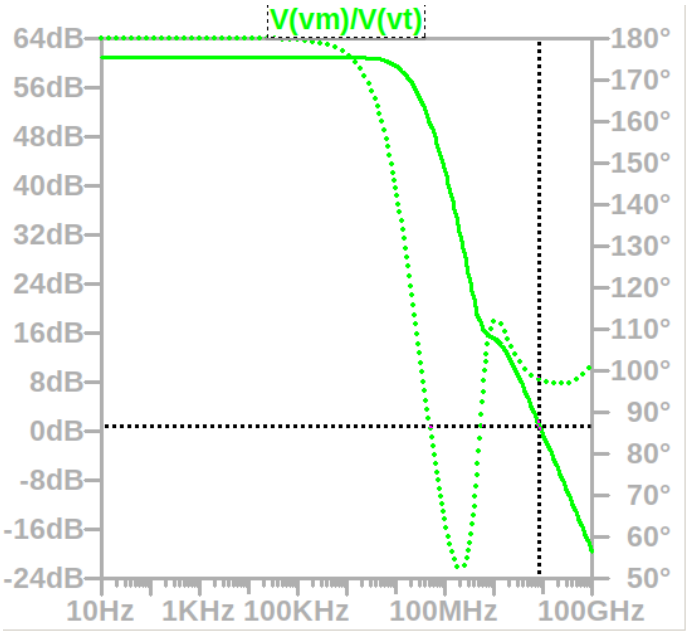

Figure 9: loop-gain

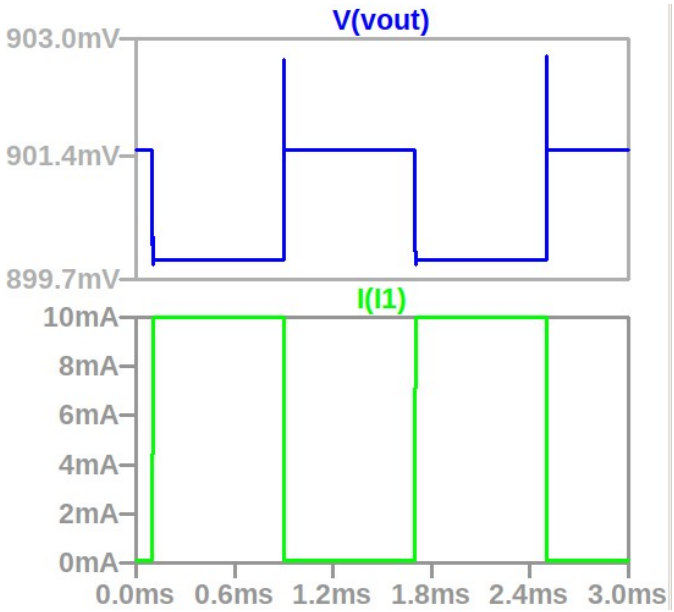

Figure 10: load-regulation, I step 0.1mA to 10mA

Bibliography

1. https://github.com/bmurmann/Book-on-gm-ID-design

Note that the functions from [1] are not compatible with this note's design, as I generated my own LUT for the PDK45 with NGSPICE and I also had to modify the functions to work with it, as the original paper requires acces to Cadence Virtuoso and Matlab.