

Project - Table of Contents

1. Project theme.....	2
2. LPF.....	3
2.1 LPF design at transistor level.....	6
2.1.1 CMFB.....	10
2.2 Verifying and characterizing the LPF.....	11
2.2.1 Verifying and characterizing the operational amplifier.....	11
2.2.2 Verifying and characterizing the LPF as a functional block.....	18
3. PGA.....	20
3.1 Sizing the PGA.....	20
3.1.1 Sizing the passive components of the PGA.....	20
3.1.2 Designing the PGA at transistor level.....	22
3.2 Verifying and characterising the PGA.....	24
3.2.1 Verifying and characterizing the transconductor.....	24
3.2.2 Verifying and characterizing the PGA as a functional block.....	28
4. Verifying and characterizing LPF + PGA.....	29
5. LPF-AO Miller Modifications.....	32
Bibliography.....	35

1. Project theme

The requirements of the project will be to design a 3rd order Chebyshev low-pass filter with a 1dB ripple and a cutoff frequency of 4 Mhz using a TT-structure. Another requirement was the implementation of a programmable gain amplifier as a cascade of two-stages with different gain steps (coarse + fine). Each gain stage should be realized as a 2Gm PGA using a Kwan-Martin transconductor. Both using a lower supply voltage of 1.8 V and a fully differential approach. This will bring a larger output voltage swing, but with a disadvantage that they will require a common-mode feedback circuit to control the common-mode output voltage.

2. LPF

The sizing and denormalization of the filter components remain the same as for the single-ended design.

For the low pass filter the first step is to compute the transfer function of the filter using the required specifications. The goal for the ripple is 1dB for an implementation with real components (finite GBW operational amplifier) so in obtaining the transfer function we go for a lower ripple of 0.2dB.

The normalized transfer function is:

$$H_0(s) = H_0 \cdot \frac{c_1}{s + c_1} \cdot \frac{d_2}{s^2 + c_2 s + d_2} \quad (1)$$

There are tables that contain the factors of the denominator polynomials normalized Chebyshev low-pass filters.

n	0.2-dB Ripple ($\epsilon = 0.21709$)
1	$s + 4.60636$
2	$s^2 + 1.92709s + 2.35683$
3	$(s + 0.81463)(s^2 + 0.81463s + 1.41363)$
4	$(s^2 + 0.44962s + 1.19866)(s^2 + 1.08548s + 0.49155)$
5	$(s + 0.46141)(s^2 + 0.28517s + 1.11741)(s^2 + 0.74658s + 0.55839)$
6	$(s^2 + 0.19705s + 1.07792)(s^2 + 0.53835s + 0.64491)(s^2 + 0.73540s + 0.21190)$
7	$(s + 0.32431)(s^2 + 0.14433s + 1.05566)(s^2 + 0.40441s + 0.71644)(s^2 + 0.58439s + 0.29343)$
8	$(s^2 + 0.11028s + 1.04183)(s^2 + 0.31407s + 0.77124)(s^2 + 0.47004s + 0.38855)(s^2 + 0.55445s + 0.11795)$

Figure 1: The factors of the denominator polynomials normalized Chebyshev low-pass filter for a 0.2dB ripple

Table 1: The coefficients of the normalized transfer function

c1	c2	d2
0.81463	0.81463	1.41363

The next step is to obtain the denormalized transfer function by replacing $s \rightarrow s/\omega_n$:

$$H_{denormat}(s) = H_0 \cdot \frac{c_{1d}}{s + c_{1d}} \cdot \frac{d_{2d}}{s^2 + c_{2d}s + d_{2d}} \quad (2)$$

Where $f_c = 4\text{MHz}$:

$$c_{1d} = c_1 \omega_n \quad (3)$$

$$c_{2d} = c_2 \omega_n \quad (4)$$

$$d_{2d} = d_2 \omega_n^2 \quad (5)$$

$$\omega_n = 2\pi f_c \quad (6)$$

The resulting coefficients are:

Table 2: The coefficients of the transfer function

c1d	c2d	d2d
2.04e7	2.04e7	8.92e14

Once the coefficients are obtained, we must compute the values of the passive components but for this we need to consider the implementation of the filter. For this we use a lossy integrator and a Tow-Thomas biquad.

The general transfer function for a lossy integrator:

$$H(s) = H_0 \cdot \frac{\omega_0}{s + \omega_0} \quad (7)$$

In this case for the lossy integrator the transfer function is:

$$H(s) = 1 \cdot \frac{2.04739 \cdot 10^7}{s + 2.04739 \cdot 10^7} \quad (8)$$

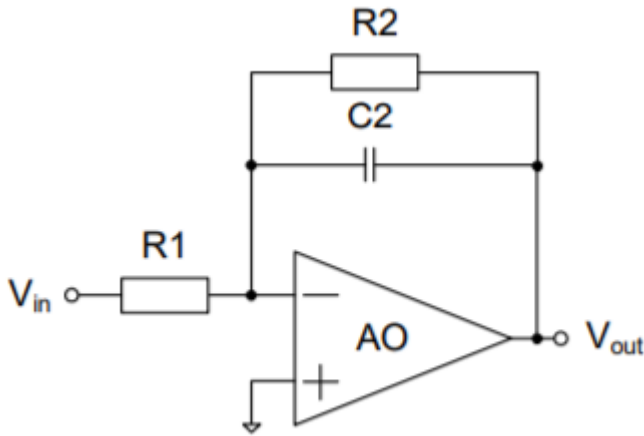


Figure 2: The schematic of a single-ended lossy integrator

The transfer function of this lossy integrator is:

$$H(s) = \frac{-R_2}{R_1} \cdot \frac{\frac{1}{R_2 C_2}}{s + \frac{1}{R_2 C_2}} \quad (9)$$

Since $H_0=1$ then $R_1=R_2$, and if we choose $C_2=1\text{pF}$ the resulting values for the passive components are:

Table 3: The values of the passive components of the lossy integrator

R1[Ohm]	R2[Ohm]	C2[F]
48.8e3	48.8e3	1e-12

The general transfer function for a second order low pass filter:

$$H(s) = H_0 \cdot \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (10)$$

In this case the transfer function for the 2nd order LPF is where $f_0 = 4.76 \text{ MHz}$:

$$H(s) = 1 \cdot \frac{(2.99 \cdot 10^7)^2}{s^2 + \frac{2.99 \cdot 10^7}{1.46}s + (2.99 \cdot 10^7)^2} \quad (11)$$

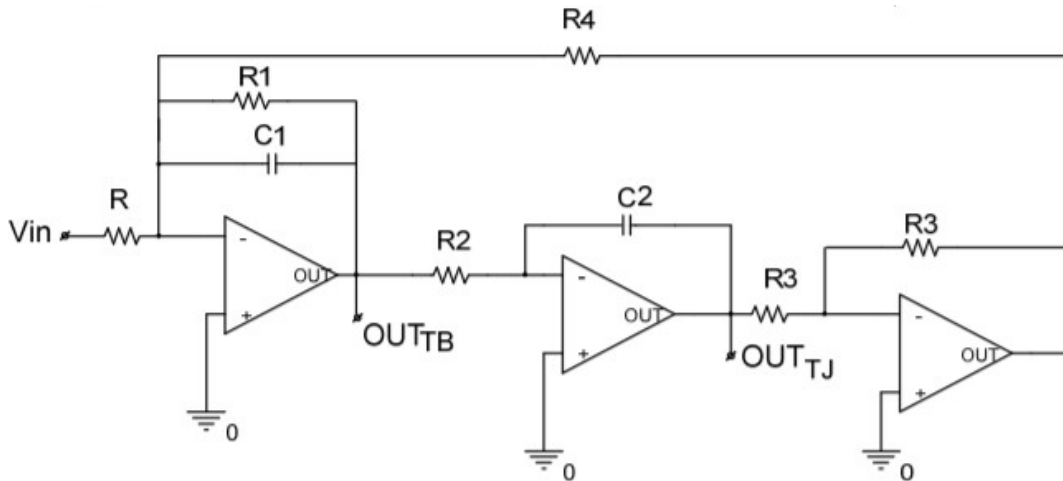


Figure 3: The schematic of a Tow-Thomas biquad

The transfer function of the Tow-Thomas biquad is:

$$H(s) = \frac{R_4}{R} \cdot \frac{\left(\frac{1}{\sqrt{R_2 R_4 C_1 C_2}} \right)^2}{s^2 + \frac{1}{\sqrt{R_2 R_4 C_1 C_2}} s + \left(\frac{1}{\sqrt{R_2 R_4 C_1 C_2}} \right)^2} \quad (12)$$

Since $H_0=1$ then $R_4=R$ and if we choose $C_1=C_2=1\text{pF}$ and $R_4=R_2=R_3$ then $R_1=Q \cdot R_2$, where $R_2 = \frac{1}{\omega_0 \cdot 1\text{pF}}$. The values for the passive components are:

Table 4: The values of the passive components of the tow-thomas-biquad

R1[Ohm]	R=R2=R3=R4[Ohm]	C1=C2[F]
48.8e3	33.5e3	1e-12

2.1 LPF design at transistor level

The active component of the LPF is a fully differential AO Miller operational amplifier.

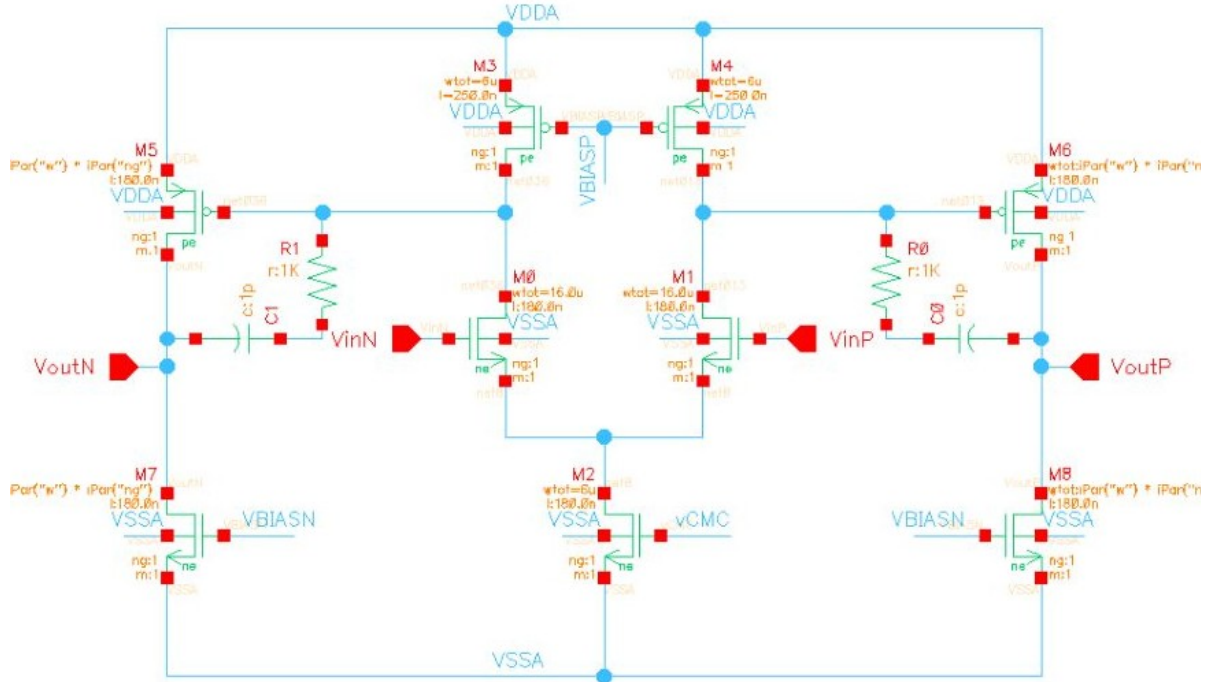


Figure 4: The schematic of the fully-differential Miller operational amplifier with RC compensation

The requirements for the OA were a gain bandwidth prooduct of 150 MHz, a Slew-Rate of at least 40 V/ μ s, a total current consumption of 150 μ A, a phase margin greater than 60 degrees and a gain of at least 60 dB for a load of 1 pF.

GBW[Hz]	I _{DD} [A]	SR[V/ μ s]	PM[°]	C _L [F]	a _o [dB]
150e6	150e-6	40	60	1e-12	60

Particular eq. for the two stage opamp with CMFB circuit (presented later) are the folowing:

DM path:

$$a_{dm0} = G_{m1} R_{o1} G_{m2} R_{o2}$$

$$|a_{dm0} f_{dm} p_{1d}| = GBW = 1 \cdot |p_{2d}| \text{ if the RHPZ has been eliminated,}$$

where f_{dm} is the feedback factor (can be instantiated to 1, if we are not concerned about the loop-gain), and GBW is the gain bandwidth product of the DM path.

$$\frac{G_{m1} R_{o1} G_{m2} R_{o2}}{R_{o1} (G_{m2} R_{o2}) C_M} = \frac{G_{m2}}{C_L} \rightarrow \frac{G_{m1}}{C_M} = \frac{G_{m2}}{C_L} \quad (13)$$

CM path:

$$a_{cmc0} \approx g_{m2h} [(r_{o1} g_{m1} r_{o2h}) || r_{o4}] G_{m2} R_{o2}$$

$$\left(\frac{W}{L} \right)_{2h} = \frac{(W/L)_2}{2} \text{ and } I_{d2h} = I_{D2}/2$$

$$|a_{cmc0} a_{cms0} p_{1c}| = 1 \cdot |p_{2c}| \rightarrow \frac{g_{m2h}}{C_M} |a_{cms0}| \approx \frac{G_{m2}}{C_L} \quad (14)$$

where a_{cms0} is the low-frequency gain through the CM-sense circuit.

Through an iterative process we can start by selecting CM, and verifying the previous equations again:

1. We choose $C_M = 0.22 \cdot C_L = 220 \text{ fF}$

2. From the equation for the gain bandwidth product we obtain G_{m1}

$$G_{m1} = 2 \pi C_M GBW \quad (15)$$

$$G_{m1} = g_{m0,1} = 207 \mu S \quad (16)$$

3. We choose $V_{dsat0,1} = 150\text{ mV}$

4. From the previous two steps we can compute I_{BIAS}

$$I_{BIAS} = G_{m1} \cdot V_{dsat0,1} = 31.1\text{ }\mu\text{ A} \quad (17)$$

5. We choose $V_{dsat3,4} = 150\text{ mV}$

6. We can compute the current through the output stage as the difference between the current budget and the current through the first stage.

$$I_{D6} = I_{D5} = \frac{I_{DD} - I_{BIAS}}{2} = \frac{150\text{e-}6 - 31.1\text{e-}6}{2} \approx 60\text{e-}6 \quad (18)$$

7. We choose $V_{dsat6,5} = V_{dsat3,4} = 150\text{ mV}$

8. We can now compute G_{m2}

$$G_{m2} = \frac{2I_{D6}}{V_{dsat6}} = \frac{2 \cdot 60\text{e-}6}{0.15} = 800\text{ }\mu\text{ S} \quad (19)$$

9. We have to split the low frequency gain between the two stages. For this we need to consider the linearity of the amplifier. We have to ensure that even for the maximum output voltage the input voltage for the second stage is not larger than the linear range of M_6 . Also since R_{O2} is the equivalent output of the amplifier we don't want it to be too large, so we prefer to have a higher gain in the first stage. Taking all this into consideration we obtain: $a_{v1} = 50\text{ V/V}$ and $a_{v2} = 20\text{ V/V}$.

10. Since we know both the gain and the transconductance of each stage we can compute the output resistance:

$$R_{O1} = \frac{a_{v1}}{G_{m1}} = \frac{50}{207\text{e-}6} \approx 240\text{ k}\Omega \quad (20)$$

$$R_{O2} = \frac{a_{v2}}{G_{m2}} = \frac{20}{800\text{e-}6} = 25\text{ k}\Omega \quad (21)$$

11. Next we have to verify that the computed Slew-Rate is greater than the required one:

$$SR_{OUT} = \frac{I_{D5,6}}{C_L} = \frac{60\text{e-}6}{1\text{e-}12} = 60\text{ V}/\mu\text{ s} \quad (22)$$

$$SR_{-IN} = \frac{I_{BIAS}}{C_1} \approx \frac{31.1e-6}{C_M} = 141 V/\mu s \quad (23)$$

12. Taking into consideration the requirement for the phase margin we can compute the value for R_M .

$$PM = 90^\circ - \tan^{-1} \frac{GBW}{f_{p2}} - \tan^{-1} \frac{GBW}{f_z} \quad (24)$$

where

$$f_{p2} = \frac{G_{m2}}{2\pi C_L} \quad (25)$$

$$f_z = \frac{1}{2\pi C_M \left(\frac{1}{G_{m2}} - R_M \right)} \quad (26)$$

From these equations it follows that for a PM of 60° we need: $R_M = 100 \Omega$

We can verify eq. 1:

$$\frac{G_{m1}}{C_M} = \frac{G_{m2}}{C_L} \rightarrow C_M = C_L \frac{G_{m1}}{G_{m2}} = \frac{1e-12 \cdot 207e-6}{792e-6} = 261 fF$$

And from eq. 2 we can get a_{cms0} :

$$\frac{g_{m2h}}{C_M} |a_{cms0}| \approx \frac{G_{m2}}{C_L} \rightarrow |a_{cms0}| = \frac{\frac{G_{m2}}{C_L} \cdot C_M}{g_{m2h}} = 0.15$$

These are the resulting values of the transistors design sheet:

M	ID [A]	Vdsat [V]	gm [A/V]	W [m]	[L]	TYPE
M3,4	15.5e-6	0.15	207e-6	5.44e-6	250e-9	PMOS
M0,1	15.5e-6	0.15	207e-6	2.4e-6	250e-9	NMOS
M2	31e-6	0.11	565e-6	4e-6	250e-9	NMOS
M5,6	60e-6	0.15	792e-6	22.8e-6	180e-9	PMOS
M7,8	60e-6	0.11	1e-3	7.7e-6	250e-9	NMOS

Table 5: Resulting values for the transistors dimensions

2.1.1 CMFB

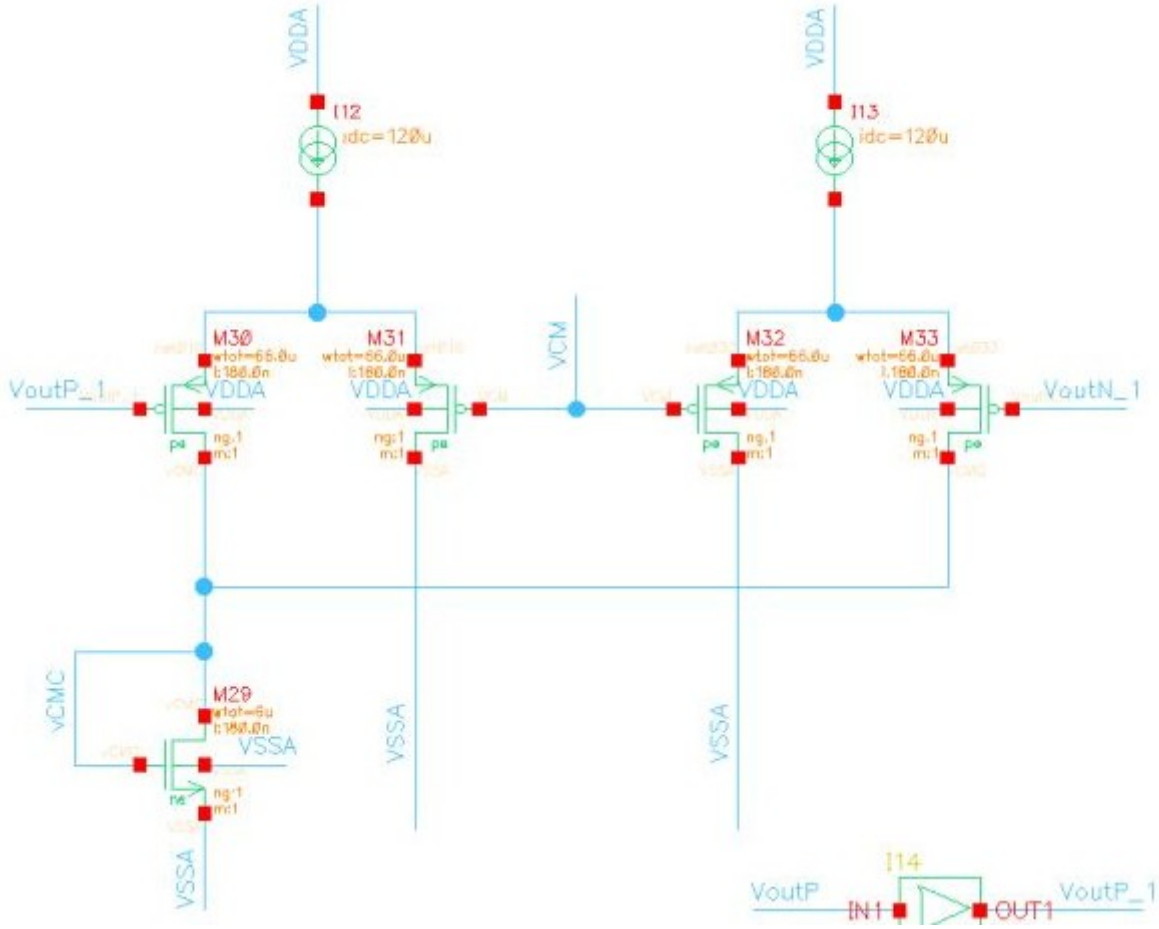


Figure 5: CMFB Circuit

→ small-signal analysis:

$$I_{D30} = \frac{I_{12}}{2} + g_{m30} \frac{(V_{CM} - V_{outP_1})}{2} \quad (27)$$

$$I_{D33} = \frac{I_{13}}{2} + g_{m33} \frac{(V_{CM} - V_{outN_1})}{2} \quad (28)$$

These currents are summed in diode-connected M29 to give the CM sensor output current:

$$I_{cms} = I + g_{m30} \left(V_{CM} - \frac{V_{outP_1} + V_{outN_1}}{2} \right) = I + g_{m30} (V_{CM} - V_{oc}) \quad (29)$$

where $I_{12} = I_{13} = I$, and $g_{m30} = g_{m33}$

We note that one design option is to select $I_{13} = I_{12} = |I_{D3}| + |I_{D4}|$ and $(W/L)_{29} = (W/L)_2$.

2.2 Verifying and characterizing the LPF

2.2.1 Verifying and characterizing the operational amplifier

Using the previously obtained values we obtain the following results for the amplifier:

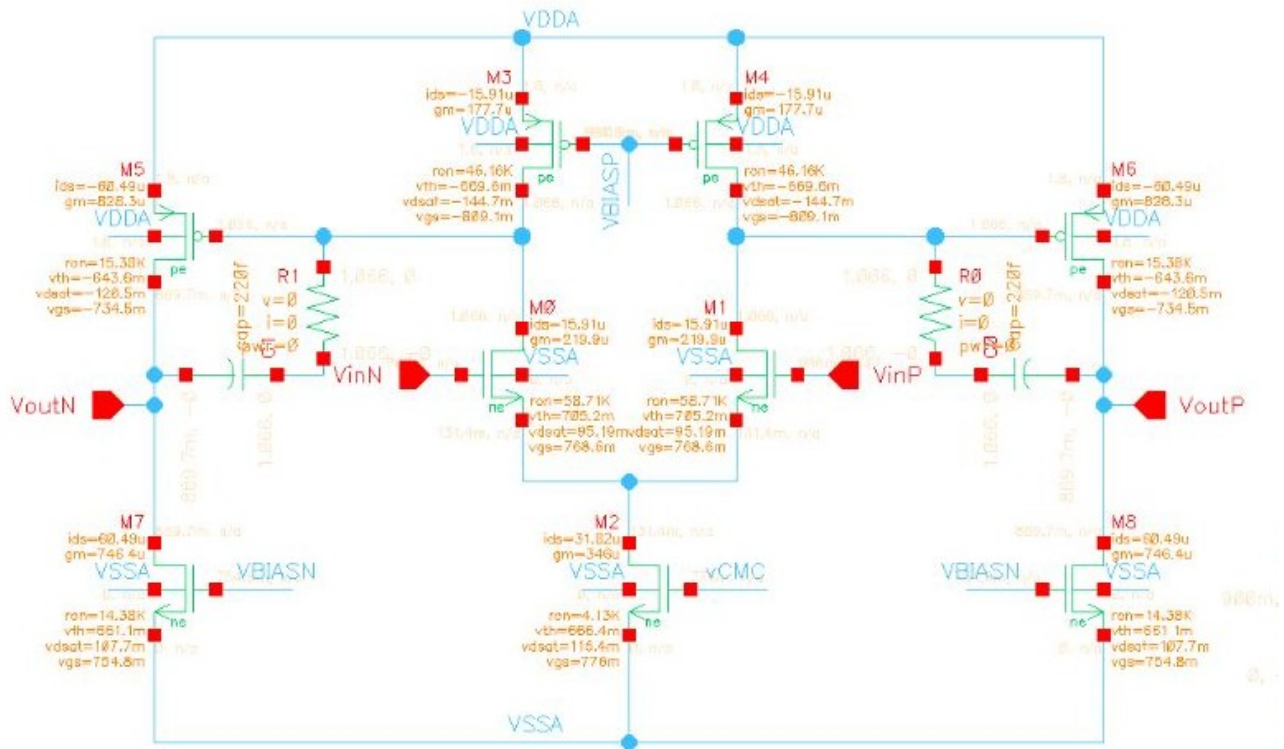


Figure 6: The DC operating point of the transistors

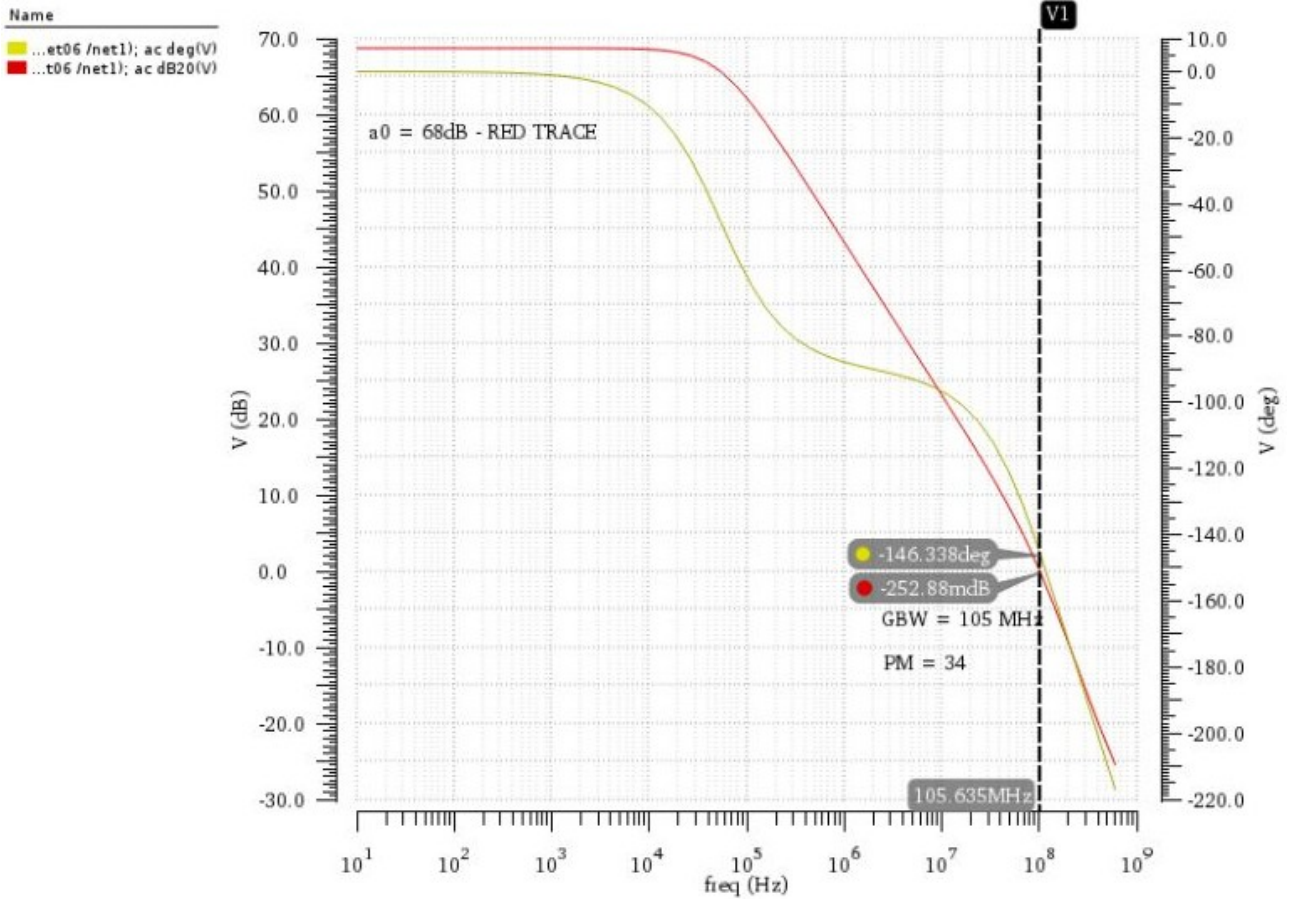


Figure 7: The transfer function of the amplifier

a_0 [dB]	GBW [Hz]	PM[°]	I_{DD} [A] w/o CMFB
68	105e6	34	168e-6

CMFB:

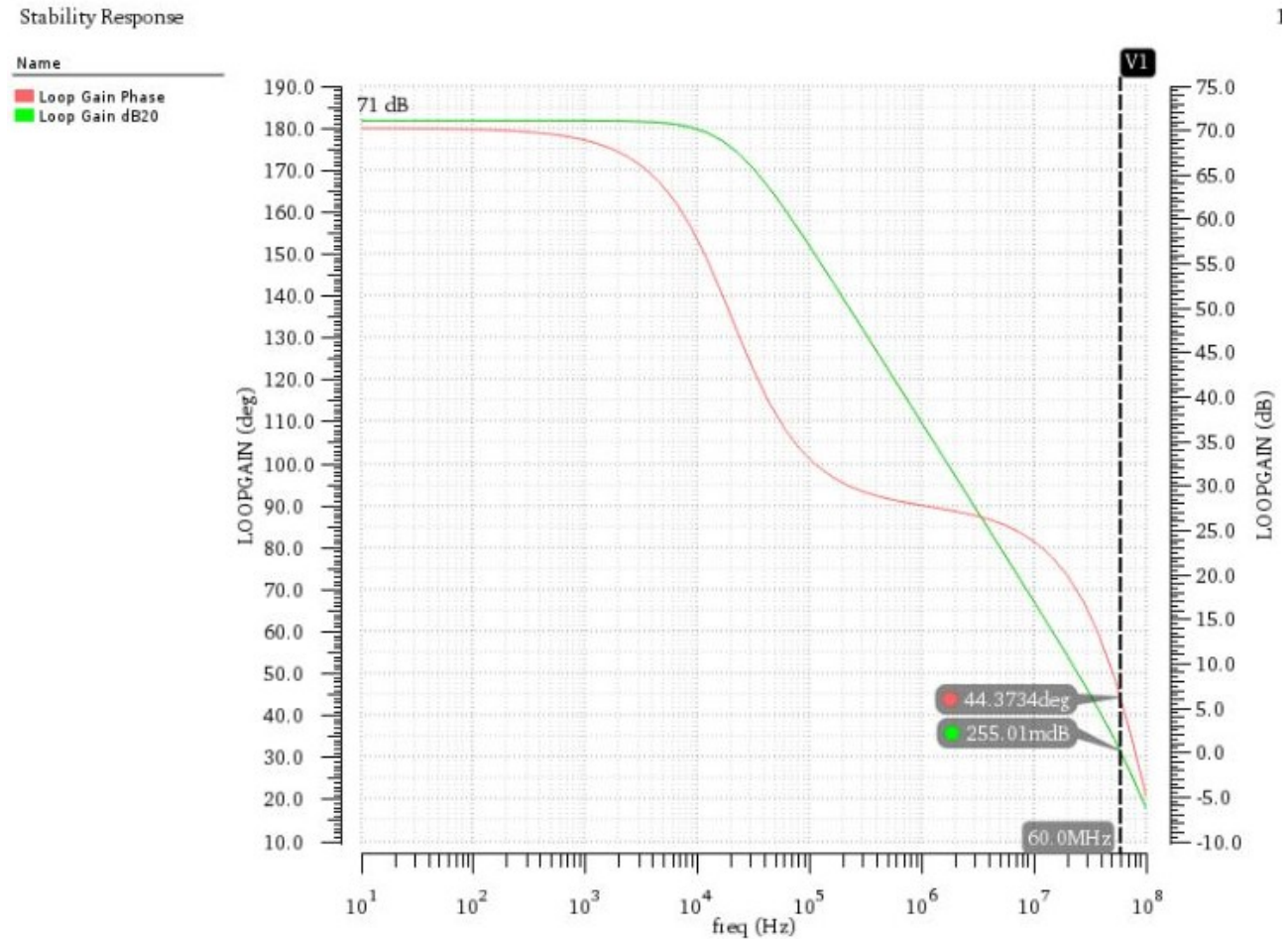


Figure 8: Loop-gain of CMFB circuit

As can be seen above after the first iteration both the phase margin and the gain bandwidth product are too small.

To make for the GBW and PM which are too small for the previous design we can restart the iteration with a higher GBW specification and a smaller C_M . The following table reveals the new transistors data for a GBW of 200 Mhz and a C_M of 120 fF.

M	ID [A]	Vdsat [V]	gm [A/V]	W [m]	[L]	TYPE
M3,4	11.3e-6	0.15	150e-6	4e-6	250e-9	PMOS
M0,1	11.3e-6	0.15	150e-6	1.72e-6	250e-9	NMOS
M2	22.6e-6	0.11	411e-6	2.92e-6	250e-9	NMOS
M5,6	63.69e-6	0.15	792e-6	25e-6	180e-9	PMOS
M7,8	63.69e-6	0.11	1.11e-3	8.25e-6	250e-9	NMOS

Table 6: Resulting values of the transistors dimensions for the second iteration

After the second iteration I obtained the following results:

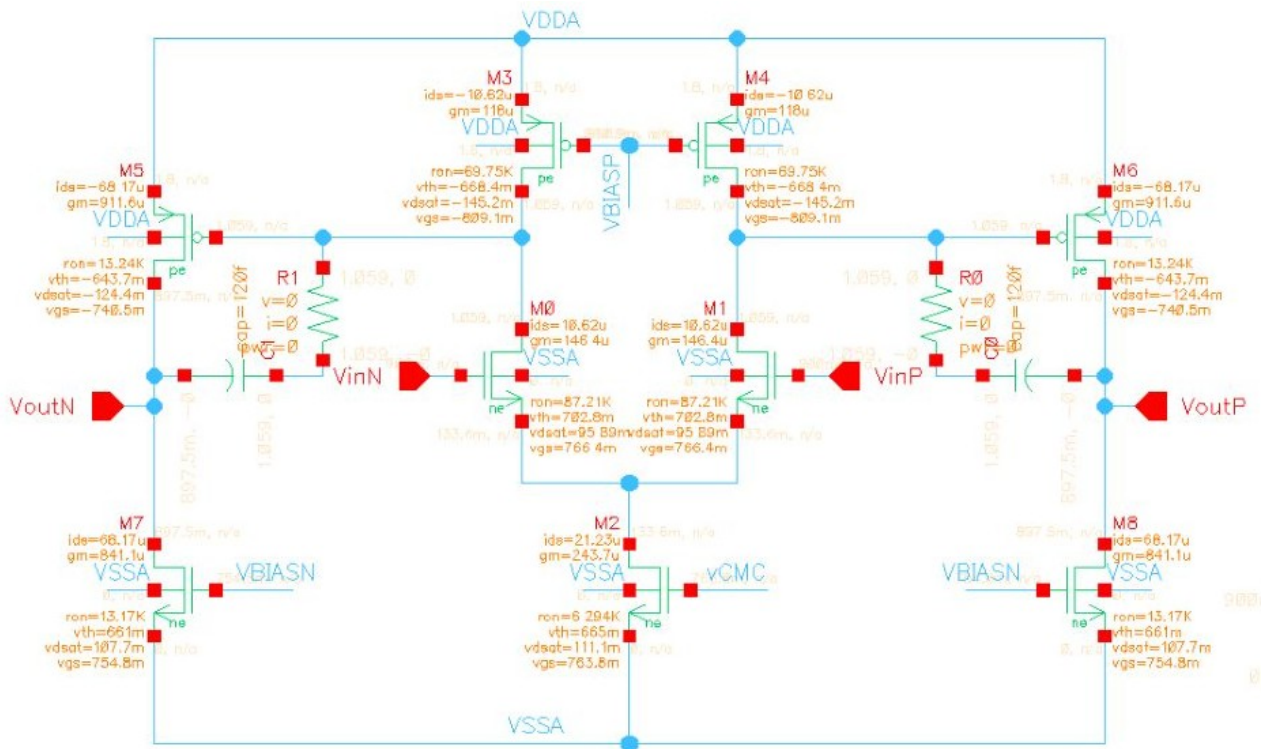


Figure 9: The DC operating point of the transistors

v (/net06 /net1); ac dB20(V):v (/net06 /net1); ac deg(V)

Fri Aug 16 05:49:14 2024

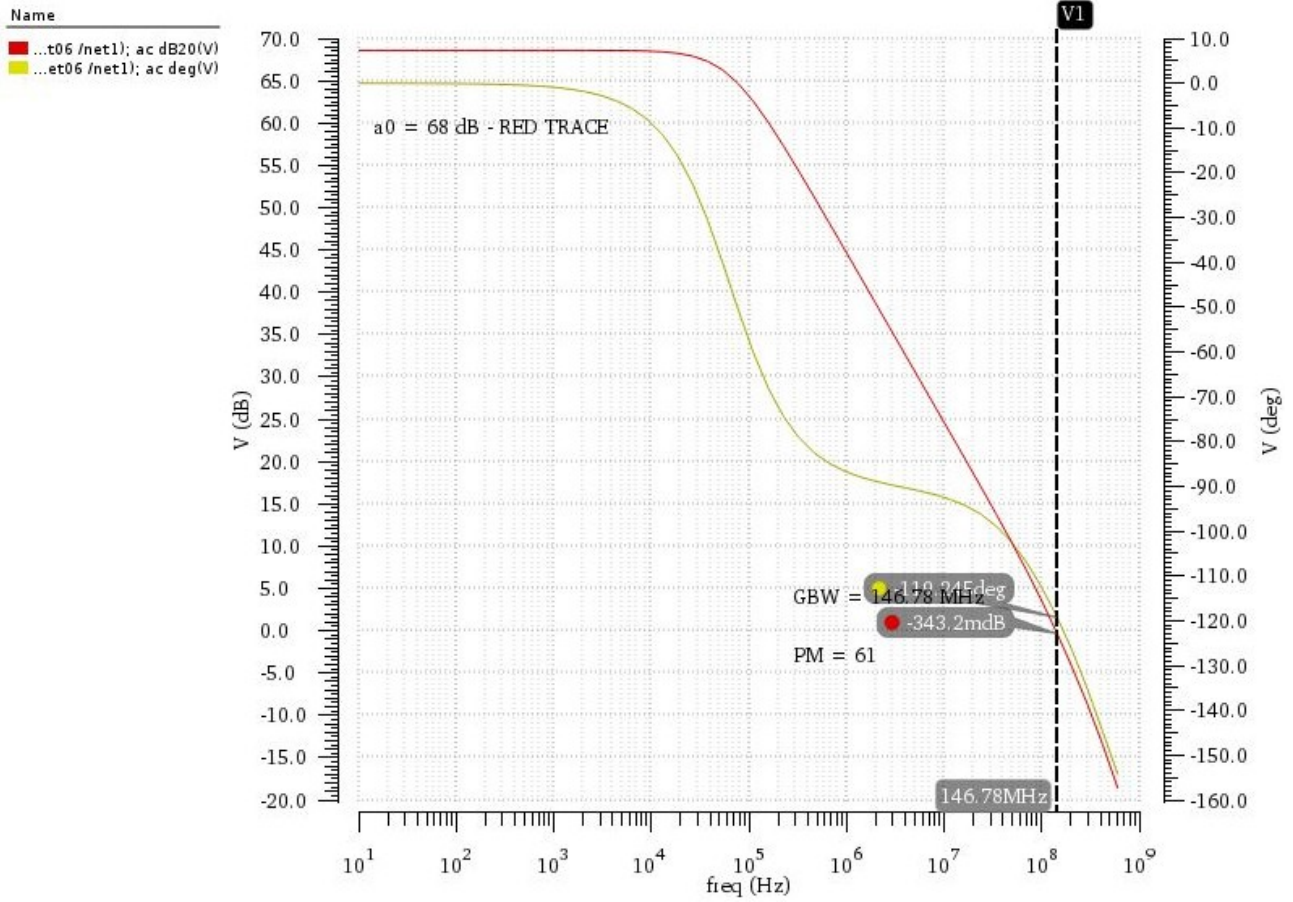


Figure 10: The DM open-loop transfer function of the amplifier

Stability Response

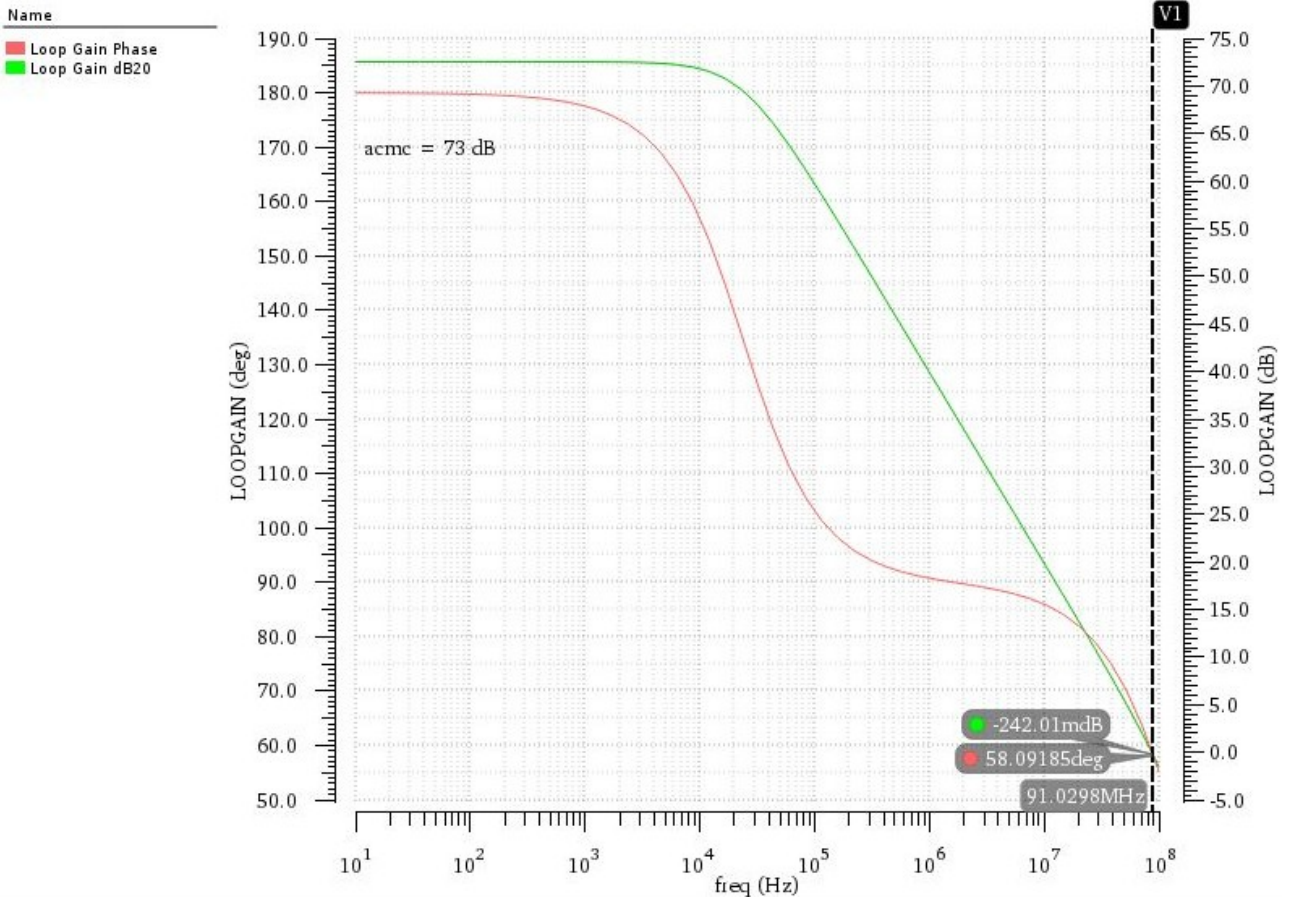


Figure 11: The CMFB loop-gain of the amplifier

Note that the CMFB loop is overcompensated due to the higher impedances at the common nodes between CM and DM paths.

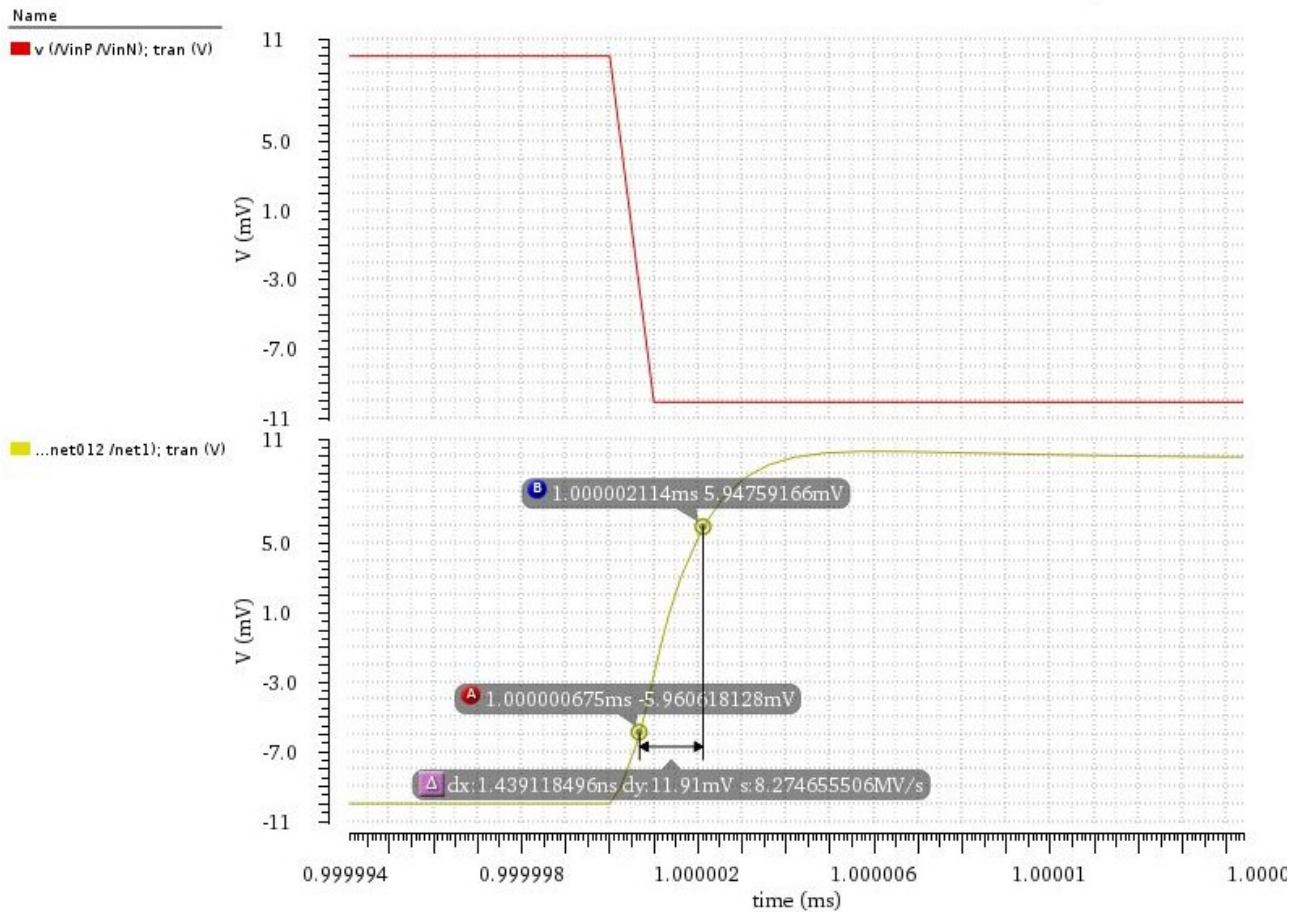


Figure 12: The SR for a negative variation of the input voltage

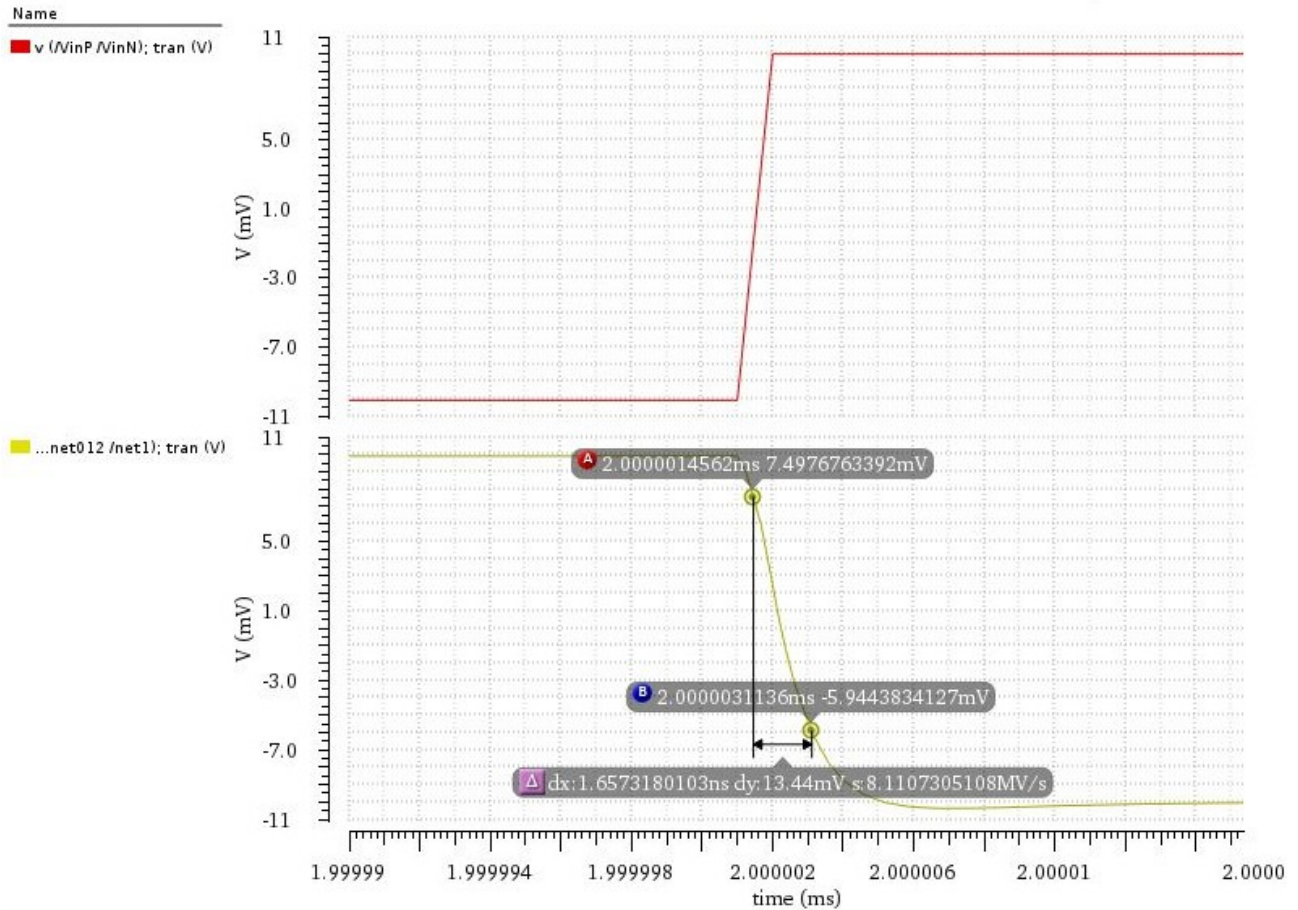


Figure 13: The SR for a positive variation of the input voltage

→ this AO cannot drive resistive loads

DM path:

A0 [dB]	GBW [Hz]	PM[°]	IDD [A]	IDD_CMFB [A]	SR_RISE[V/ us]	SR_FALL
68	143e6	62	173e-6	44e-6	8.27	8.11

Table 7: The main parameters of the AO

V _{DD} [V]	V _{ICMmin} [V]	V _{ICMmax} [V]	V _{OCMmin} [V]	V _{OCMmax} [V]	V _{ICM_MEDIU} [V]	V _{OCM_MEDIU} [V]
1.8	0.8775	1.76	0.107	1.67	1.31	0.885

2.2.2 Verifying and characterizing the LPF as a functional block

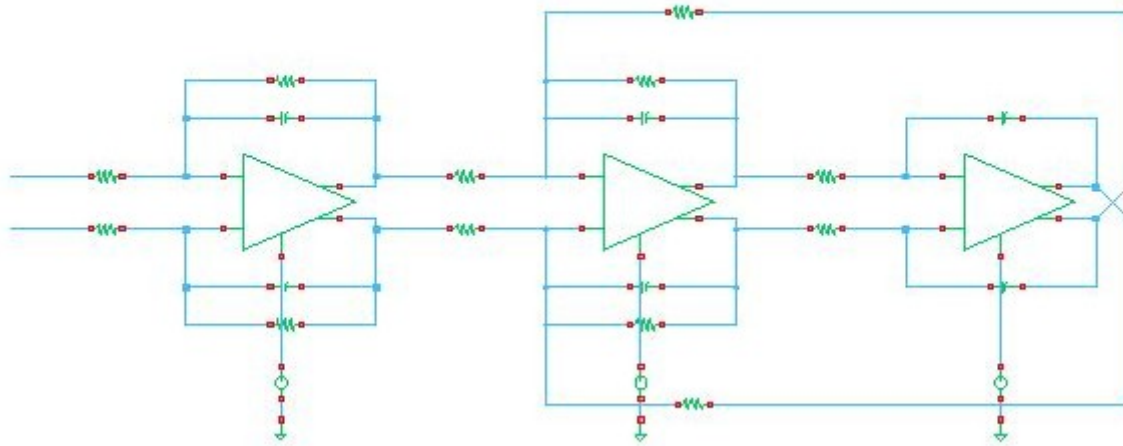


Figure 14: The implementation of the 3rd order chebyshev LPF

AC Response

Name

...6 /net018); ac dB20(V)

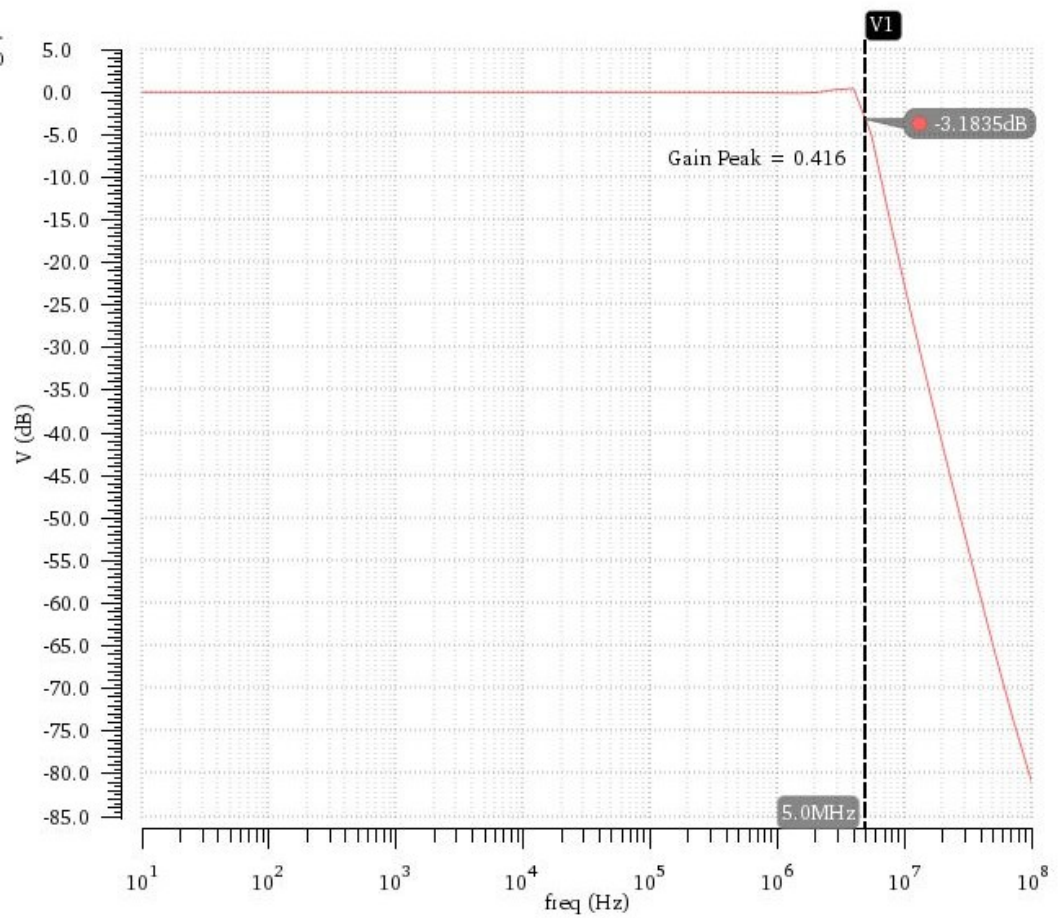


Figure 15: The frequency characteristic of the filter

3. PGA

3.1 Sizing the PGA

3.1.1 Sizing the passive components of the PGA

Requirements: different gain steps (coarse + fine), 0 dB – 20 dB, $BW_{PGA} = 20\text{ MHz}$, $CL = 5\text{ pF}$, linear input of at least 50 mV

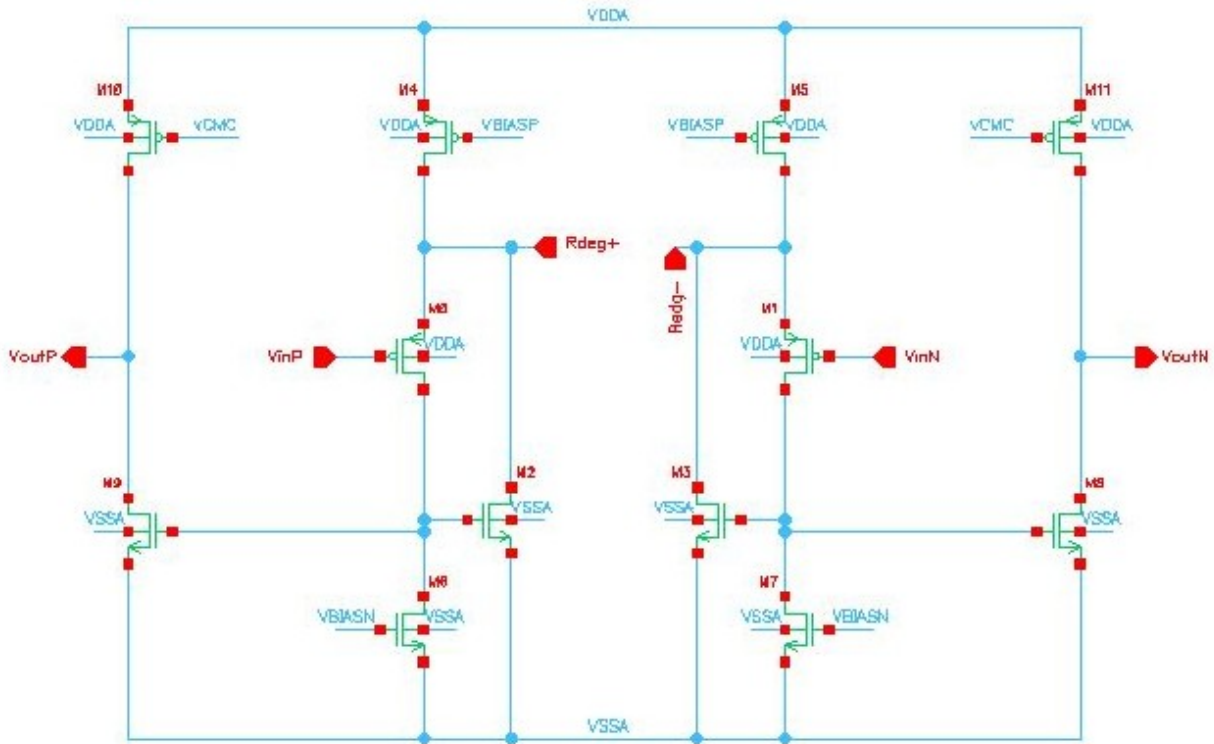


Figure 16: Kwan-Martin transconductor

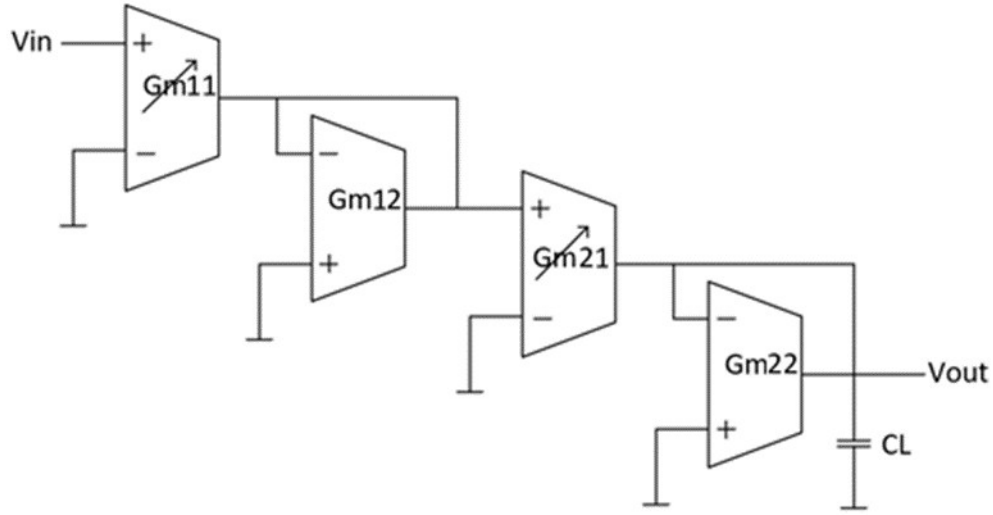


Figure 17: The schematic of the PGA

Where G_{m11} and G_{m12} realize the first stage and G_{m21} and G_{m22} realize the second stage.

The bandwidth of the PGA is given by:

$$BW_{PGA} = \frac{G_{m22}}{2\pi C_L} \quad (30)$$

From the previous equation we can obtain $G_{m22} = 628 \text{ uS}$.

If we consider $G_{m12} = G_{m22}$, then we can compute the values for $G_{m11} = A_{v1} G_{m12}$, and $G_{m21} = A_{v2} G_{m22}$.

Av1 [dB]	Av1 [V/V]	Gm12 [S]	Gm11[S]
0	1	6.28E-04	6.28E-04
6	1.995262	6.28E-04	1.25E-03
12	3.981072	6.28E-04	2.50E-03
18	7.943282	6.28E-04	4.99E-03

Av2 [dB]	Av2 [V/V]	Gm22 [S]	Gm21[S]
0	1	6.28E-04	6.28E-04
1	1.122018	6.28E-04	7.05E-04
2	1.258925	6.28E-04	7.91E-04
3	1.412538	6.28E-04	8.87E-04
4	1.584893	6.28E-04	9.95E-04
5	1.778279	6.28E-04	1.12E-03

Each transconductor is implemented with a Kwan-Martin structure with a variable degeneration resistance. The transconductance is computed as:

$$G_m = \frac{A_{ii}}{R_{deg}} \quad (31)$$

For a current gain $A_{ii}=4$ we obtain the following values for the degeneration resistances.

Av1 [dB]	Rdeg12	Rdeg11
0	6.37E+03	6.37E+03
6	6.37E+03	3.19E+03
12	6.37E+03	1.60E+03
18	6.37E+03	8.02E+02

Av2 [dB]	Rdeg22	Rdeg21
0	6.37E+03	6.37E+03
1	6.37E+03	5.68E+03
2	6.37E+03	5.06E+03
3	6.37E+03	4.51E+03
4	6.37E+03	4.02E+03
5	6.37E+03	3.58E+03

3.1.2 Designing the PGA at transistor level

For sizing the transistor of each G_m cell I used the following design strategy.

1. Having already obtained the values of the degeneration resistance and knowing the required input range of the transconductor I computed the maximum degeneration current as

$$i_{deg_max} = \frac{50e-3}{R_{deg_min}} = 62e-6 \quad (32)$$

2. To ensure that all transistors remain in conduction we have to ensure that $M_{(2,3)}$ have a drain current large enough.

$$I_{DM2,3} > 1.2 i_{deg_max} = 74e-6 \text{ A} \quad (33)$$

3. We can choose $V_{(dsatM2,3)}=150\text{mV}$

4. Note that the other transconductors could have been designed for lower bias currents due to higher R_{deg_min} . If $M_{(2,3)}$ in the actual implementation were realized using 2 cascodes, the same parameters can be used for the cascode transistors.

5. The current through $M_{(0,1)}$ I chose as $100\mu A$ and $V_{dsatM0,1}=150mV$

6. Considering that previously I chose $A_{ii}=4$ it results that the current through $M_{(8,9)}$ and $M_{(10,11)}$ is $2i_{dM2,3}=296\mu A$. $V_{dsatM8,9}$ was chosen $0.150V$ and $V_{dsatM10,11}$ was chosen as $182mV$.

7. If $M_{(8,9)}$ and $M_{(10,11)}$ in the actual implementation were realized using 2 cascodes, the same parameters can be used for the cascode transistors.

8. For $M_{6,7}$ current sources their bias currents are the same as for $M_{0,1}$ of $100\mu A$. While $V_{dsat} = 150mV$. For $M_{4,5}$ current sources its current value is equal to $I_{DM0,1} + I_{DM2,3} = 100\mu A + 74\mu A = 174\mu A$, while $V_{dsat} = 150mV$.

After applying the sizing strategy I obtained the following results for the transistor dimensions.

	ID	VDSAT	gm	W[m]	L[m]	
M2,3	7.40E-05	0.15	9.87E-04	2.49E-06	2.00E-07	NMOS
M0,1	1.00E-04	0.15	1.33E-03	3.07E-05	2.50E-07	PMOS
M6,7	1.00E-04	0.165	1.21E-03	2.78E-06	2.00E-07	NMOS
M8,9	2.96E-04	0.15	3.95E-03	9.95E-06	2.00E-07	NMOS
M10,11	2.96E-04	0.182	3.25E-03	4.93E-05	2.00E-07	PMOS
M4,5	1.74E-04	0.182	1.91E-03	2.90E-05	2.00E-07	PMOS

3.2 Verifying and characterising the PGA

3.2.1 Verifying and characterizing the transconductor

I used the previously obtained dimensions to implement the Kwan-Martin Gm cell. Since the phase margin was not large enough I realised a dominant pole compensation to reduce the corresponding gain peaking by placing a capacitor in the drain of the input transistors.

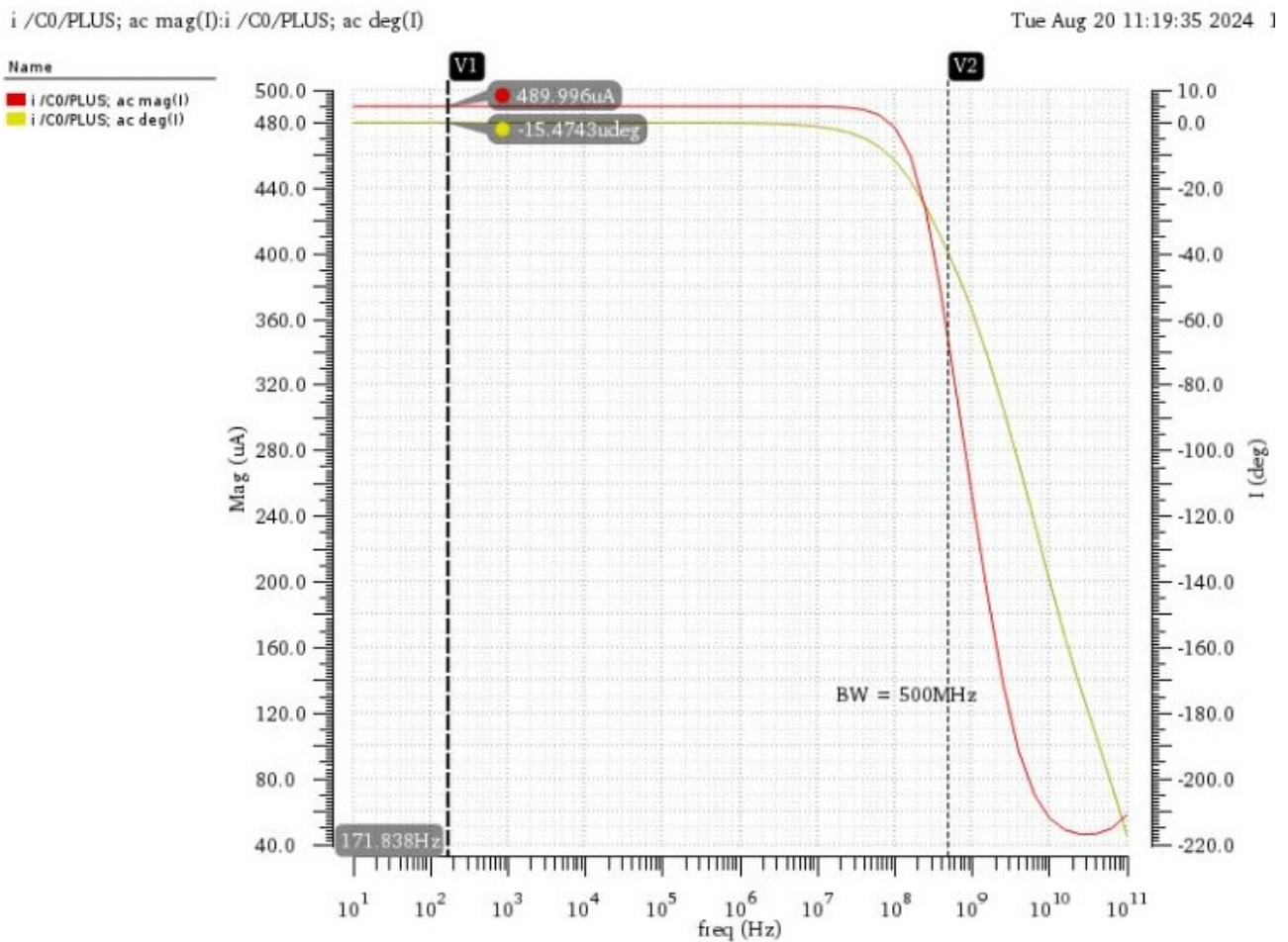


Figure 18: The minimum transconductance necessary

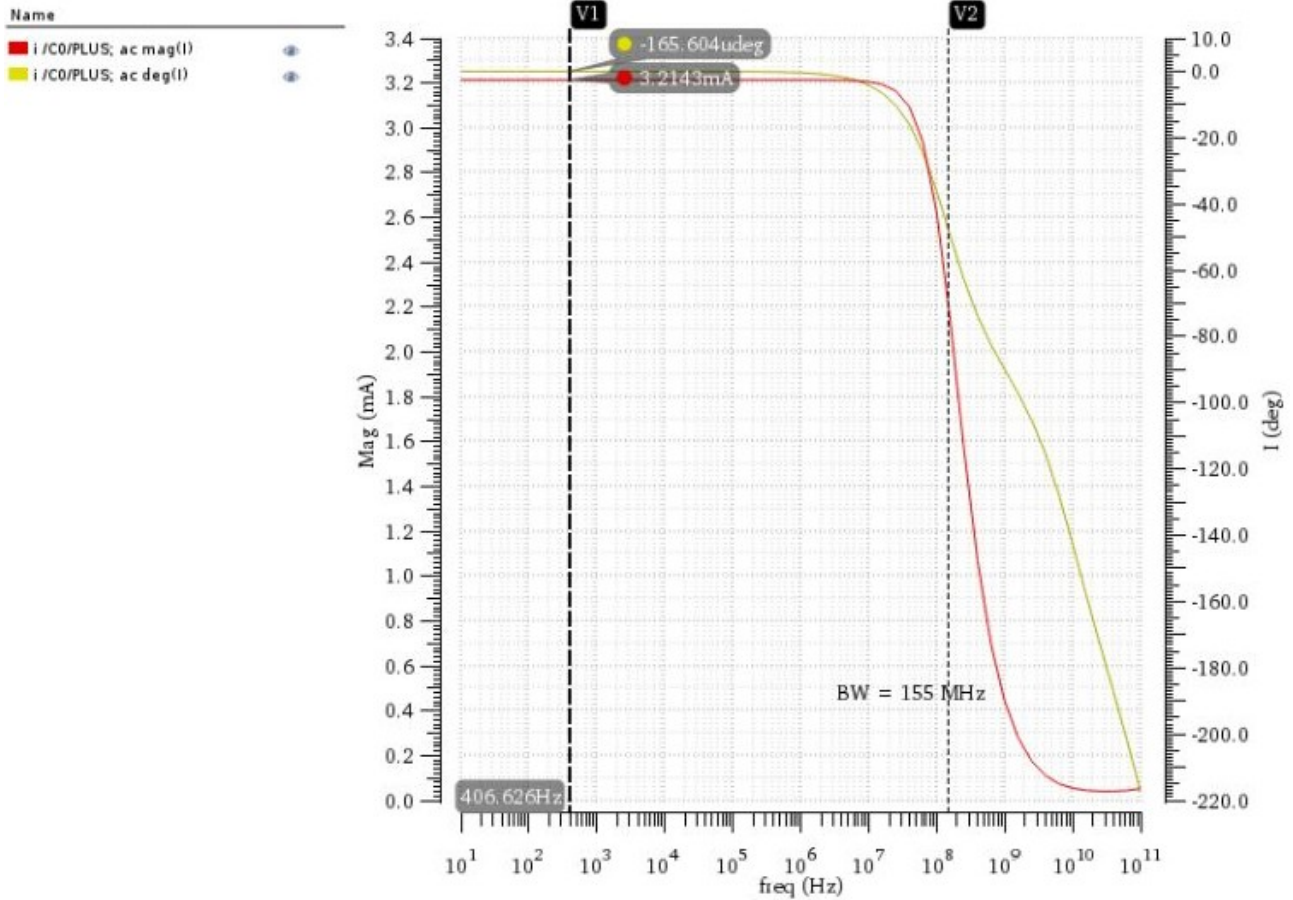
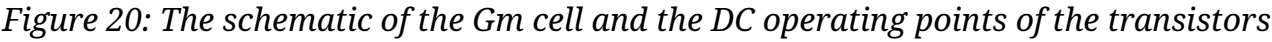


Figure 19: The maximum transconductance necessary

Note that while the original project [1] used cascode's, mine hasn't. Because my output resistance which is around 10k Ohms is much lower than hers the G_m also have errors from the nominal values. The output CM voltage also influence G_m .



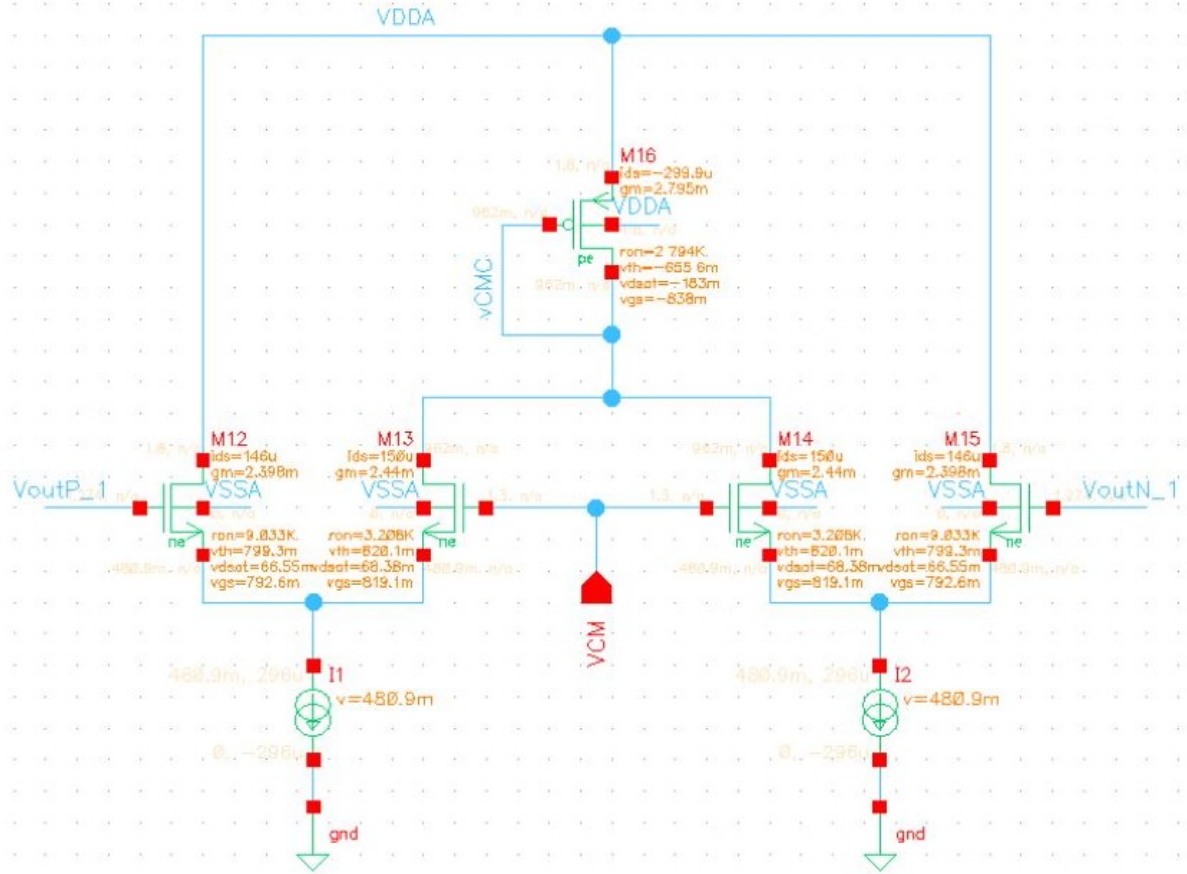


Figure 21: CMFB circuit

For R_{deg} 6.37k, and G_m of 3.21 mS, an input signal of 1 mV with a frequency of 500kHz the THD is 0.397 %, and for an input signal of 50 mV and frequency of 500 kHz for the same G_m , the THD is 0.720 %.

Note that I use a smaller linear input range as the original requirement of 400 mV would have required too large bias currents, and transistor dimensions. (see eq. 20)

VDD[V]	V _{ICM_MIN} [V]	V _{ICM_MAX} [V]	V _{OCM_MIN} [V]	V _{OCM_MAX} [V]	V _{ICM_MED} [V]	V _{OCM_MED} [V]
1.8	0.041	0.671	0.153	1.618	0.356	0.885

3.2.2 Verifying and characterizing the PGA as a functional block

// I had to modify $M_{8,9}$ had $\frac{W}{L} = \frac{10\mu}{200n}$ with $r_{ds} = 11k \rightarrow \frac{W}{L} = \frac{44\mu}{900n}$ with $r_{ds} = 98k$ to increase the output resistance, for a better G_m reproducibility. $M_{10,11}$ have $r_{ds} = 50k$.

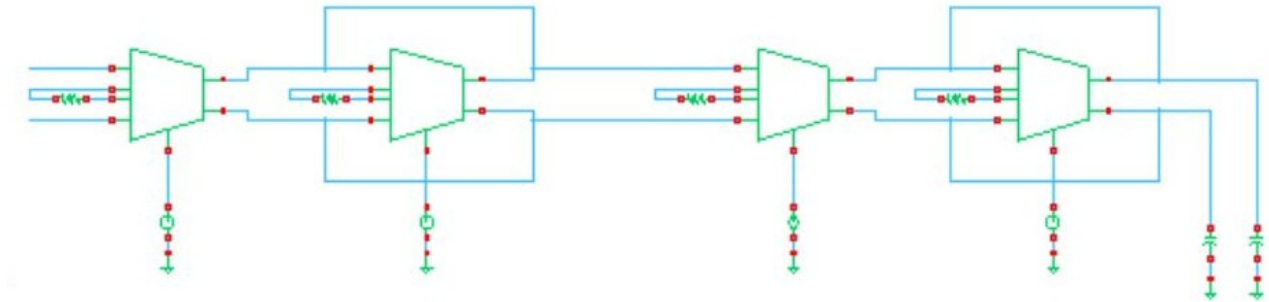


Figure 22: The implementation of the PGA

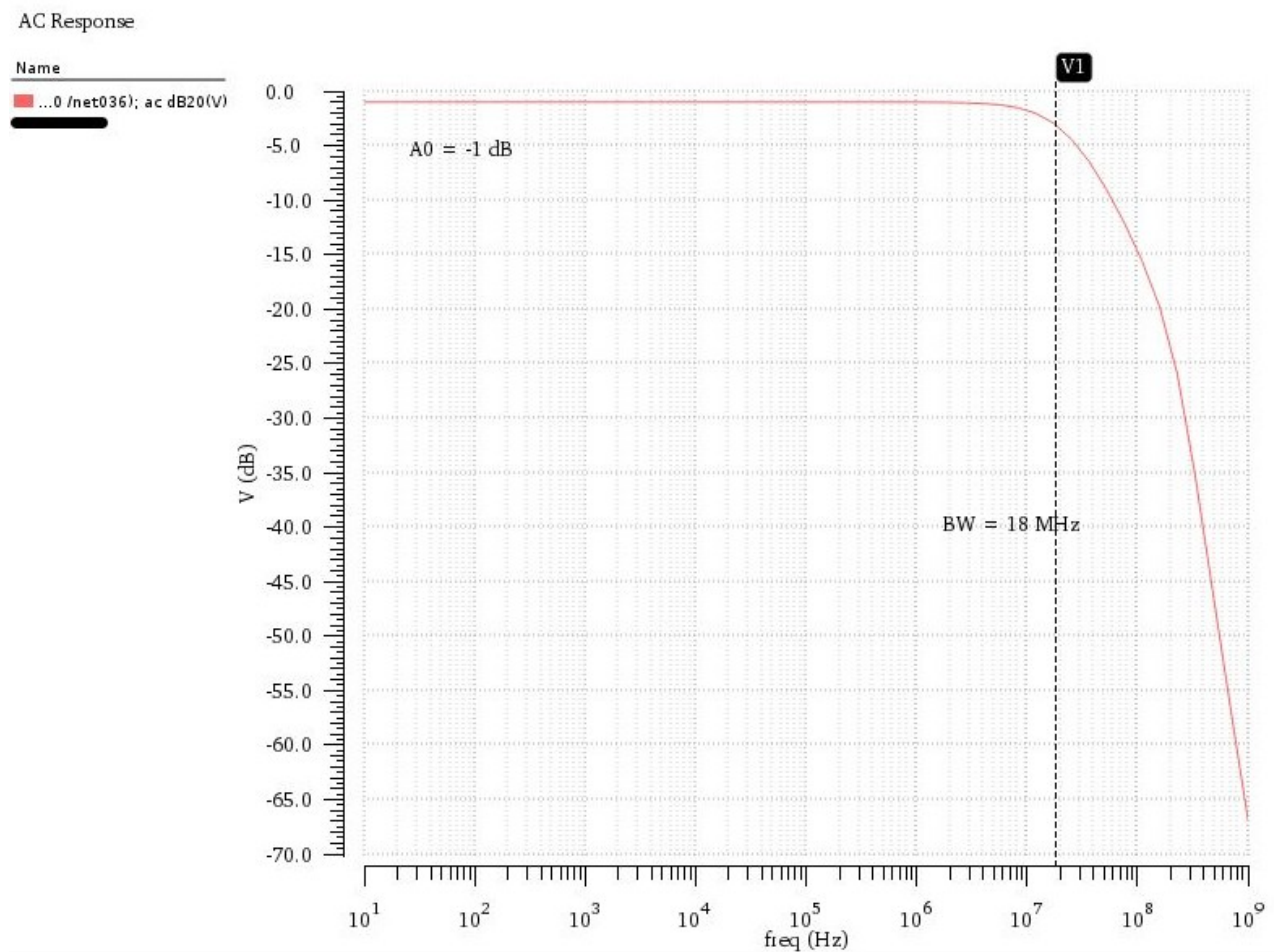


Figure 23: The frequency characteristic for the minimum gain

Here we can see that instead of 0 dB I am getting -1 dB. This could be an issue with the CM output voltage being too low for all transconductors. IF VCM is 0.4 V then the error is -1.15 dB.

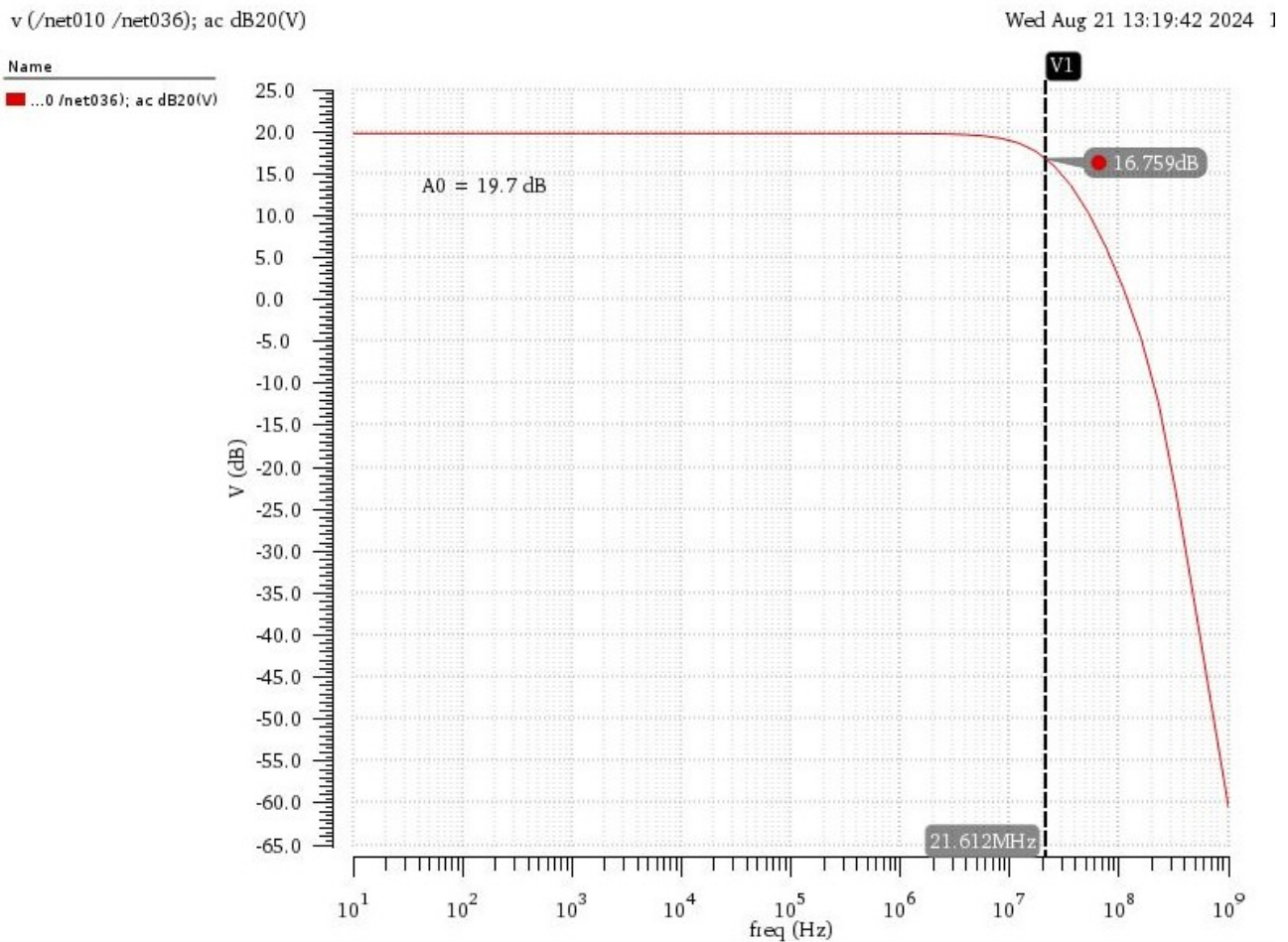


Figure 24: The frequency characteristic for the maximum gain

4. Verifying and characterizing LPF + PGA

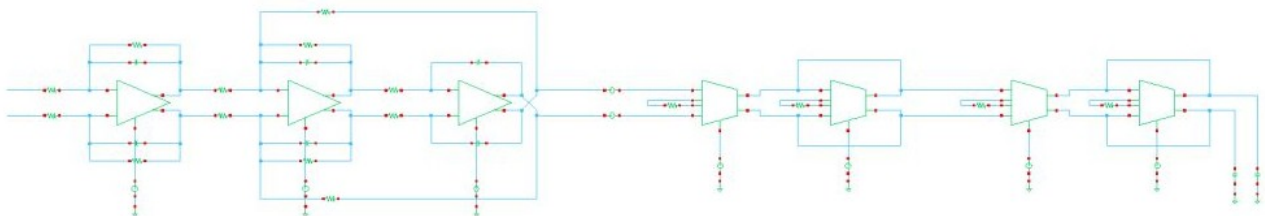


Figure 25: The schematic implementation

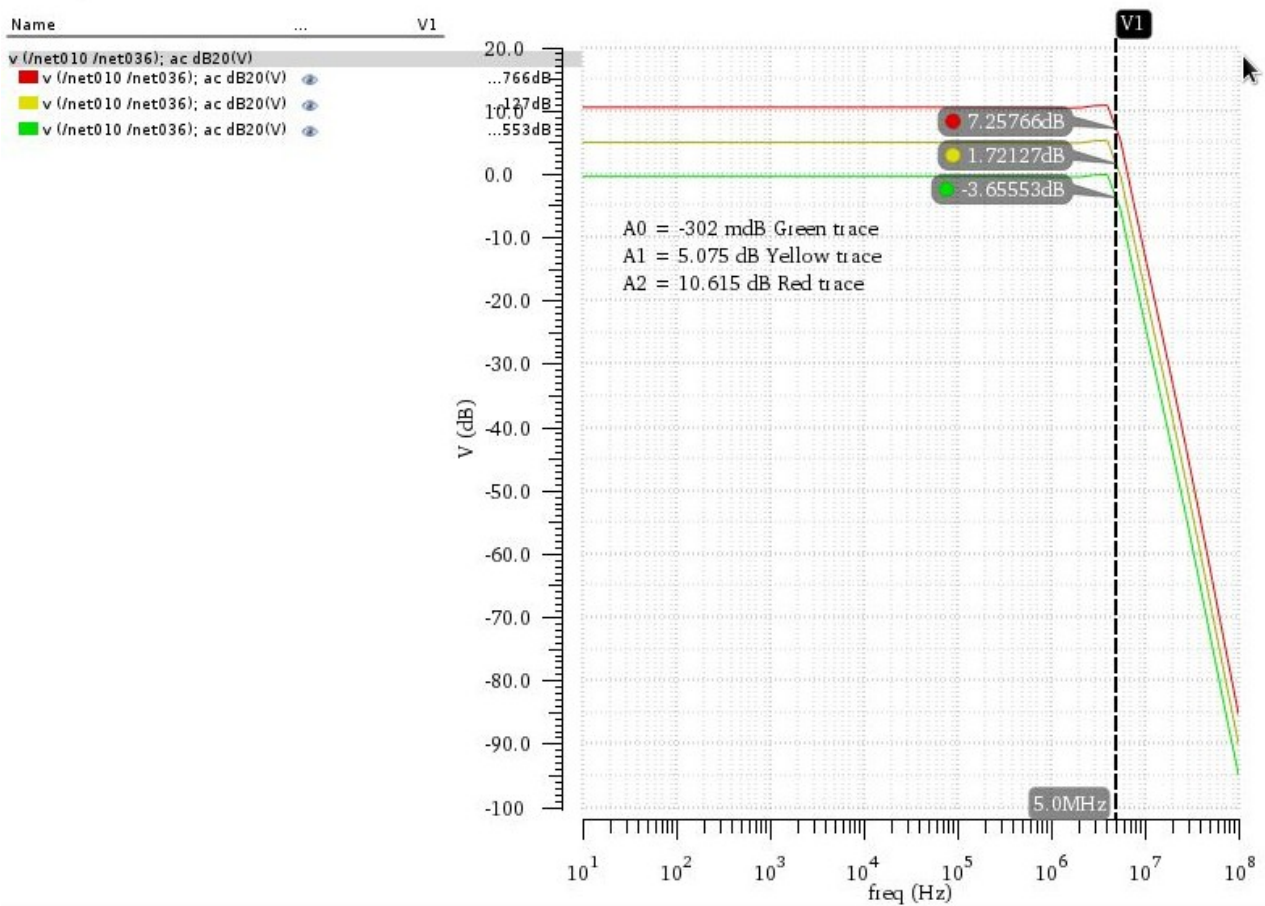


Figure 26: Frequency characteristic

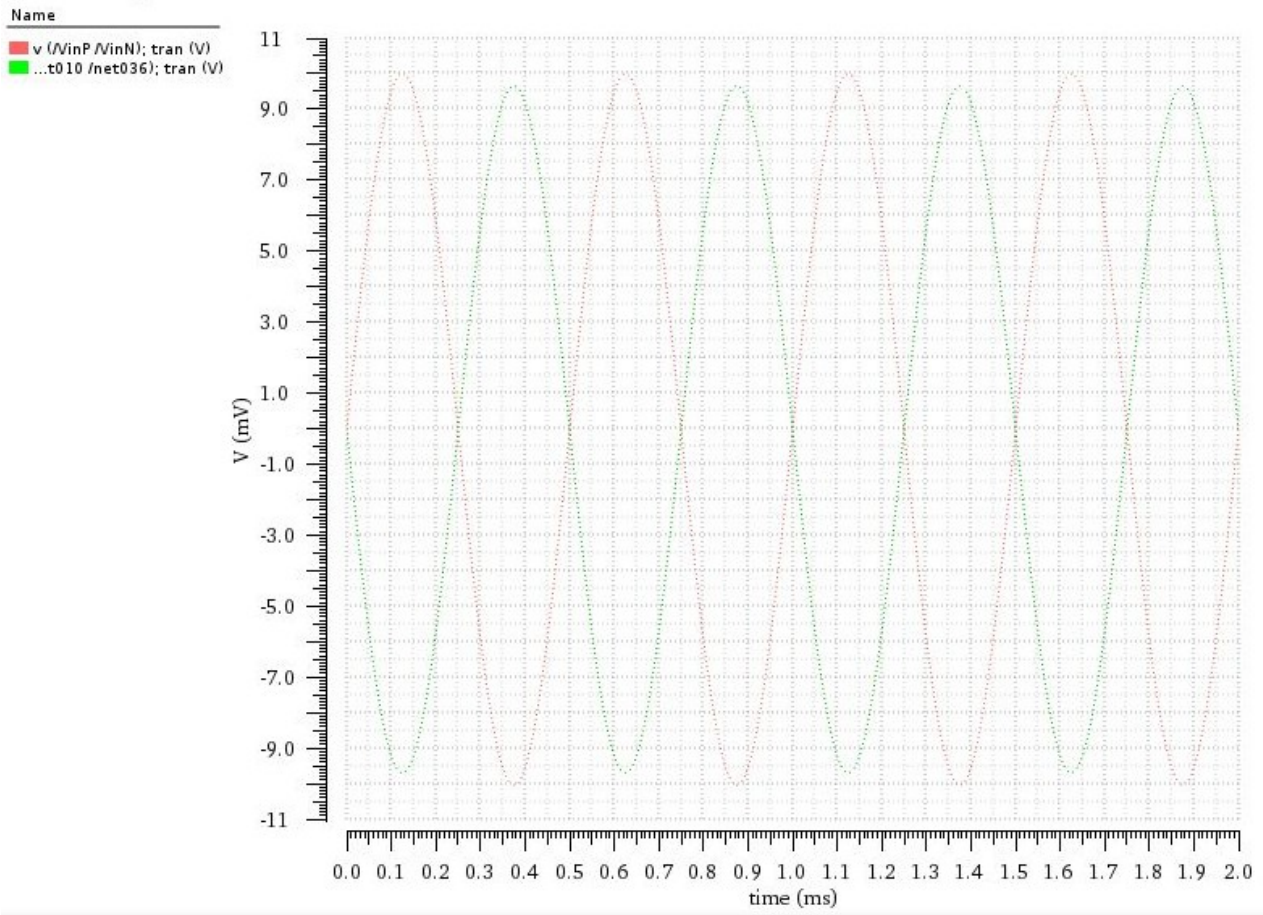


Figure 27: Transient response for minimum gain

Transient Response

Name

■ v (/VinP /VinN); tran (V)
■ ...t010 /net036); tran (V)

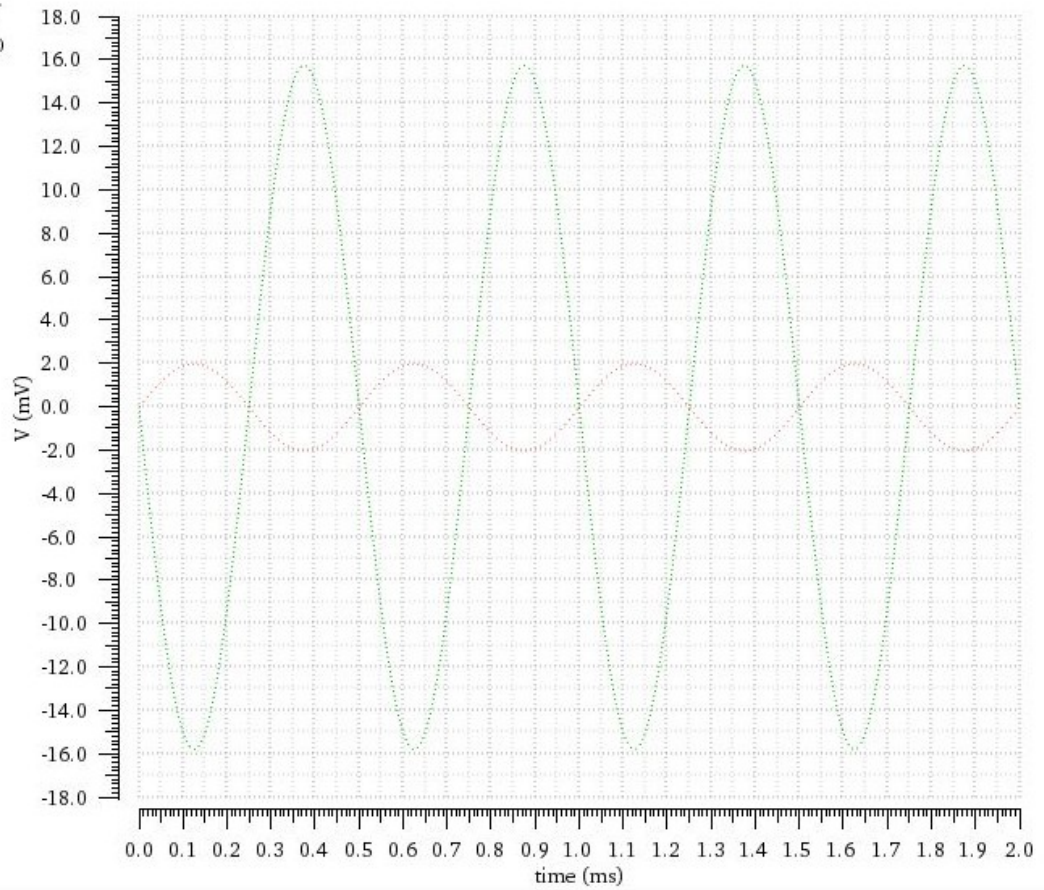


Figure 28: Transient response for maximum gain

5. LPF-AO Miller Modifications

Because of the initial CMFB circuit used in AO Miller to control the tail current source, seemingly the circuit would struggle to find the DC operating point with a feedback circuit. In this regard the CMF has been changed to drive the active loads of the differential pair.

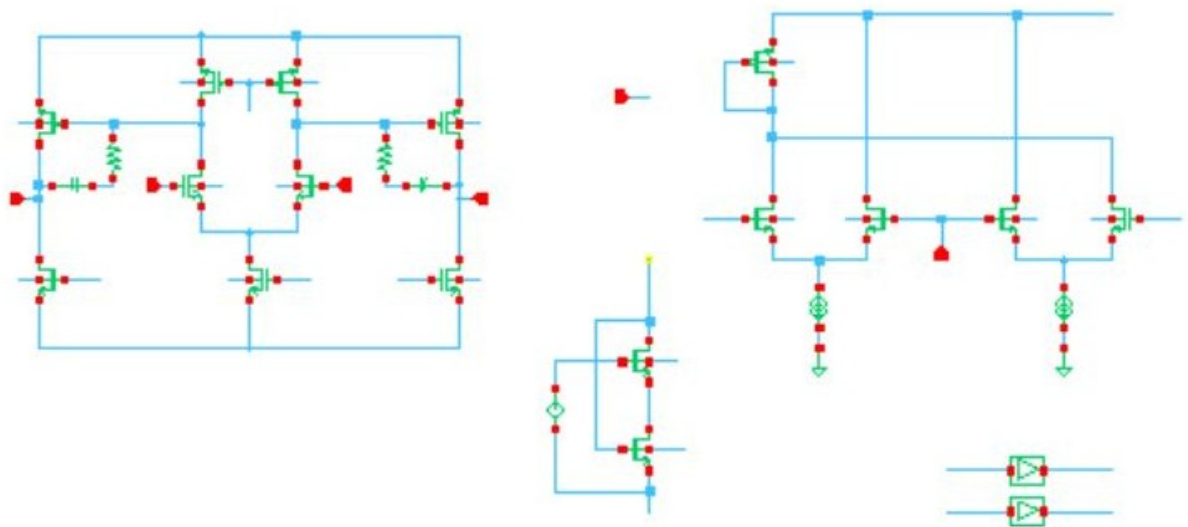


Figure 29: AO Miller and CMFB

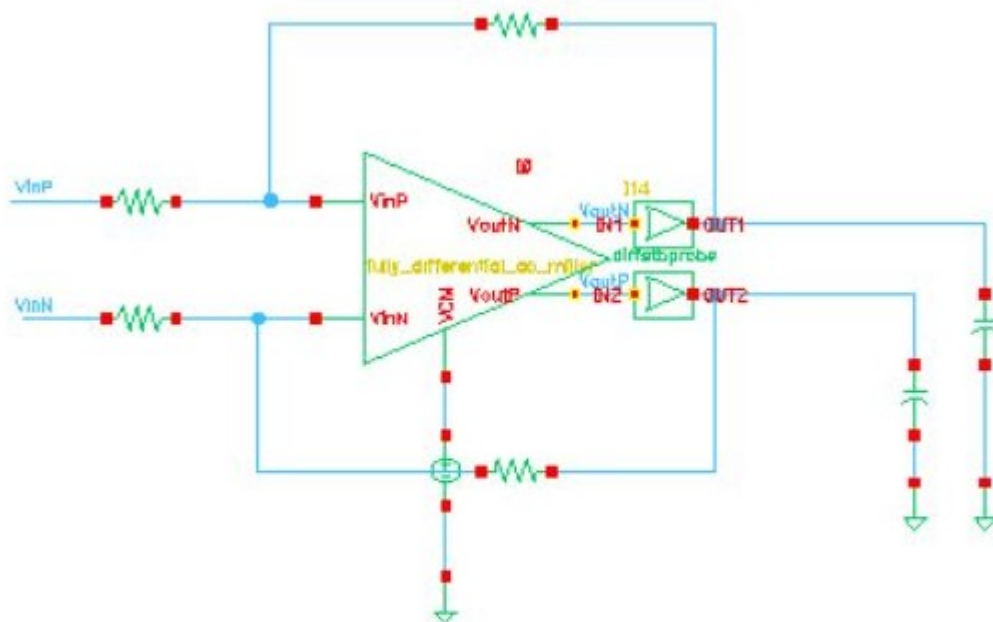


Figure 30: AO Miller TB

Bibliography

[1]