flyback 85 – 275 VRMS 5V at 6A 30W design notes (120 (i.e. 85*sqrt(2)) – 388 Vpp)

the rectifier bridge

Vmin is usually selected around 25 to 30% of the minimum peak line voltage - for instance, if the converter operates down to 85VRMS, then Vmin can be chosen around

$$(85\cdot\sqrt{2})\cdot 0.7 = 84\,Vdc$$

(the power supply, a flyback, delivers 30W (Pconv) to a given load with an estimated efficiency of 85%)

(85 – 275 VRMS 47 – 63 Hz Vmin = 80 Vdc

T = 45 C MAX

tc the diode conduction time, longest at lowest line input

$$t_c = \frac{1}{4\cdot F_{line}} - \Delta t = \frac{1}{4\cdot F_{line}} - \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{1}{4\cdot 60} - \frac{\sin^{-1}\frac{80}{85\cdot\sqrt{2}}}{2\cdot 3.14\cdot 60} = 4.16\text{e-}3 - \frac{7.28\text{e-}1}{377} = 2.22\text{e-}3\,s$$

the discharge time is evaluated by

$$t_d = \frac{1}{2\cdot F_{line}} - t_c = \frac{1}{2*60} - 2.2\text{e-}3 = 6.13\text{e-}3\,s$$

$$C_{bulk} \geq \frac{2P_{out}}{\eta(V_{peak}^2 - V_{min}^2)}\cdot t_d = \frac{2\cdot 35}{0.85(120^2 - 80^2)}\cdot 6.1\text{e-}3 = 62.79\,uF$$

the final capacitor selection is always based on the rms current flowing through it

$$I_{Cbulk,rms} = \frac{P_{out}}{\eta V_{bulk,avg}}\sqrt{\frac{2}{3F_{line}t_c} - 1} = \frac{35}{0.85\left(\frac{120+80}{2}\right)}\sqrt{\frac{2}{3\cdot 60\cdot 2.2\text{e-}3} - 1} = 828\,mA$$

the capacitor needs to permanently sustain a steady – state voltage of 275 * sqrt(2) = 388 Vdc → hence, a 400V type is mandatory

Kemet 47uF/450V ESU476M450AM3
Iripple at 100 kHz and 105 C 880 mArms
ripple coefficient at 50 Hz 0.5 → 0.5 * 880 mArms = 440 mArms
tan δ = 0.2 then

$$ESR = \frac{\tan\delta}{2\pi f C} = \frac{0.2}{6.28\cdot 120\cdot 47e-6} = 5.64\,\Omega$$

D x L (mm) 16 x 36

SELECT 2 * 47 uF = 94 uF

now that we have selected 2 * 47 uF, the various times also need to be updated, and from Cbulk eq. we have

$$V_{min} = \sqrt{\frac{\eta C_{bulk} V_{peak}^2 - 2P_{conv}t_d}{C_{bulk}\eta}} = \sqrt{\frac{0.85\cdot 94u\cdot 120^2 - 2\cdot 35\cdot 6.1\text{e-}3}{94u\cdot 0.85}} = 95.16\,V$$

results

$$t_c = \frac{1}{4\cdot F_{line}} - \Delta t = \frac{1}{4\cdot F_{line}} - \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{1}{4\cdot 60} - \frac{\sin^{-1}\frac{95.16}{85\cdot\sqrt{2}}}{2\cdot 3.14\cdot 60} = 4.16\text{e-}3 - \frac{0.913}{377} = 1.73\text{e-}3\,s$$

$$t_d = \frac{1}{2\cdot F_{line}} - t_c = \frac{1}{2*60} - 1.73\text{e-}3 = 6.6\,ms$$

the capacitor peak curent can be evaluated

$$I_{Cbulk,peak} = 2\pi Fline\, C_{bulk} V_{peak} \cos(2\pi F_{line}\Delta t)$$

$$where\ \Delta t = \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{\sin^{-1}\frac{95.16}{85\cdot\sqrt{2}}}{2\pi 60} = 2.42\text{e-}3\,s$$

$$I_{Cbulk,peak} = 6.28\cdot 60\cdot 94\,u\cdot(85\sqrt{2})\cos(6.28\cdot 60\cdot 2.42\text{e-}3) = 2.6\,A$$

$$I_{Cbulk,peak\,for\,47uF} = 6.28\cdot 60\cdot 47\,u\cdot(85\sqrt{2})\cos(6.28\cdot 60\cdot 2.42\text{e-}3) = 1.3\,A$$

$$I_{Cbulk,rms} = \frac{P_{out}}{\eta V_{bulk,avg}}\sqrt{\frac{2}{3F_{line}t_c} - 1} = \frac{35}{0.85\left(\frac{120+80}{2}\right)}\sqrt{\frac{2}{3\cdot 60\cdot 1.73\text{e-}3} - 1} = 958\,mA$$

the diode peak current is by

$$I_{d,peak} = I_{out} + I_{Cbulk,peak} = \frac{P_{out}}{\eta}\frac{2}{V_{min}+V_{peak}} + I_{Cbulk,peak} = \frac{35}{0.85}\frac{2}{95+120} + 2.6 = 2.98\,A$$

$$I_{d,rms} = \frac{P_{conv}}{\eta V_{bulk,avg}\sqrt{3F_{line}t_c}} = \frac{35}{0.85\left(\frac{120+95}{2}\right)\sqrt{3\cdot 60\cdot 1.73\text{e-}3}} = 686\,mArms$$

$$I_{d,avg} = \frac{P_{conv}}{2\eta V_{bulk,avg}} = \frac{35}{2\cdot 0.85\left(\frac{120+95}{2}\right)} = 191\,mA\ then\ P_{d,avg} \approx V_f\cdot I_{d,avg} \approx 0.7\cdot 0.191 = 134\,mW$$

diodes such as the ON Semiconductor 1N5406 (600V/3A) are well suited for this application

the rms input current also needs to be known to select the right fuse

$$I_{in,rms} = \frac{\sqrt{2}P_{conv}}{\eta V_{bulk,avg}\sqrt{3F_{line}t_c}} = \frac{\sqrt{2}\cdot 35}{0.85\left(\frac{120+95}{2}\right)\sqrt{3\cdot 60\cdot 1.73\text{e-}3}} = 0.97\,Arms$$

a 250 Vrms/3.15 A delayed type (a time-delay type is necessary because of the large in-rush current at power-on)

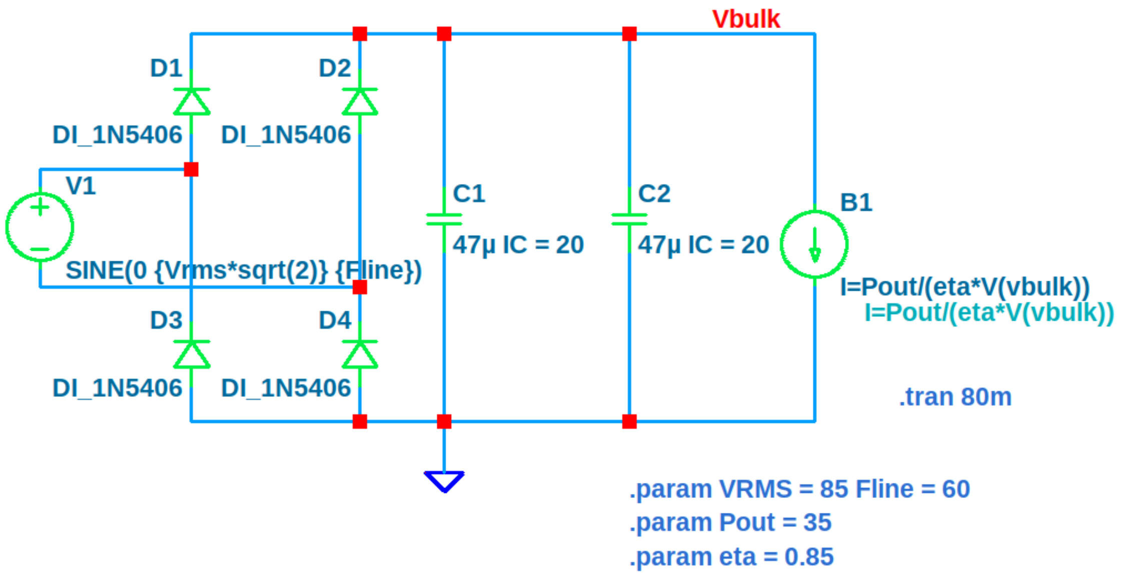
SR-5-6.3A-AP Bussman/Eaton → (optional)

$$PF = \frac{V_{bulk,avg}}{V_{in,rms}}\sqrt{\frac{3}{2}F_{line}t_c} = \frac{107.5}{85}\sqrt{\frac{3}{2}\cdot 60\cdot 1.73\text{e-}3} = 0.499$$

→ the power factor gives information about the input energy spread over the mains period. With narrow input spikes, the instantaneous energy remains confined in the vicinity of the peak, inducing a high rms and peak current

$$then\, I_{in,rms} = \frac{P_{out}}{\eta V_{in\,min,rms} \cdot PF} = \frac{35}{0.85 \cdot 85 \cdot 0.499} = 970.8\, mArms$$

SPICE SIMULATION

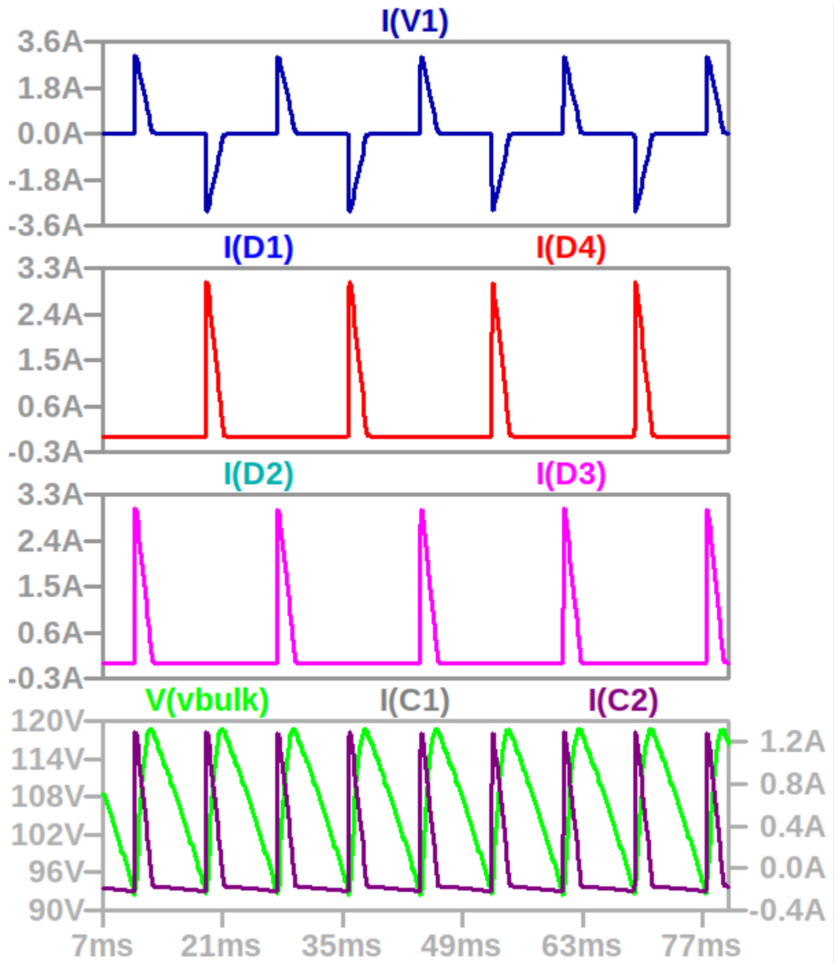


Note the initial condition on the capacitor which avoids a SPICE division by zero when the capacitor is totally discharged at power on.

(to measure the power factor, measure the rms input current and multiply it by the input voltage 85 Vrms. This gives us the VA. The average input power is found by multiplying vmains(t) by iin(t), you have pin(t) and average over one period, and you obtain watts)

$$PF = \frac{v_{mains}(t) \cdot i_{mains}(t)}{V_{in\,rms} \cdot I_{in\,rms}} = \frac{42.95\, W}{85 \cdot 908e\text{-}3} = \frac{42.95\, W}{77.18\, VA} = 0.556$$

(this is a poor value, typical of a full-wave application)



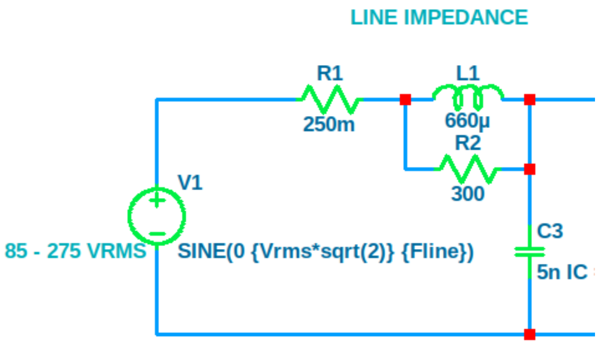
SIMULATIONS CONDITIONS (85 VRMS 60 Hz FLINE)

	EQUATIONS	SPICE
Vmin	95.16 V	92.63 V
Vbulk_avg	107.5 V	107 V
tc	1.73e-3s	1.83e-3s
td	6.6e-3s	6.2e-3s
Icbulk_peak	1.3 A	1.29 A
Icbulk_rms	0.479 Arms	0.405 Arms
Idpeak	2.98 A	2.91 A
Idrms	0.686 Arms	0.636 Arms
Idavg	0.191 A	0.195 A
I_inrms	0. Arms	0. Arms

SIMULATIONS CONDITIONS (240 VRMS 50 Hz FLINE)

	EQUATIONS	SPICE
Vmin		326 V
Vbulk_avg		332 V
tc		927e-6s
td		8.69e-3s
Icbulk_peak		1.24 A
Icbulk_rms		0.275 Arms
Idpeak		2.58 A
Idrms		0.350 Arms
Idavg		0.069 A
I_inrms		0. Arms

(it is important to note that all the above equations are assuming a perfectly sinusoidal input voltage source (for simplicity), featuring a low output impedance. In reality, the mains is often distorted and because of the EMI filter presence, the output impedance varies quite a bit. Final results captured on the bench might differ from the above calculations.)



(single output) flyback analysis

Vinmin	85 Vrms
Vbulkmin	90 Vdc (considering 25% ripple on the bulk capacitor)
	$i.e.,0.75(85\sqrt{2})$
Vinmax	265 Vrms
Vbulkmax	375 Vdc
	$i.e.,265\sqrt{2}$
Vout	5 V
Vripple ΔV	250 mV
Vout drop	0.25 V maximum from Iout = 0.5 to 6 A in 10 us
Ioutmax	6 A
MOSFET derating factor k_D	0.85
Diode derating factor k_d	0.5
RCD clamp diode overshoot Vos	20 V

fsw	65 kHz

CCM CM (at least at VINMIN)

(derived from the buck-boost converter)

$$L=\frac{\eta V_{bulk,min}^{2}\left(\frac{V_{out}+V_f}{N}\right)^2}{\delta I_r F_{sw} P_{out}\left(V_{bulk,min}+\left(\frac{V_{out}+V_f}{N}\right)\right)\left(\left(\frac{V_{out}+V_f}{N}\right)+\eta V_{bulk,min}\right)}$$

$$\delta I_r=\frac{\Delta I_L}{I_{L,avg}}(=0.85)$$

$$where\, V_{bulk,min}=95\, Vdc$$

600-V MOSFET

- transformer coupling kc of 1.5 (reasonable)

$$N=\frac{N_S}{N_P}=\frac{k_c(V_{out}+V_f)}{BV_{dss}k_D-V_{os}-V_{bulk,max}}=\frac{1.5(5+0.6)}{600\cdot 0.85-20-375}=0.073$$

SELECT N = 0.075

$$L=\frac{0.85\cdot 95^2\left(\frac{5.6}{0.075}\right)^2}{0.85\cdot 65k\cdot 30\left(95+\left(\frac{5.6}{0.075}\right)\right)\left(\left(\frac{5.6}{0.075}\right)+0.85\cdot 95\right)}=978\, uH$$

$$I_{\mathrm{in},avg}=I_{L,avg}\cdot D$$

$$I_{\mathrm{in},avg}=\frac{P_{out}}{\eta V_{min}}=\frac{30}{0.85\cdot 95}=0.371\, A$$

$$D_{max}=\frac{V_{out}}{V_{out}+N\,V_{min}}=\frac{5}{5+0.075\cdot 95}=0.412$$

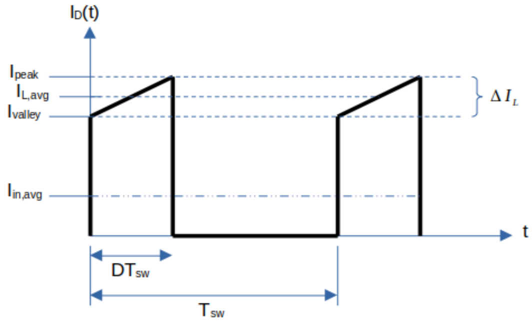
$$\Rightarrow I_{L,avg}=\frac{I_{\mathrm{in},avg}}{D_{max}}=\frac{0.371}{0.412}=0.9\, A$$

$$then$$

$$\Delta I_L=I_{L,avg}\,\delta I_r=0.9\cdot 0.85=0.765\, mA$$

$$I_{peak}=I_{L,avg}+\frac{\Delta I_L}{2}=I_{L,avg}\left(1+\frac{\delta I_r}{2}\right)=0.9\left(1+\frac{0.85}{2}\right)=1.28\,A$$

$$I_{valley}=I_{L,avg}-\frac{\Delta I_L}{2}=I_{L,avg}\left(1-\frac{\delta I_r}{2}\right)=0.9\left(1-\frac{0.85}{2}\right)=0.517\,A$$



-> the inductor current in continuous conduction mode

$$t=0\rightarrow i_{Lp}(t)=I_{valley}=I_{peak}-\Delta I_L$$

$$t=DT_{SW}\rightarrow i_{Lp}(t)=I_{valley}+\Delta I_L$$

$$i_{Lp}(t)=I_{valley}+\Delta I_L\frac{t}{DT_{SW}}=I_{peak}-\Delta IL+\Delta I_L\frac{t}{DT_{SW}}$$

$$then\, I_{L,rms}=\sqrt{\frac{1}{T_{SW}}\int_0^{DT_{sw}} I_{peak}-\Delta IL+\Delta I_L\frac{t}{DT_{SW}}}=\sqrt{D\left(I_{peak}^2-I_{peak}\Delta I_L+\frac{\Delta I_L^2}{3}\right)}$$

→ we have the final rms current circulating in the transformer primary, the MOSFET, and the sense resistor:

$$I_{L,rms}=\sqrt{D\left(I_{peak}^2-I_{peak}\Delta I_L+\frac{\Delta I_L^2}{3}\right)}=\sqrt{0.412\left(1.28^2-1.28\cdot 0.765+\frac{0.765^2}{3}\right)}=0.593\,mArms$$

MOS REF	MANUFACTURER	RDS(on)	BVDSS	QG
SPP11N60C3	INFINEON	0.38	650 V	60 nC

$$P_{cond}=I_{D,rms}^2\cdot R_{DS(on)@Tj=110C}=0.593^2\cdot 0.6=0.21\,W$$

$$P_{SWON}=\frac{I_{valley}\left(V_{bulk}+\frac{(V_{out}+V_f)}{N}\right)\Delta t}{6}F_{SW},$$ where Δt is the overlap time where V_DS (t) transitions from the plateau voltage to zero and i_D (t) transitions from zero to valley level

$$P_{MOSFET}=P_{cond}+P_{sw,on}+P_{sw,off}$$

$$P_{drv}=F_{SW}Q_G V_{cc}=65k\cdot 60n\cdot 15=59\,mW$$

(assume the voltage image across Rsense of the primary current reaches 1 V)

$$R_{sense}=\frac{1V}{I_{peak}}$$

We need a peak current of 1.28 A. Considering a design margin of 10% (Ipeak = 1.4 A), the sense resistor value equals

$$R_{sense}=\frac{1V}{1.4}=0.71\Omega$$

$$P_{sense}=I_{D,rms}^2\cdot R_{sense}=0.593^2\cdot 0.7=0.24\,W$$

$$R_{clp}=\frac{(k_c-1)[2k_c(V_{out}+V_f)^2]}{N^2 F_{SW} L_{leak} I_{peak}^2}=\frac{(1.5-1)[2\cdot 1.5(5+0.6)^2]}{0.075^2\cdot 65k(0.01\cdot 978u)1.4^2}=6.71k$$

$$C_{clp}=\frac{k_c(V_{out}+V_f)}{N R_{clp} F_{sw}\Delta V}=\frac{1.5(5+0.6)}{0.075\cdot 6.71k\cdot 65k\cdot 12}=21.4\,nF$$

ΔV is the selected ripple in percentage of the clamp voltage; 12 V roughly corresponds to 10% of the clamp voltage (≈ 117 V).

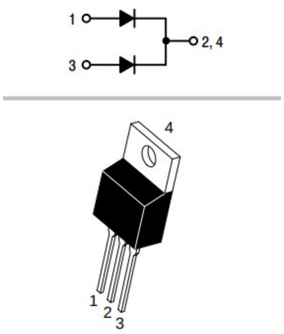
$$P_{Rclp}=\frac{1}{2}F_{sw}L_{leak}I_{peak}^2\frac{k_c}{k_c-1}=\frac{1}{2}65k\cdot(0.01\cdot 978u)1.4^2\frac{1.5}{1.5-1}=1.86\,W$$

CLAMP DIODE MUR160

the secondary-side diode

$$PIV=NV_{bulk,max}+V_{out}=0.075\cdot 375+5=28.12+5=33\,V$$

With a diode voltage derating factor kd of 50%, select a diode featuring a 100-V VRRM and accepting at least Ipeak_pri/N (i.e., 1.4/0.075 = 19 A) . (Its average current is nothing more than the direct output current.) An MBR20100CTG in a TO-220 package could be a possible choice.



TO−220
CASE 221A
STYLE 6

VRM	100 V
IF(AV)	10 A
IFRM	20 A (peak repetitive forward current)
Vf	0.8 V maximum at Tj = 125 C and IFAVG = 10 A
Ir	2 mA at Tj = 150 C and Vr = 40 V

$$P_d = V_{T0} I_{d,avg} + R_d I^2_{d,rms} + DI_r PIV \approx V_f I_{d,avg} = 0.8\,V \cdot 3\,A = 2.4\,W$$

In the above equation, we assumed an equal current sharing between both diodes as they sit on the same die. The total power dissipation is thus twice previous eq. states: 4.8 W. A heat sink is necessary.

$$T_j - T_A = P\left(R_{\Theta J-C} + R_{\Theta C-H} + R_{\Theta H-A}\right)$$

the thermal resistance our heatsink will need is

$$R_{\Theta H-A} = \frac{T_{j,max} - T_A}{P} - R_{\Theta J-C} - R_{\Theta C-H} = \frac{150-70}{4.8} - 2 - 1 = 13.6\,C/W$$

Our diode junction when operated at a 70°C ambient temperature will thus theoretically increase up to

$$T_j = T_A + PR_{\Theta J-A} = 70 + 4.8(13.6+1+2) = 149.68\,C$$

For the capacitor selection, (as for a DCM design) we consider the ESR as the dominant term

$$I_{sec,peak} = \frac{I_{peak}}{N} = \frac{1.4}{0.075} = 18.6\,A$$

$$\textit{based on this number } R_{ESR} \leq \frac{V_{ripple}}{I_{sec,peak}} \leq \frac{0.25}{18.6} = 13.4\,m\Omega$$

(SELECT) MAL217256471E3 – 25 V – 470 uF
D x L (mm) 10 x 12 RADIAL TYPE
RESR = 48 mΩ at TA = 20 C and 100 kHz
ICRMS = 1.7 A at 100 kHz and 105 C

https://www.vishay.com/docs/28499/172rlx.pdf

$$I^2_{Cout,rms} + I^2_{out,avg} - I^2_{sec,rms} = 0 \; then \; I^2_{Cout,rms} = I^2_{sec,rms} - I^2_{out,avg}$$

$$I_{sec,rms} = \sqrt{(1-D_{max})\left(I^2_{sec,peak} - I_{sec,peak}\frac{\Delta I_L}{N} + \frac{\Delta I_L^2}{3N^2}\right)}$$

$$= \sqrt{(1-0.412)\left(18.6^2 - 18.6\frac{0.765}{0.075} + \frac{0.765^2}{3 \cdot 0.075^2}\right)} = 10.6\,A$$

$$I_{Cout,rms} = \sqrt{10.6^2 - 6^2} = 8.73\,Arms$$

→ given the individual rms capability of each capacitor (1.7 A at 105°C), we need to put five of them in parallel for a total capability of 8.73 Arms. (A final bench measurement at the minimum input voltage and maximum current will indicate if the capacitor temperature is within safe limits or not.)

$$\rightarrow R_{ESR,total} = \frac{48\text{e-}3}{5} = 9.6\,m\Omega < 13.4\,m\Omega$$

total loss incurred by this resistive path amounts to

$$P_{Cout}=I^2_{Cout,rms}\cdot R_{ESR}=8.73^2\cdot 9.6\text{e-}3=0.731\,W$$

Lp	978 uH
Rsense	0.71 Ω
N	0.075 i.e, NS/NP
Cout	2350 uF
Resr	9.6 mΩ
Rload	5 V/6 A

AC ANALYSIS

$$f_c \approx \frac{\Delta I_{out}}{2\pi \Delta V_{out} C_{out}} = \frac{5.5}{6.28\cdot 0.25\cdot 2350\text{e-}6} = 1.49\,kHz$$

$$RHPZ\, f_{z2} = \frac{(1-D)^2 R_{load}}{2\pi D L_p N^2} = \frac{(1-.412)^2\cdot 0.833}{6.28\cdot 0.412\cdot 978u\cdot 0.075^2} = 20.23\,kHz$$

-> we are operating at a crossover frequency below the 20% of the RHPZ location

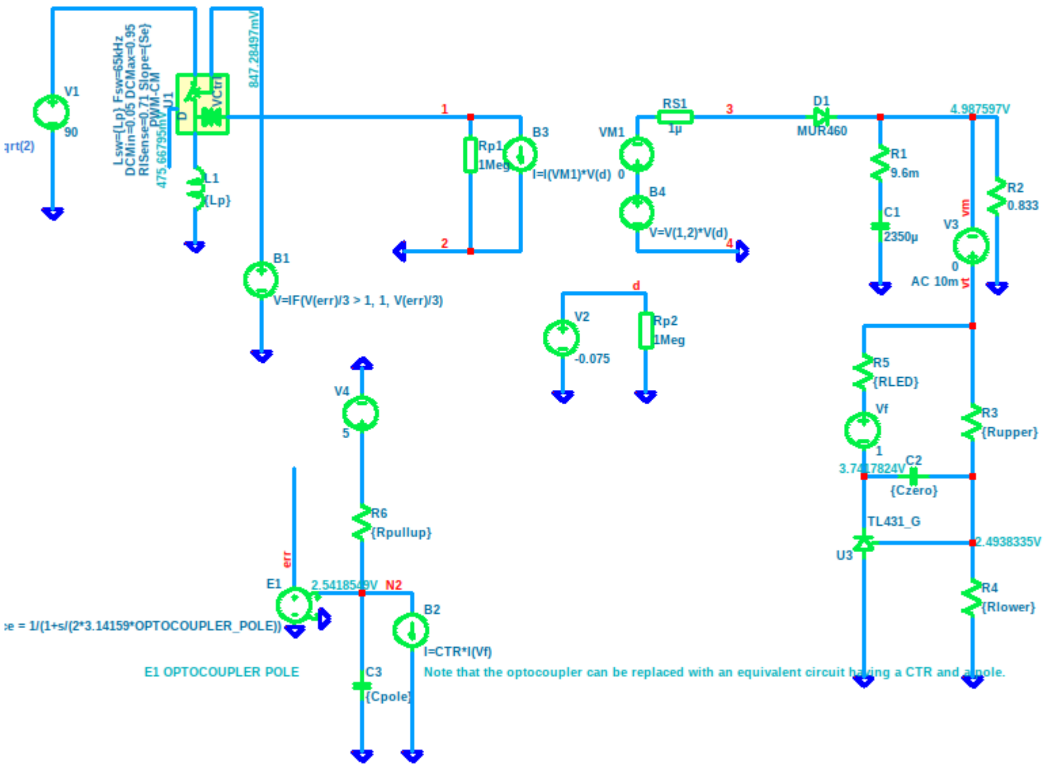
$$we\,operate\,\text{in}\,CCM\,with\,D\approx 50\,\% \rightarrow Q=\frac{1}{\pi\left(D`\frac{S_e}{S_n}+\frac{1}{2}-D\right)}=\frac{1}{3.14\left((1-.412)\frac{0}{S_n}+\frac{1}{2}-.412\right)}=3.61$$

This result suggests that we need to damp the subharmonic poles to bring the quality factor below 1. Extracting the Se parameter (the external ramp amplitude) leads to:

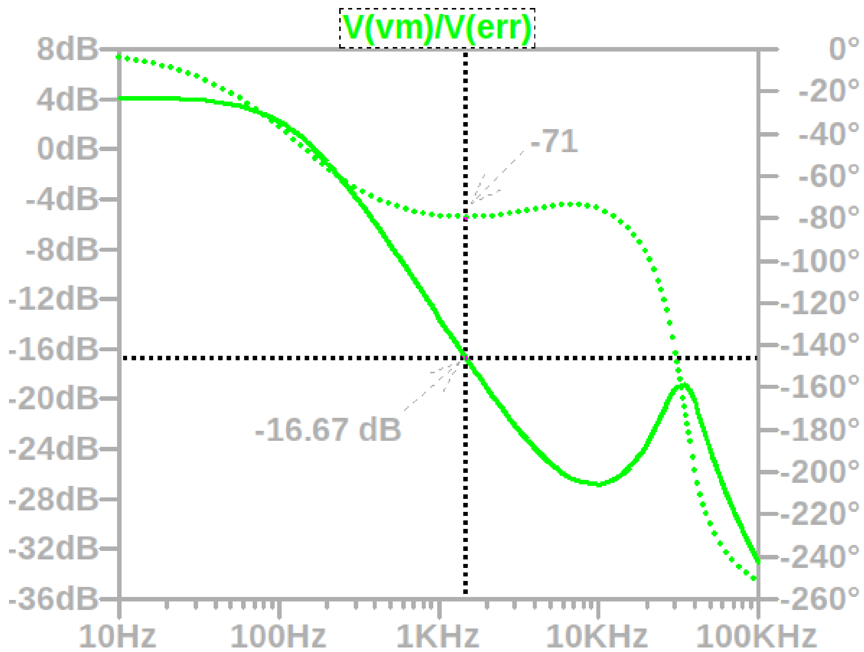
$$S_e=\frac{S_n}{D`}\left(\frac{1}{\pi}-0.5+D\right)=\frac{V_{\text{in}} R_{sense}}{L_p D`}\left(\frac{1}{\pi}-0.5+D\right)=\frac{90\cdot 0.71}{978u\cdot(1-0.412)}\left(\frac{1}{3.14}-0.5+0.412\right)=25.6\,kV/s$$

2nd Method to derive Se

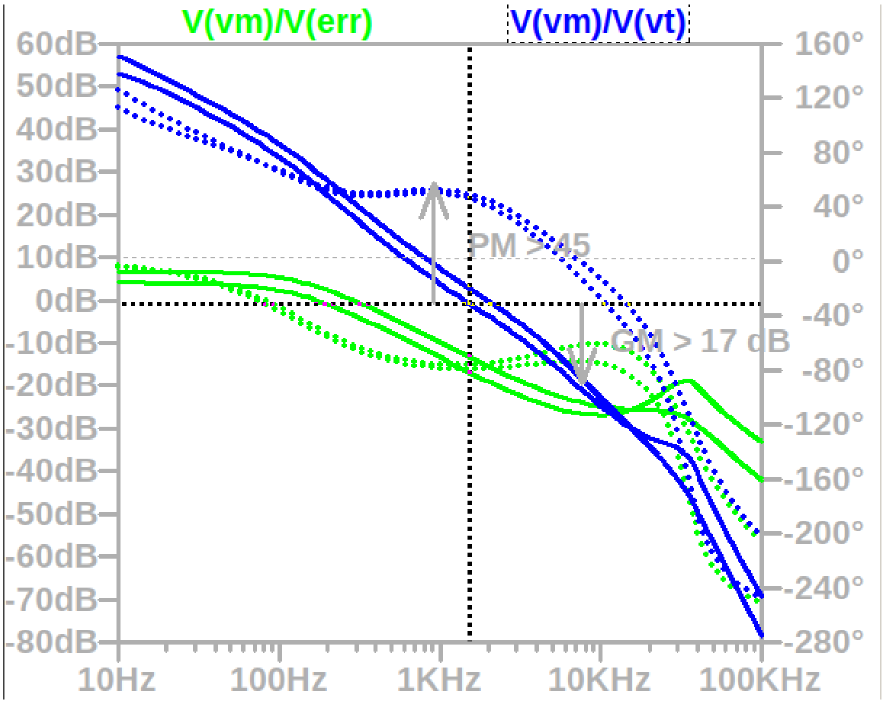
$$S_e=\frac{S_{off}\cdot R_{sense}}{2}=\frac{\frac{V_{out}}{NL_p}\cdot R_{sense}}{2}=\frac{\frac{5}{0.075\cdot 978u}\cdot 0.71}{2}=\frac{48.39\,kV/s}{2}=24.2\,kV/s$$



→ open-loop sweep of the CM CCM flyback

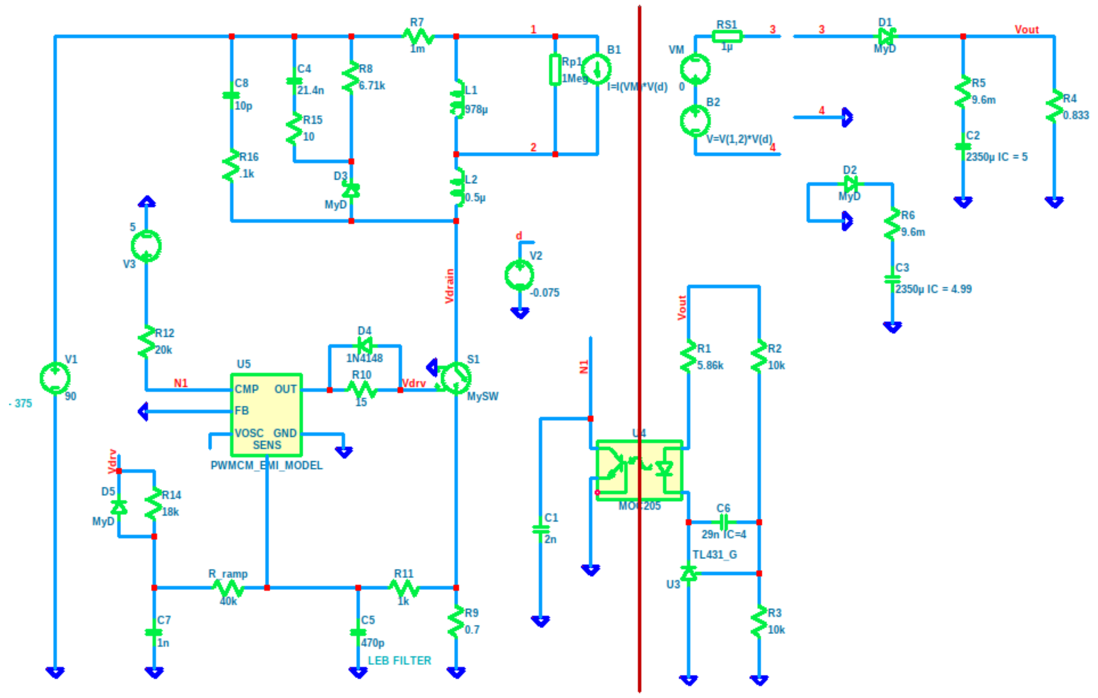


→ (compensated) loop-gain sweep of the CM CCM flyback (tested at both input levels 90 Vdc and 330 Vdc)



Rupper	10 kΩ
Rlower	10 kΩ
Rled	5.86 kΩ
Cpole	2 nF
Czero	29 nF

CYCLE BY CYCLE SIMULATION



the ramp signal is derived from a low-impedance source (the driver pin)

$$I_{C7} \approx \frac{V_{drvhigh}}{R14} = \frac{15}{18k} \approx 800\text{e-}6\,A$$

for a 0.412 duty ratio and a 15.4-μs switching period, the on-time duration is 6.34 us

$$i.e.,\, t_{onmax} = D_{max} \cdot T_{SW} = 0.412 \cdot 15.4\,us = 6.34\,us$$

the voltage across C7 ramps up to

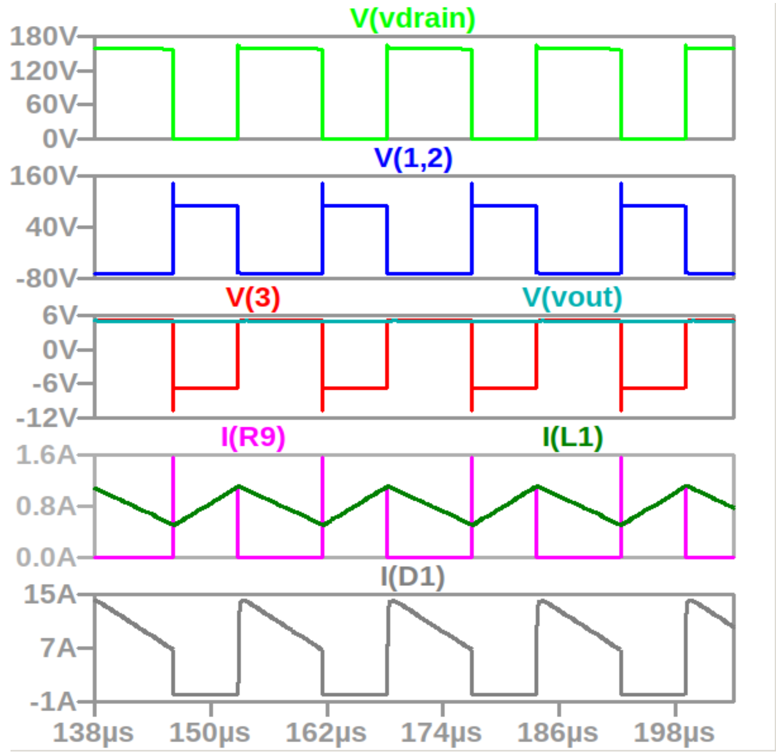
$$V_{C7} = \frac{I_{C7}\, t_{onmax}}{C_7} = \frac{800u \cdot 6.34u}{1\text{e-}9} = 5.072$$

its voltage slope is then

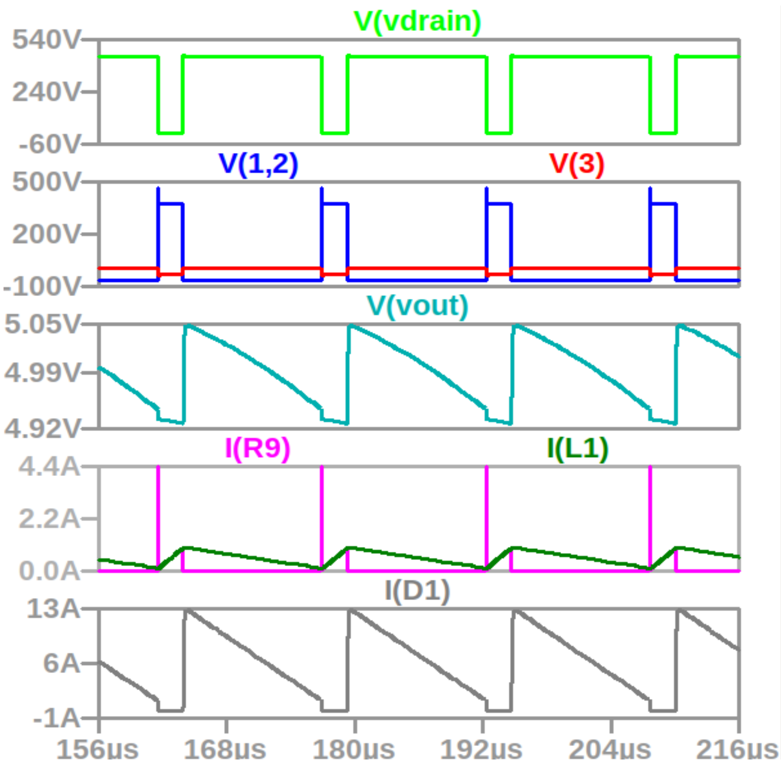
$$S_{ramp} = \frac{V_{peak}}{t_{onmax}} = \frac{5.072}{6.34u} = 800\,kV/s$$

$$then\; R_{ramp} = \frac{S_{ramp}}{S_e} \cdot R11 = \frac{800k}{20k} 1\text{e}3 = 40k$$

for VIN 90 VDC

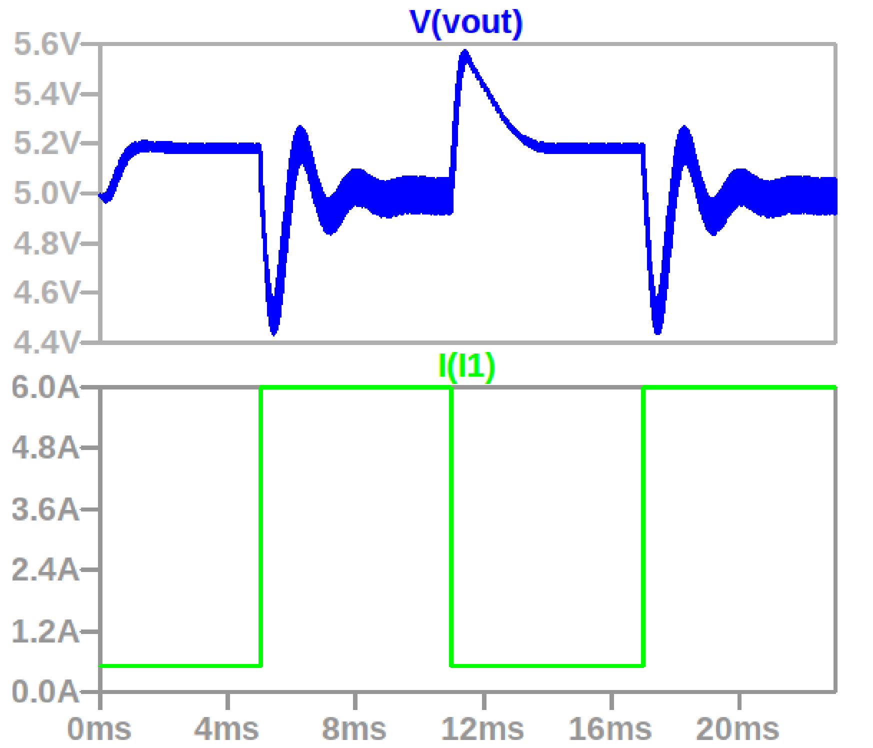


for VIN 375 VDC



(an LC output filter can be added with f_0 greater than f_c)

LOAD STEP 0.5 A – 6 A with tr, and tf of 1us at VIN 90 VDC



LOAD STEP 0.5 A – 6 A with tr, and tf of 1us at VIN 375 VDC