flyback 85 – 275 VRMS 12V at 2A 24W design notes (120 (i.e. 85*sqrt(2)) – 388 Vpp)

the rectifier bridge

Vmin is usually selected around 25 to 30% of the minimum peak line voltage for instance, if the converter operates down to 85 VRMS, then Vmin can be chosen around

$$(85\sqrt{2})\cdot 0.7 = 84\,Vdc$$

(the power supply, a flyback, delivers 24W (Pconv) to a given load with an estimated efficiency of 85%)

85 – 275 VRMS 47 – 63 Hz Vmin = 80 V dc

T = 45 C MAX

tc the diode conduction time, longest at lowest line input

$$t_c = \frac{1}{4F_{line}} - \Delta t = \frac{1}{4F_{line}} - \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{1}{4\cdot 60} - \frac{\sin^{-1}\frac{80}{85\sqrt{2}}}{2\cdot 3.14\cdot 60} = 4.16\text{e-}3 - \frac{728\text{e-}3}{377} = 2.2\text{e-}3\,s$$

the discharge time is evaluated by

$$t_d = \frac{1}{2F_{line}} - t_c = \frac{1}{2\cdot 60} - 2.2\text{e-}3 = 6.13\text{e-}3\,s$$

$$C_{bulk} \geq \frac{2P_{out}}{\eta\left(V_{peak}^2 - V_{min}^2\right)} t_d = \frac{2\cdot 24}{0.85\left(120^2 - 80^2\right)} 6.13\text{e-}3 = 43.27\,uF$$

the final capacitor selection is always based on the rms current flowing through it

$$I_{Cbulk,rms} = \frac{P_{out}}{\eta V_{bulk,avg}}\sqrt{\frac{2}{3F_{line}t_c} - 1} = \frac{24}{0.85\frac{120+80}{2}}\sqrt{\frac{2}{3\cdot 60\cdot 2.2\text{e-}3} - 1} = 0.568\,Arms$$

the capacitor needs to permanently sustain a steady – state voltage of 275 * sqrt(2) = 388 Vdc → hence, a 400V type is mandatory

Kemet 47uF/450V ESU476M450AM3
Iripple at 100 kHz and 105 C 880 mArms with ripple coefficient at 50 Hz of 0.5 → 0.5 * 880 mArms = 440 mArms
tan δ = 0.2 then

$$ESR = \frac{\tan\delta}{2\pi f C} = \frac{0.2}{2\cdot 3.14\cdot 120\cdot 47\text{e-}6} = 5.64\,\Omega$$

D x L (mm) 16 x 36

SELECT 1 * 47 uF

-> now that we have selected 1 * 47 uF, the various times also need to be updated and from Cbulk eq. we have

$$V_{min} = \sqrt{\frac{\eta C_{bulk} V_{peak}^2 - 2P_{conv}t_d}{C_{bulk}\eta}} = \sqrt{\frac{0.85\cdot 47\text{e-}6\cdot 120^2 - 2\cdot 24\cdot 6.13\text{e-}3}{47\text{e-}6\cdot 0.85}} \approx 84\,V$$

$$t_c = \frac{1}{4F_{line}} - \Delta t = \frac{1}{4F_{line}} - \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{1}{4\cdot 60} - \frac{\sin^{-1}\frac{84}{85\sqrt{2}}}{2\cdot 3.14\cdot 60} = 4.16\text{e-}3 - \frac{773\text{e-}3}{377} = 2.1\text{e-}3\,s$$

$$t_d = \frac{1}{2F_{line}} - t_c = \frac{1}{2\cdot 60} - 2.1\text{e-}3 = 6.23\text{e-}3\,s$$

the capacitor peak current can be evaluated by

$$I_{Cbulk,peak} = 2\pi F_{line} C_{bulk} V_{peak} \cos(2\pi F_{line}\Delta t)$$

$$where\ \Delta t = \frac{\sin^{-1}\frac{V_{min}}{V_{peak}}}{2\pi F_{line}} = \frac{\sin^{-1}\frac{84}{85\sqrt{2}}}{2\cdot 3.14\cdot 60} = 2.05\text{e-}3\,s$$

$$\text{and } I_{Cbulk,peak} = 6.28\cdot 60\cdot 47\text{e-}6\cdot(85\sqrt{2})\cos(6.28\cdot 60\cdot 2.05\text{e-}3) = 1.52\,A$$

$$I_{Cbulk,rms} = \frac{P_{out}}{\eta V_{bulk,avg}}\sqrt{\frac{2}{3F_{line}t_c} - 1} = \frac{24}{0.85\frac{120+84}{2}}\sqrt{\frac{2}{3\cdot 60\cdot 2.1\text{e-}3} - 1} = 0.573\,Arms$$

the diode peak current is defined by

$$I_{d,peak} = I_{out} + I_{Cbulk,peak} = \frac{P_{out}}{\eta}\frac{2}{V_{min}+V_{peak}} + I_{Cbulk,peak} = \frac{24}{0.85}\frac{2}{84+85\sqrt{2}} + 1.52 = 0.276 + 1.52 = 1.79\,A$$

$$I_{d,rms} = \frac{P_{conv}}{\eta V_{bulk,avg}\sqrt{3F_{line}t_c}} = \frac{24}{0.85\frac{120+84}{2}\sqrt{3\cdot 60\cdot 2.1\text{e-}3}} = 0.450\,Arms$$

$$I_{d,avg} = \frac{P_{conv}}{2\eta V_{bulk,avg}} = \frac{24}{2\cdot 0.85\frac{120+84}{2}} = 0.138\,A\ then\ P_{d,avg} \approx V_f \cdot I_{d,avg} = 0.7\,V\cdot 0.138\,A = 96.6\,mW$$

-> diodes such as the ON Semiconductor 1N5406 (600V/3A) are well suited for this application

the rms input current also needs to be known to select the right fuse

$$I_{in,rms} = \frac{\sqrt{2}P_{conv}}{\eta V_{bulk,avg}\sqrt{3F_{line}t_c}} = \frac{\sqrt{2}\cdot 24}{0.85\frac{120+84}{2}\sqrt{3\cdot 60\cdot 2.1\text{e-}3}} = 0.636\,Arms$$

a 250 Vrms/3.15 A delayed type (a time-delay type is necessary because of the large in-rush current at power-on)

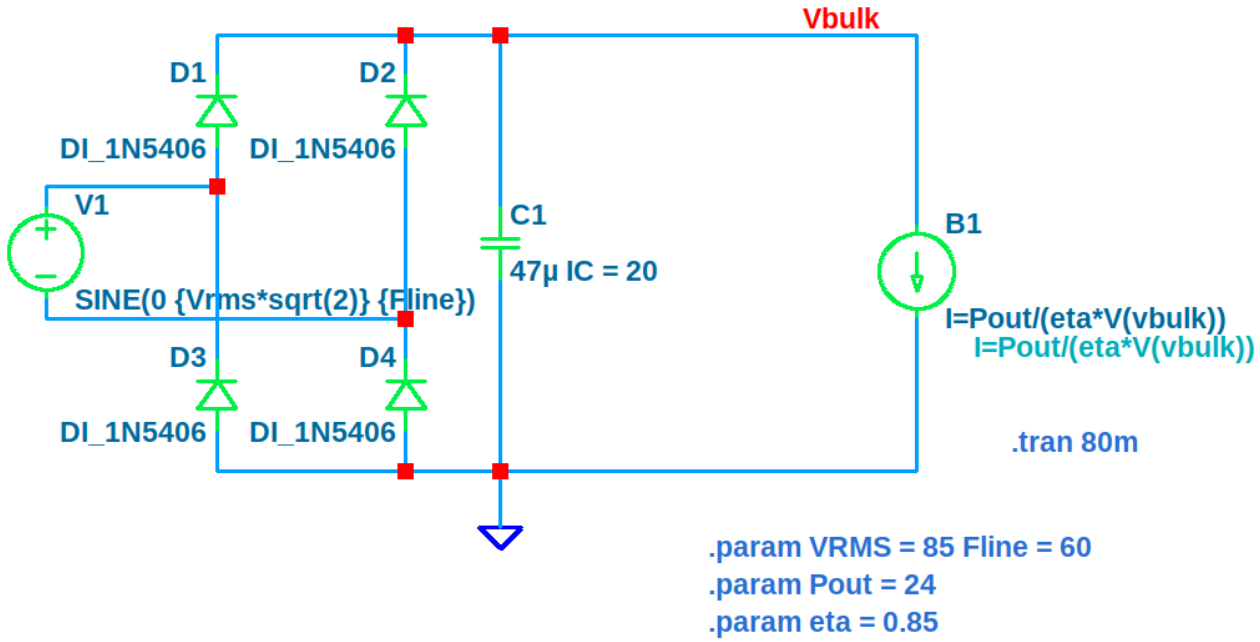
SR-5-6.3A-AP Bussman/Eaton → “optional”

$$PF = \frac{V_{bulk,avg}}{V_{in,rms}}\sqrt{\frac{3}{2}F_{line}t_c} = \frac{102}{85}\sqrt{\frac{3}{2}\cdot 60\cdot 2.1\text{e-}3} = 0.521$$

-> the power factor gives information about the input energy spread over the mains period. With narrow input spikes, the instantaneous energy remains confined in the vicinity of the peak, inducing a high rms and peak current

$$then\ I_{\text{in},rms} = \frac{P_{out}}{\eta V_{\text{in}min,rms} PF} = \frac{24}{0.85 \cdot 85 \cdot 0.521} = 0.637\ Arms$$

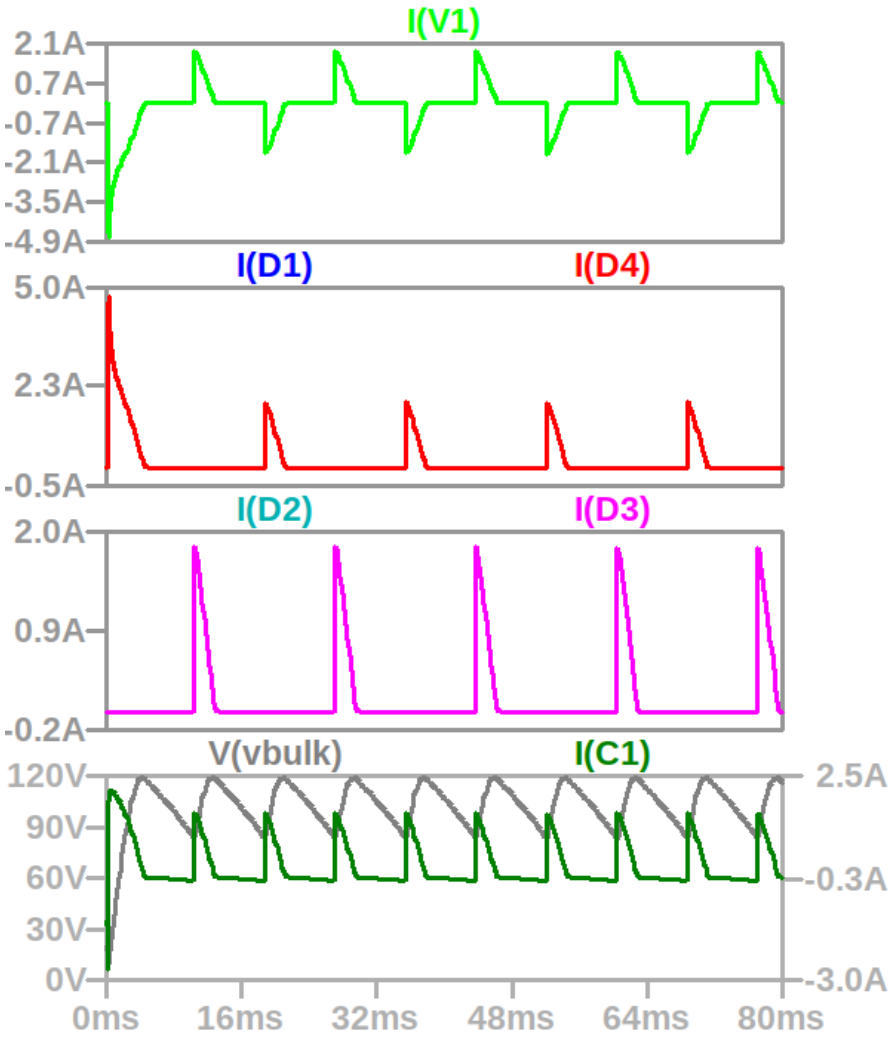
SPICE SIMULATION



Note the initial condition on the capacitor which avoids a SPICE division by zero when the capacitor is totally discharged at power on.

(to measure the power factor, measure the rms input current and multiply it by the input rms voltage. This gives us the VA. The average input power is found by multiplying vmains(t) by iin(t), you have pin(t) and average over one period, and you obtain watts)

$$PF = \frac{v_{mains}(t) \cdot i_{mains}(t)}{V_{\text{in},rms} \cdot I_{\text{in},rms}} = \frac{28.56\,W}{85 \cdot 0.608} = \frac{28.56\,W}{51.68\,VA} = 0.552$$ (this is a poor value, typical of full-wave application)



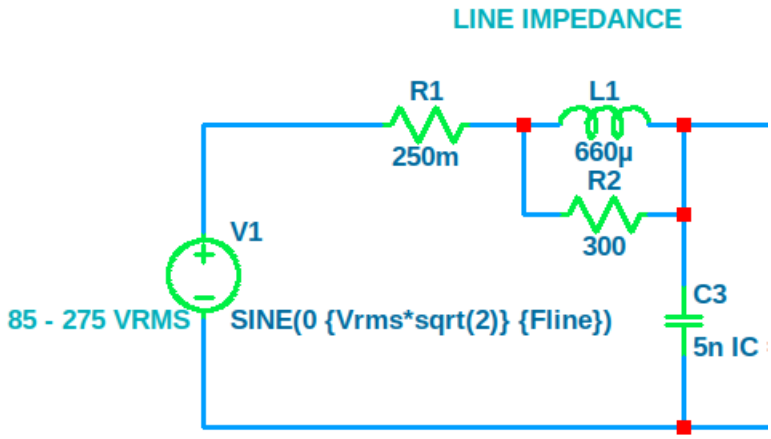
SIMULATION CONDITIONS (85 VRMS 60 Hz FLINE)

	EQUATIONS	SPICE
Vmin	84 V	83.9 V
Vbulk_avg	102 V	103.29 V
tc	2.1e-3s	2.147e-3s
td	6.23e-3s	6.143e-3s
Icbulk_peak	1.52 A	1.48 A
Icbulk_rms	0.573 Arms	0.504 Arms
Idpeak	1.79 A	1.80 A
Idrms	0.45 Arms	0.437 Arms
Idavg	0.138 A	0.153 A
I_inrms	0.636 Arms	0.594 Arms

SIMULATION CONDITIONS (240 VRMS 50 Hz FLINE)

EQUATIONS SPICE	
Vmin	322 V
Vbulk_avg	330 V
tc	1.1e-3s
td	8.6e-3s
Icbulk_peak	1.46 A
Icbulk_rms	0.282 Arms
Idpeak	1.54 A
Idrms	0.222 Arms
Idavg	0.047 A
I_inrms	0.294 Arms

(it is important to note that all the above equations are assuming a perfectly sinusoidal input voltage source (for simplicity), featuring a low output impedance. In reality, the mains is often distorted and because of the EMI filter presence, the output impedance varies quite a bit. Final results captured on the bench might differ from the above calculations.)



(single output) flyback analysis

Vinmin	85 Vrms
Vbulkmin	90 Vdc (considering 25% ripple on the bulk capacitor)
	$i.e., 0.75(85\sqrt{2})$
Vinmax	265 Vrms
Vbulkmax	375 Vdc
	$i.e., 265\sqrt{2}$
Vout	12 V
Vripple ΔV	250 mV
Vout drop	0.25 V maximum from Iout = 0.2 to 2 A in 10 us
Ioutmax	2 A
MOSFET derating factor k_D	0.85
Diode derating factor k_d	0.5

RCD clamp diode overshoot Vos	15 V
fsw	65 kHz

DCM CM

600 V MOSFET

$$N=\frac{k_c(V_{out}+V_f)}{BV_{DSS}k_D-V_{os}-V_{bulk,max}}=\frac{1.5(12+0.7)}{600\cdot0.85-15-357}=0.138\,(k_c\,of\,1.5\,if\,L_{leak}\leqslant1\%)$$

SELECT N 0.14

$$(\text{from the buck}-\text{boost converter})\,I_{peak}=\frac{2\left(V_{min}+\frac{V_{out}+V_f}{N}\right)(V_{out}+V_f)N}{\eta V_{bulk,min}R_{load}}$$

$$V_{min}=V_{bulk,min}=0.75\cdot85\sqrt{2}=90\,V\,dc$$

$$V_{bulk,avg}\approx\frac{V_{peak}+V_{min}}{2}=\frac{85\sqrt{2}+90}{2}=105\,V$$

$$then\,I_{peak}=\frac{2\left(90+\frac{12+0.7}{0.14}\right)(12+0.7)0.14}{0.85\cdot90\cdot6}=1.4\,A$$

$$L_P=\frac{2P_{out}}{I_{peak}^2F_{sw}\eta}=\frac{2\cdot24}{1.4^2\cdot65e3\cdot0.85}=443\,uH$$

$$t_{on,max}=\frac{I_{peak}L_p}{V_{bulk,min}}=\frac{1.4\cdot443\text{e-}6}{90}=6.89\,us\,then\,D_{max}=\frac{t_{on,max}}{T_{sw}}=\frac{6.89\text{e-}6}{15.38\text{e-}6}=0.448$$

$$t_{on,min}=\frac{I_{peak}L_p}{V_{bulk,max}}=\frac{1.4\cdot443\text{e-}6}{375}=1.65\,us\,then\,D_{min}=\frac{t_{on,min}}{T_{sw}}=\frac{1.65\text{e-}6}{15.38\text{e-}6}=0.107$$

$$I_{D,rms}=I_{peak}\sqrt{\frac{D_{max}}{3}}=1.4\sqrt{\frac{0.448}{3}}=0.54\,Arms$$

$$P_{max}=\frac{T_{j,max}-T_A}{R_{\Theta J-A}}=\frac{110-50}{62}=\frac{60}{62}=0.96\,W\,(\text{maximum power accepted by the package in free-air})$$

$$P_{cond}=I_{D,rms}^2R_{DS,on}\,at\,T_j=110\,C$$

$$R_{DS,on}\,at\,T_j=110\,C\leqslant\frac{P_{max}}{I_{D,rms}^2}\leqslant\frac{0.96}{0.54^2}\leqslant3.29\,\Omega$$

$$SELECT\,R_{DS,on}\,at\,T_j=25\,C\approx1.64\,\Omega$$

$$P_{sw,lump-max}=\frac{1}{2}C_{lump}\left(V_{bulk,max}+\frac{V_{out}+V_f}{N}\right)F_{sw}$$

$$P_{sw,lump-min}=\frac{1}{2}C_{lump}\left(V_{bulk,max}-\frac{V_{out}+V_f}{N}\right)F_{sw}$$

$$P_{sw,off}=\frac{I_{peak}\left(V_{bulk}+V_{clamp}\right)\Delta t}{2}F_{sw}$$

where Δt is the overlap of the current through "and" the voltage across the MOSFET (which can be measured on the prototype)

$$P_{MOSFET}=P_{cond}+P_{sw,lump}+P_{sw,off}$$

$$P_{drv}=F_{sw}Q_gV_{cc}\left(dissipation\,on\,IC\right)$$

$R_{sense}=\frac{1\,V}{I_{peak}}$, assuming our controller considers a current limit when the voltage image on its dedicated pin hits 1 V.

We need a peak current of 1.4 A. Considering a design margin of 10% (Ipeak = 1.54 A), the sense resistor value equals

$$R_{sense}=\frac{1\,V}{1.4\cdot1.1}=0.65\,\Omega$$

$$P_{Rsense}=I_{D,rms}^2R_{sense}=0.54^2\cdot0.65=0.19\,W$$

$$R_{clp}=\frac{\left(k_c-1\right)\left[2\,k_c\left(V_{out}+V_f\right)^2\right]}{N^2F_{sw}L_{leak}I_{peak}^2}=\frac{\left(1.5-1\right)\left[2\cdot1.5\left(12+0.7\right)^2\right]}{0.14^2\cdot65e3\cdot\left(450\,u\cdot0.01\right)1.54^2}=17.8\,e\,3\,\Omega$$

$$C_{clp}=\frac{k_c\left(V_{out}+V_f\right)}{N\,R_{clp}F_{sw}\Delta V}=\frac{1.5\cdot12.7}{0.14\cdot17.8e3\cdot65e3\cdot11}=10.7\,nF$$

where Lleak is the leakage inductance, selected to be 1% of the primary inductance and ΔV is the selected ripple in percentage of the clamp voltage; 11 V roughly corresponds to 10% of the clamp voltage (~ 114 V)

(the power dissipated in the clamp resistor will guide us through the resistor selection)

$$P_{Rclp}=\frac{1}{2}F_{sw}L_{leak}I_{peak}^2\frac{k_c}{k_c-1}=0.5\cdot65e3\cdot4.43e\text{-}6\cdot1.54^2\frac{1.5}{0.5}=1.02\,W$$

$$\left(secondary-diode\,voltage\,stress\right)PIV=NV_{bulk,max}+V_{out}$$

$$PIV=0.14\cdot375+12=64.5\,V$$

with kd of 0.5 → select a diode featuring a VRRM of 150 V

$$P_d=V_{T0}I_{d,avg}+R_dI_{d,rms}^2+D\,I_R\,PIV$$

$$P_d\approx V_fI_{d,avg}=0.7\,V\cdot2\,A=1.4\,W$$ (MBR20200)

$$I_{sec,peak} = \frac{I_{peak}}{N} = \frac{1.4}{0.14} = 10\,A$$

$$R_{ESR} \leqslant \frac{V_{ripple}}{I_{sec,peak}} \leqslant \frac{0.25}{10} \leqslant 25\,m\Omega$$

680 uF – 16 V – YXG series
R_{ESR} = 60 mΩ at T_A = 20 C and 100 kHz
$I_{C,rms}$ = 1.2 A at 100 kHz

$$I^2_{Cout,rms} = I^2_{sec,rms} - I^2_{out,avg}$$

$$I_{sec,rms} = I_{sec,peak}\sqrt{\frac{1-D_{max}}{3}} = 10\sqrt{\frac{1-0.448}{3}} = 4.28\,A$$

$$I_{Cout,rms} = \sqrt{4.28^2 - 2^2} = 3.78\,Arms$$

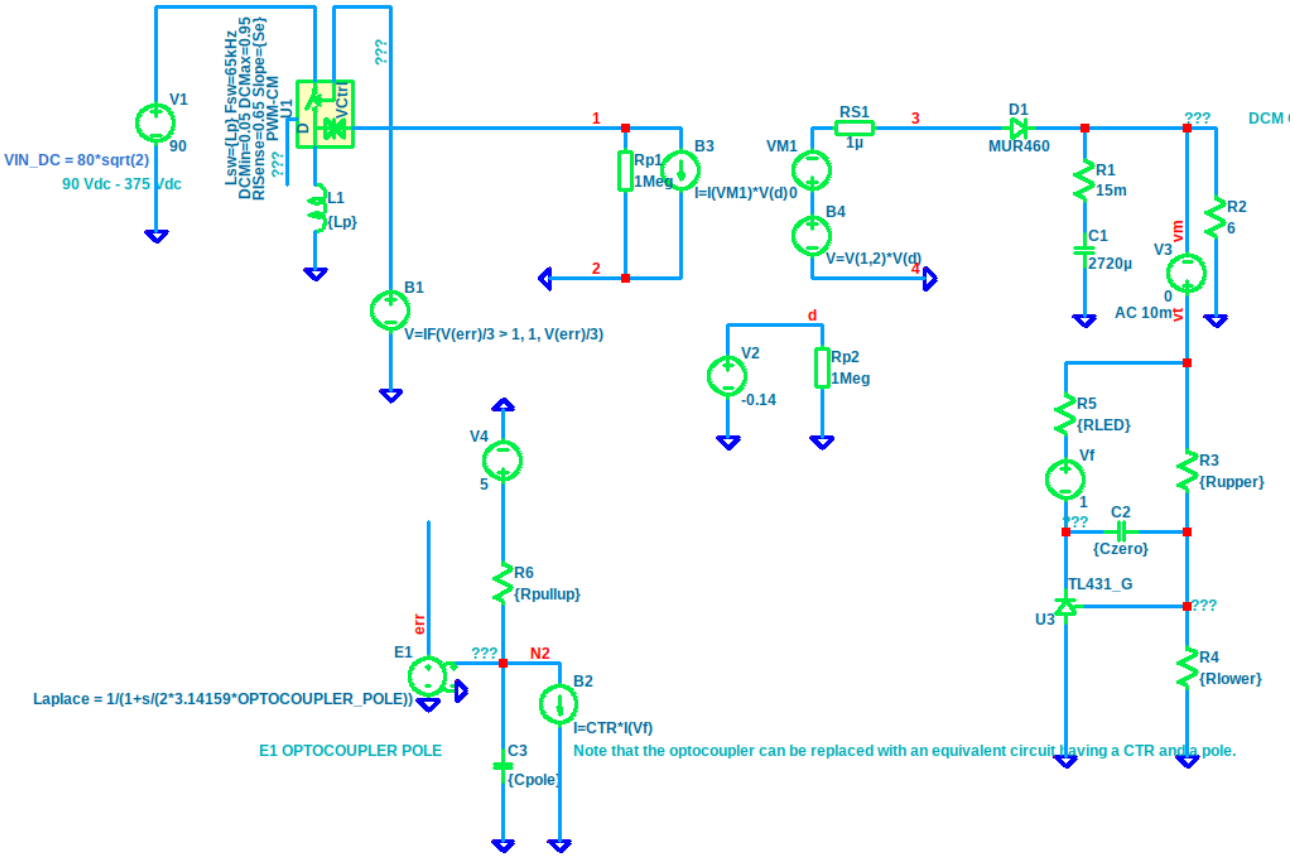
→ this means we have to put in parallel four 680 uF capacitors to accept the above rms current, assuming they share the current equally.

$$R_{ESR,total} = \frac{60\,m}{4} = 15\,m\Omega$$

$$P_{Cout} = I^2_{Cout,rms} R_{ESR} = 3.78^2 \cdot 15\text{e-}3 = 0.214\,W$$

AC ANALYSIS

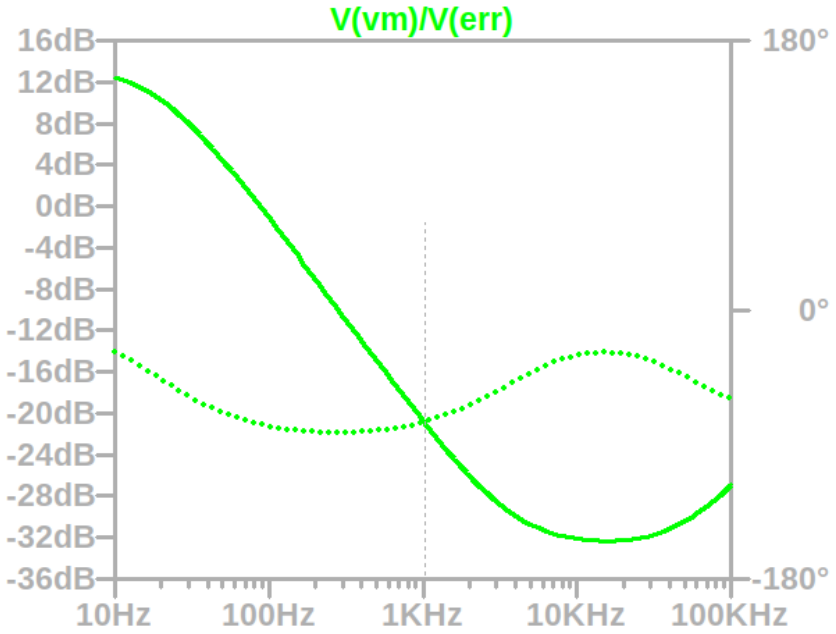
Lp	443 uH
Rsense	0.65 Ω
N	0.14
Cout	680 uF x 4
Resr	15 mΩ
Rload	6 Ω



$$f_c \approx \frac{\Delta I_{out}}{2\pi \Delta V_{out} C_{out}} = \frac{1.8}{6.28 \cdot 0.25 \cdot 2720\text{e-}6} = 421\,Hz$$

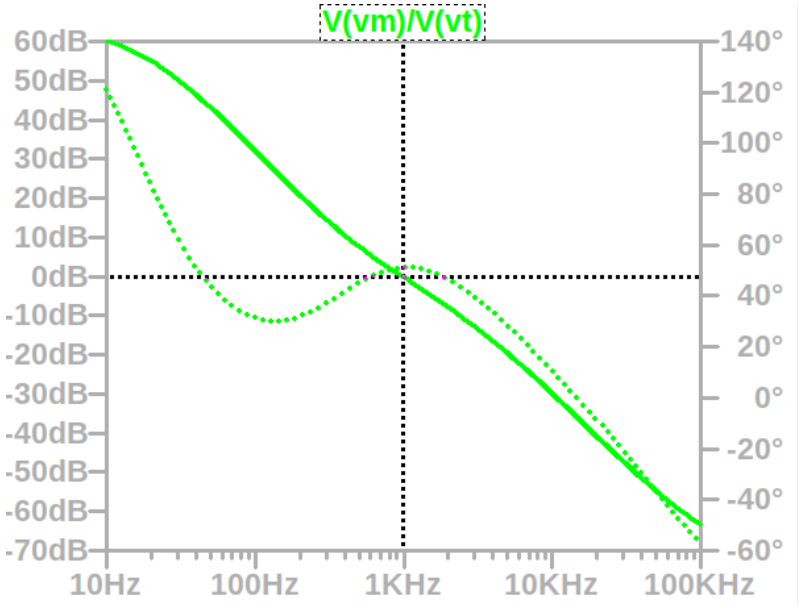
SELECT f_c of 1 kHz

→ open-loop sweep of the CM DCM flyback (at 90 V VIN)



From the Bode plot we can see that the required gain at 1 kHz is 20 dB worst case. The phase lag this point is 75 °.

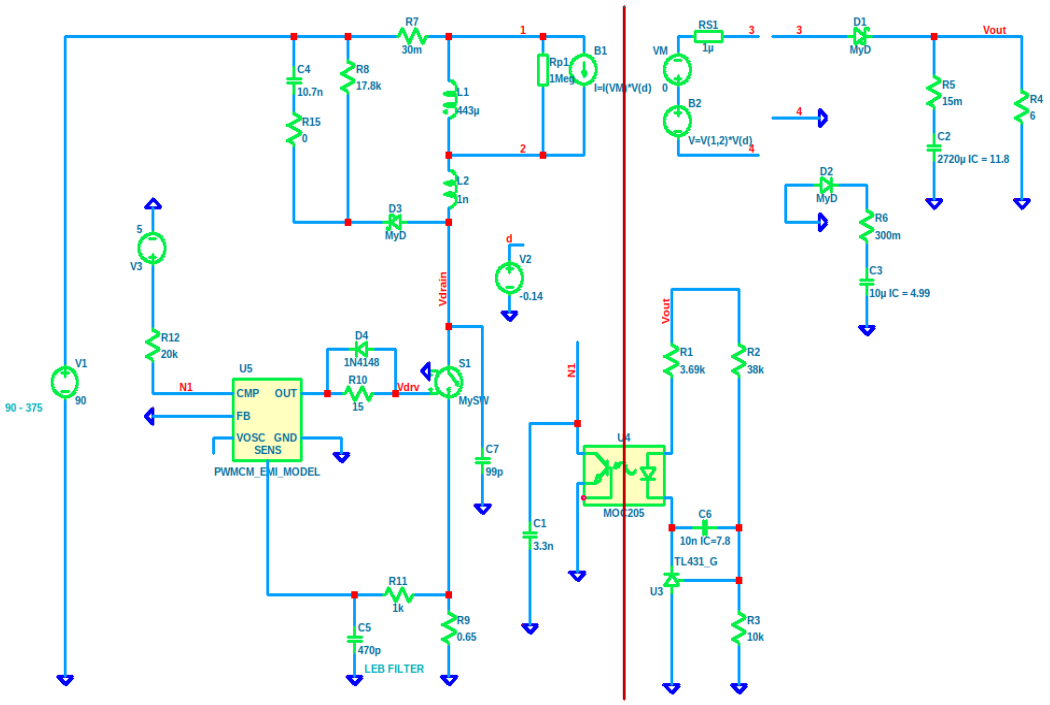
→ compensated loop-gain sweep of the CM DCM flyback (at 90 V VIN)



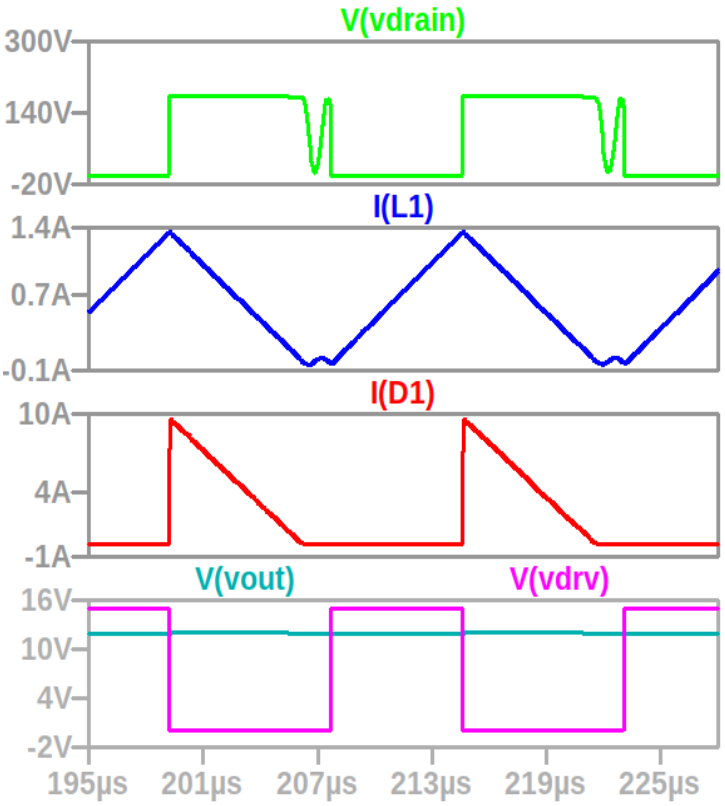
Its component recommendations for the 1-kHz bandwitdth and a targeted 60 ° phase margin are:

Rled	3690 Ω
Cpole	3.3 nF
Czero	10 nF

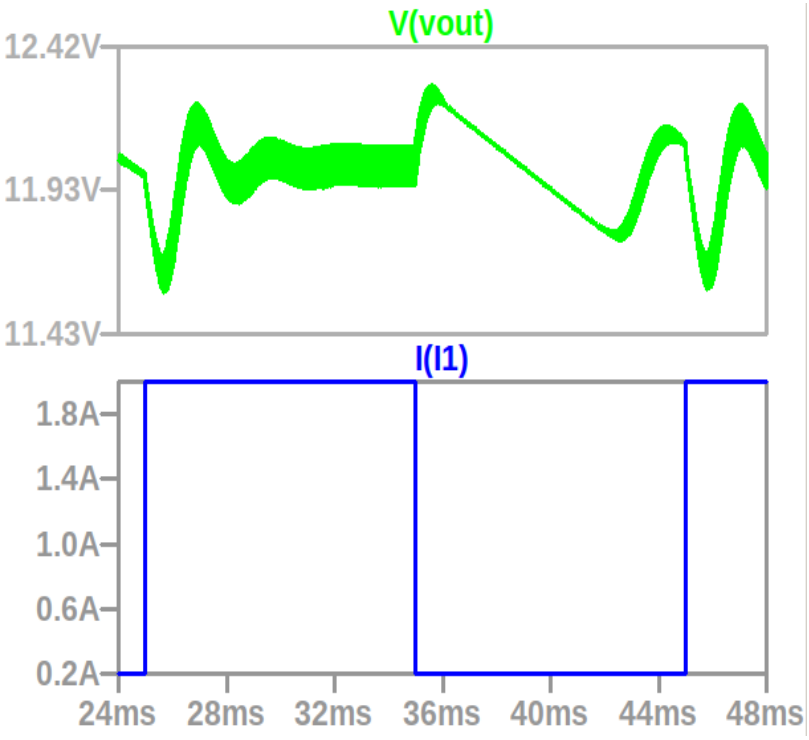
CYCLE BY CYCLE SIMULATION



SIMULATION CONDITIONS (VIN 90 Vdc)



LOAD STEP 0.2 A – 2 A with tr, tf of 1us



OUTPUT RIPPLE (2 A LOAD) (without LC output filter)