



UiO : **Department of Physics**
University of Oslo

FYS4260 2019

Microsystems, electronic packaging and
interconnection technologies

Lecture 5 – PCB Layout Theory, DFM, DFT



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Agenda

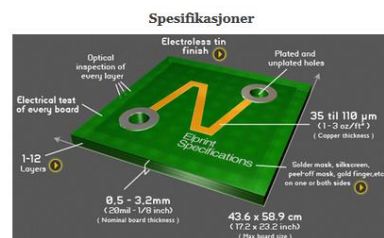
- Manufacturer design rules
- Some very basic PCB Layout theory
 - Just to give you some background for the rules and limitations in this course.
 - Design constraints.
- DFM – Design for Manufacturing
 - What we as designers can do to reduce the failure risk of our boards.
- DFT – Design for Testability
 - How to design a board that is easy to test and debug.

PCB Layout theory

- The schematics are in many ways an «ideal» representation of a circuit.
- Moving over to the «real» world of pcb's, there are some things we need to keep in mind.
- First, its the capabilities of the manufacturer.
- Second, its the electrical behaviour of our circuit, where the tracks are no longer ideal conductors.
- The following sections are only intended to give you a basic qualitative introduction to some of the physics behind a pcb design, it is by no means a complete guide.

Manufacturer Design rules

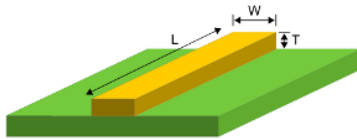
- The processes and capabilities of the manufacturing process gives a set of rules that define the minimum spacing between PCB objects.
- Example from Elprint.no
- In CadSTAR this is defined in the assignments tab as minimum spacings between two objects.



Design regler

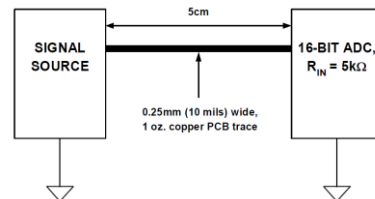
PARAMETER	CHEAPEST		MINIMUM*	
	mm	mil	mm	mil
Trace width	0.125	5	0.10	4
Clearance	0.125	5	0.10	4
Annular ring	0.2	8	0.10	4
Solder mask ring	0.1	4	0.075	3
Via pad diameter	0.7	30	0.25	10
Hole diameter	0.3	12	0.10	4

PCB Trace Resistance



$$R = \rho * \frac{\text{Length}}{\text{Area}} = \rho * \frac{L}{W * t}$$

For a trace in 35μ this gives
 $0,48\text{m}\Omega/\text{square}$

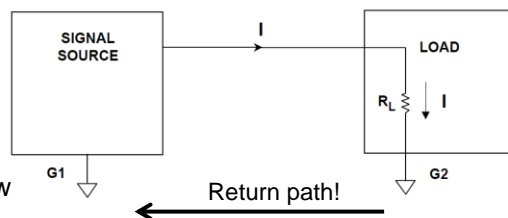


- A 10mil trace gives $\sim 19\text{mohm/cm}$
- 5cm trace $\sim 0.1\Omega$
- This forms a voltage divider with the input resistance of the ADC, creating an error of $0.1/5\text{k} = 0,0019\%$

The LSB of an 16bits ADC is $\dots 0,0015\%$
 (But the input resistance is usually much higher than 5k...)

Grounding and Return Path

- As the grounding is not ideal, there IS a voltage potential between two grounding points.
- From ohm's law we know that this potential can be minimized by
 - Decrease the ohmic resistance in the ground traces -> Use more copper, eg planes!
 - Minimize ground currents.

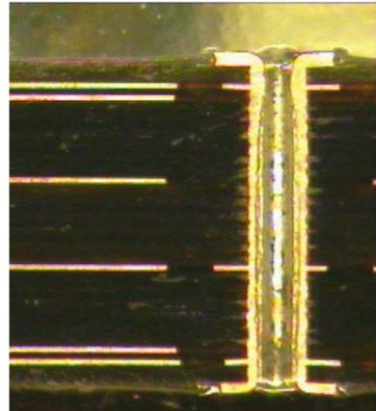


At any point in a circuit the algebraic sum of the currents is zero

Remember your ground currents!
 Identify how and where your ground currents flow.

Parasitic / Plane Capacitance

- Two conducting faces of area A separated by a distance d forms a parallel plate capacitor.
- We have a lot of these on our boards! (every pad...)
- This capacitance may be both parasitic and/or useful.
- Closely spaced GND and PWR planes act as a HF parallel plate capacitor for the whole board.



1 Top
2 Gnd
3 Pwr

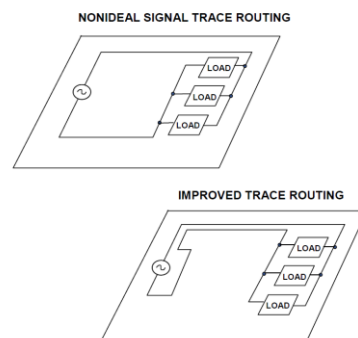
4 Sig

5 Sig

6 Pwr
7 Gnd
8 Bot

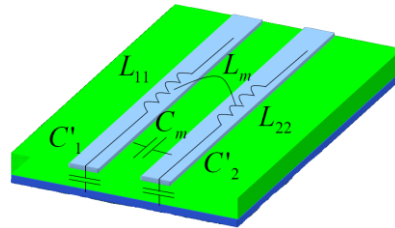
Inductance

- Current flowing in a closed loop forms a single turn inductor.
- This inductance is proportional to the area the loop encloses.
- A large loop can both produce external magnetic fields, and is more susceptible to pick up noise from external fields.
- Ex, avoid routing your reset signal in a large loop, this might pick up noise and reset your circuit...



Crosstalk

- When two traces run parallel to each other we will have a coupling between them
- This coupling is both capacitive and inductive, and called crosstalk.
- No (negligible) resistive coupling
-> no DC coupling
- Proportional to rise/fall times, voltage swings, and physical implementation.
- Less crosstalk from stripline traces than from microstrip.



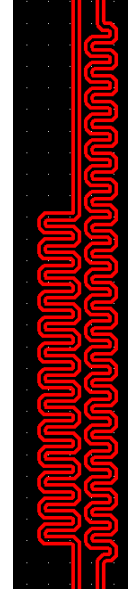
ElectroMagnetic Compatibility - EMC

- As we have seen a current loop acts as an antenna and radiates electromagnetic fields.
- From Maxwells equations we get that this field is proportional to

$$E = K * Area * Current * Frequency^2$$
- This is a great approximation, among others assuming a sinusoidal wave form. But the important here are the relationship between the factors.
- To reduce EMI one have to:
 - reduce frequency (or more correct – rise and fall times)
 - use components with lower drive strengths
 - minimize current loops.
 - Ensure you have a low impedance to ground by using solid ground planes.

Very short on trace length

- In high speed designs, signal propagation delay is comparable to one half the period of the frequency of operation.
- To ensure correct functionality, these traces need to be length-matched to make sure all signals appear at the receiver within the acceptable window.
- Propagation delay for 100mm trace is ~600ps for microstrip and ~700 for stripline.
- Typical examples are memory busses.



Very short on high voltage

- High voltage $> 1\text{kV}$
- To prevent arcing over conductors:
 - Use larger spacing between conductive elements (traces, pads, vias, ...)
 - Use special materials with high dielectric breakdown voltages.
- The IPC-2221 standard is a good place to start.

Design constraints

- This all leads to a set of rules that must be followed to ensure correct circuit performance.
- This can be spacing between tracks to avoid crosstalk, maximum skew between two signals, maximum delay, track width to ensure minimal DC losses, and others.
 - Ref the Net Route Code constraints used in FYS4260, it is a constrain on the power nets to make sure the layout engineer uses correct track width on high current nets.
- Constraints can be set on the whole design, or on single nets, pads, vias, etc.
- Many CAD tools use constrain managers to handle these settings between the circuit designer and layout engineer.
- Together with the manufacturers design limitations, this forms the complete design rule set for a given design and manufacturing process.

DFM – Design for manufacturability

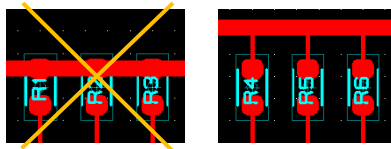
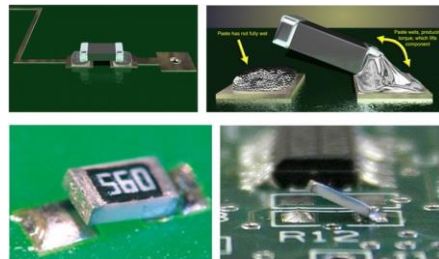
- Design for manufacturability is the process of identifying and reducing problems that may be encountered during the PCB fabrication and assembly processes.
- The first part of DFM is the DRC, but where a design rule is a hard pass or fail, DFM is more nuanced and tries to identify issues that *may have the potential* to create problems.
- While a DRC fail will be present in every copy of the PCB, a DFM issue may only manifest itself in some PCBs.
- See next slides for a few examples.

Tombstoning

Uneven heating of solder paste may cause capillary forces to «lift» one side of small components, creating a «tombstone».

Causes of Tombstoning:

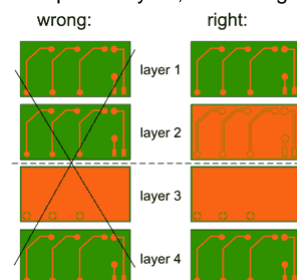
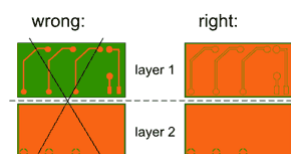
- Copper Pad size and shapes, eg different thermal mass.
- Uneven solder paste printing
- Solder temperature profile
- Pad Surface finish
- Cooling
- Type of Solder paste



To minimize risk of tombstoning try to make the copper mass on each pad as closely matched as possible.

PCB Balancing – Copper symmetry

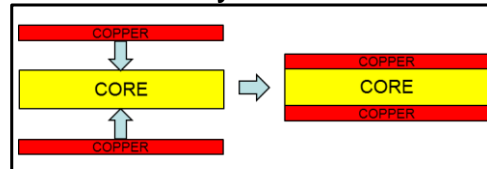
- Due to thermal expansions in the materials, a PCB board might end up bending or cracking up (warping).
- To avoid this, make sure to use a symmetrical stack up. Look at the stack up used in FYS4260...
- Try to make the design as symmetrical as possible with regards to the copper filling on each corresponding layer.
 - Comparable copper filling on GND and power layers, and on signal layers 1 and 4.



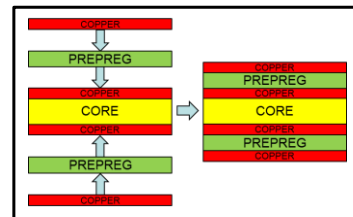
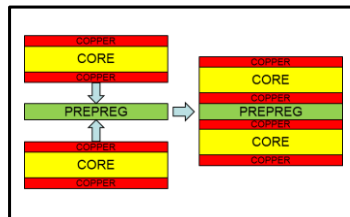
PCB Balancing - Symmetrical Builds

The layers should always be symmerically distributed, both in ragards to copper filling and copper thickness, and to layer spacing and materials!

2 Layer Build

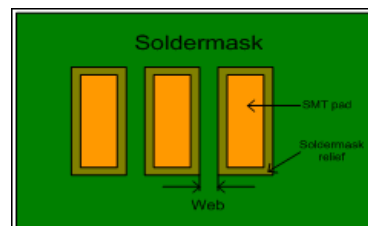


4 Layer Builds



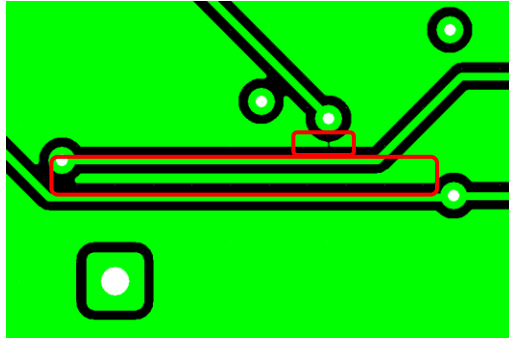
Solder Mask Relief and Web

- To ease the soldering of PCB boards a solder mask layer is applied over the PCB, with openings for the solderable pads.
- Due to misalignment or shrinking, the solder mask openings needs to be oversized by minimum ~4mils compared to the copper pad.
- Today, most manufacturers adjusts the oversizing to their capabilities, we dont add the oversizing ourselves.
- But make sure to have enough spacing between pads to leave room for a solder mask web of minimum 4mils wide.
- Together with the oversizing this means the minimum distance between pads are 8mils ~ 0.2mm.



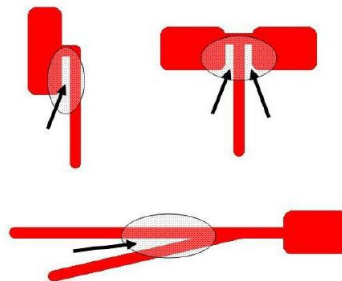
Copper slivers

- Slivers are thin «arms» of copper added during copper pour.
- May come loose during the manufacturing process, risking to short nearby tracks.
- Adjust the sliver width in template properties to reduce the number and occurrences of copper slivers.



Acid Traps

- Small gaps and angles have the risk of «trapping» residue of etching fluids or other contaminations. This may lead to malfunction later on if these residues are trapped inside the board.
- Using PR Editors «Same net» design rule check will highlight these errors, they will not show up on a regular Design rule Check.
- This check will highlight a lot of other things as well, you are NOT supposed to remove all these errors, use it as a means to find areas where you could improve your layout.



Thermal Considerations - Cooling

- The thermal characteristics of a pcb design can be complex, but some considerations on the thermal conductivity of your design is necessary.
- The approach to translating heat away from power components is through copper areas/planes on the PCB.
- Many boards today have large planes inside the PCB, this can be utilized as a thermal layers by connecting power components with multiple thermal vias to these layers.
- With only natural convection and no heatsink, rule of thumb is you need 15cm² of board space filled with copper to dissipate 1W of power for a 40°C rise in temperature.
- If you need more cooling you need to add heatsinks, active cooling by fans or other mechanical solutions.

DFT – Design for Testability

- All boards needs some form of testability
- Ranging from simple testpoints intended for manual measurements, to full sets of testpoints intended for automated «bed of nails» test fixtures.
- As a minimum, all designs must include a GND test point, where you attach your probe GND connection.
 - Use the TP/Testpin component in MECH library.
- Add more testpoints as you need.
 - Do not crowd your design with testpoints, they take up quite a lot of board space.
 - For our purpose through hole pads can be used to test on, but it is not recommended to use SMD pads (it is possible, but can be difficult to detect solder errors – ref tombstoning).

Testpoints

- We have five available testpoints in the library
 - TP/TESTPIN
 - Large through hole testpoint intended for a GND pin.
 - TP/PAD/1.5mm
 - Single sided 1.5mm square
 - TP/PAD/1.5mm/HOLE
 - Double sided 1.5mm square with hole for probe
 - TP/WIRESTUB
 - Smaller through hole suitable for soldering a wire.
 - TP/TOUCHPAD
 - Special testpoint only for the touchpads.
- In addition, pinrows makes excellent testpoints for digital signals (easy connection to probes)
- Testpoints are added in the schematics, then update the pcb.

