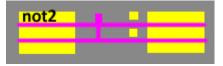
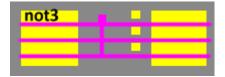
SHARP DMG CPU Cells Library

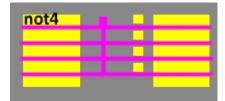
Rev. 1.0

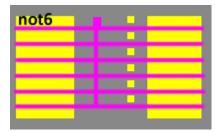
Overview

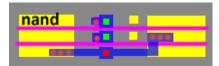


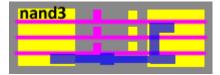


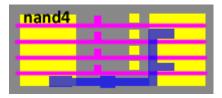


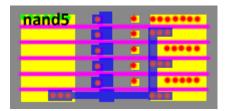


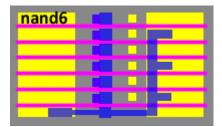


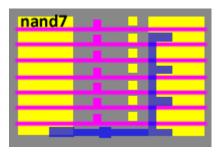




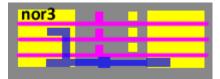


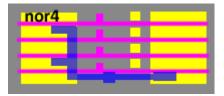


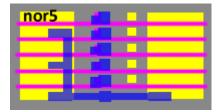


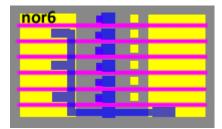


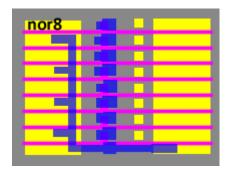




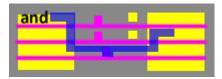




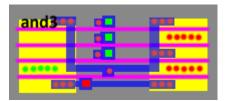




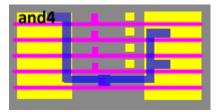
and



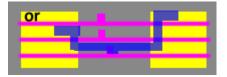
and3



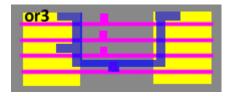
and4



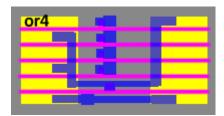
or



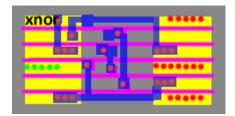
or3



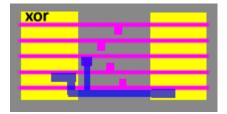
or4



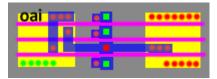
xnor



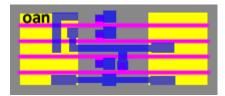
xor

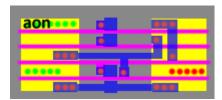


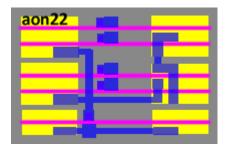
oai

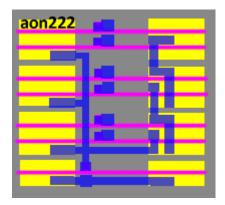


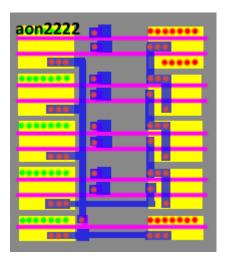
oan

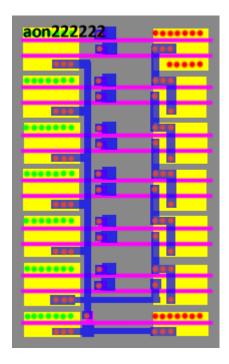




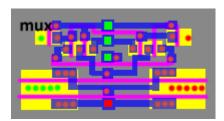




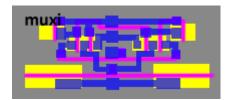




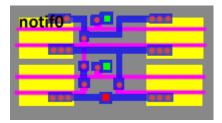
mux



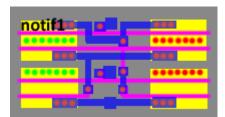
muxi



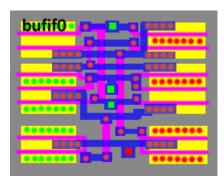
notif0



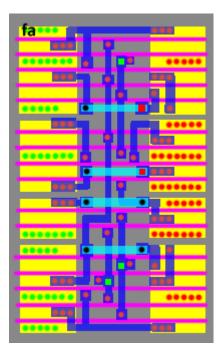
notif1



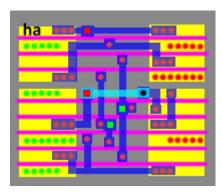
bufif0



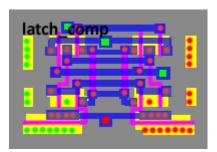
fa



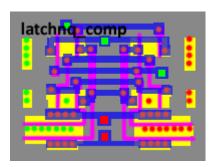
ha



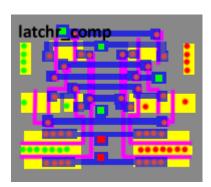
latch_comp



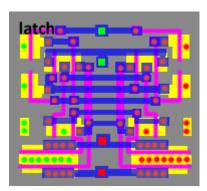
latchnq_comp



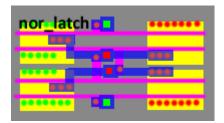
latchr_comp



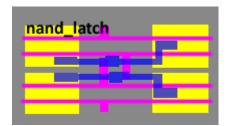
latch



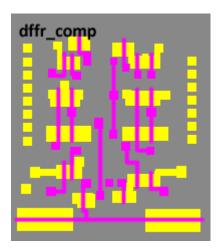
nor_latch



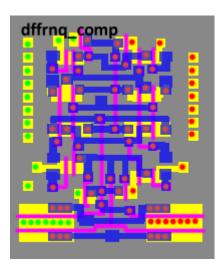
nand_latch



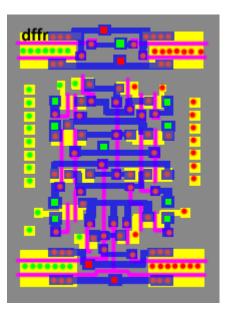
dffr_comp



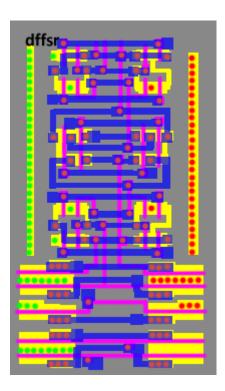
dffrnq_comp



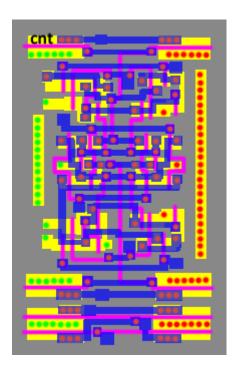
dffr



dffsr



cnt



const

