7.1. Instruction cycle times

Table 7.1 describes the symbols used in tables.

Table 7.1. Symbols used in tables

Symbol	Meaning
b	The number of busy-wait states during coprocessor accesses
m	In the range 1 to 4, depending on early termination (see *Multiplier cycle counts*)
n	The number of words transferred in an LDM/STM/LDC/STC
C	Coprocessor register transfer (C-cycle)
I	Internal cycle (I-cycle)
N	Non-sequential cycle (N-cycle)
S	Sequential cycle (S-cycle)

Table 7.2 summarizes the ARM9TDMI instruction cycle counts and bus activity when executing the ARM instruction set.

Table 7.2. Instruction cycle bus times

Instruction	Cycles	Instruction bus	Data bus	Comment
Data Op	1	1S	1I	Normal case, PC not destination
Data Op	2	1S+1I	2I	With register controlled shift, PC not destination
Data Op	3	2S + 1N	3I	PC destination register
Data Op	4	2S + 1N + 1I	4I	With register controlled shift, PC destination register
LDR	1	1S	1N	Normal case, not loading PC
LDR	2	1S+1I	1N+1I	Not loading PC and following instruction uses loaded word (1 cycle load-use interlock)
LDR	3	1S+2I	1N+2I	Loaded byte, half-word, or unaligned word used by following instruction (2 cycle load-use interlock)
LDR	5	2S+2I+1N	1N+4I	PC is destination register
STR	1	1S	1N	All cases
LDM	2	1S+1I	1S+1I	Loading 1 Register, not the PC
LDM	n	1S+(n-1)I	1N+(n-1)S	Loading n registers, n > 1, not loading the PC
LDM	n+4	2S+1N+ (n+1)I	1N+(n-1)S+4I	Loading n registers including the PC, n > 0
STM	2	1S+1I	1N+1I	Storing 1 Register
STM	n	1S+(n-1)I	1N+(n-1)S	Storing n registers, n > 1
SWP	2	1S+1I	2N	Normal case
SWP	3	1S+2I	2N+1I	Loaded byte used by following instruction
B, BL, BX	3	2S+1N	3I	All cases
SWI, Undefined	3	2S+1N	3I	All cases
CDP	b+1	1S+bI	(1+b)I	All cases

Instruction	Cycle time Cycles	Instruction bus	Data bus	Comment
LDC, STC	b+n	1S+(b+n-1)I	bI+1N+(n-1)S	All cases
MCR	b+1	1S+bI	bI+1C	All cases
MRC	b+1	1S+bI	bI+1C	Normal case
MRC	b+2	1S+(b+1)I	(b+I)I+1C	Following instruction uses transferred data
MRC	b+3	1S+(b+2)I	(b+2)I+1C	MRC to the PC
MRS	1	1S	1T	All cases
MSR	1	1S	1T	If only flags are updated (mask_f)
MSR	3	1S + 2I	3I	If any bits other than just the flags are updated (all masks other than_f)
MUL, MLA	2+m	1S+(1+m)I	(2+m)I	All cases
SMULL, UMULL, SMLAL, UMLAL	3+m	1S+(2+m)I	(3+m)I	All cases

Table 7.3 shows the instruction cycle times from the perspective of the data bus:

Table 7.3. Data bus instruction times

Instruction	Cycle time
LDR	1N
STR	1N
LDM,STM	1N+(n-1)S
SWP	1N+1S
LDC, STC	1N+(n-1)S
MCR,MRC	1C