APPLICATION NOTE

Atmel AT01607: XMEGA C Schematic Checklist

8-bit Atmel Microcontrollers

Features

- Power supplies
- Reset circuit
- Clocks and crystal oscillators
- PDI
- USB

Introduction

This application note describes a common checklist which should be used when starting and reviewing the schematics for an Atmel® AVR® XMEGA® C design.

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1. Power supplies

1.1 Power supply connections

All power supply pins of the device must be connected to the microcontroller supply.

Both V_{CC} (digital) and AV_{CC} (analog) must be connected to the same microcontroller positive supply, thus ensuring that they both share an identical supply profile. Likewise both ground pins must be connected to the same microcontroller ground reference supply.

Figure 1-1. Power supply schematic.

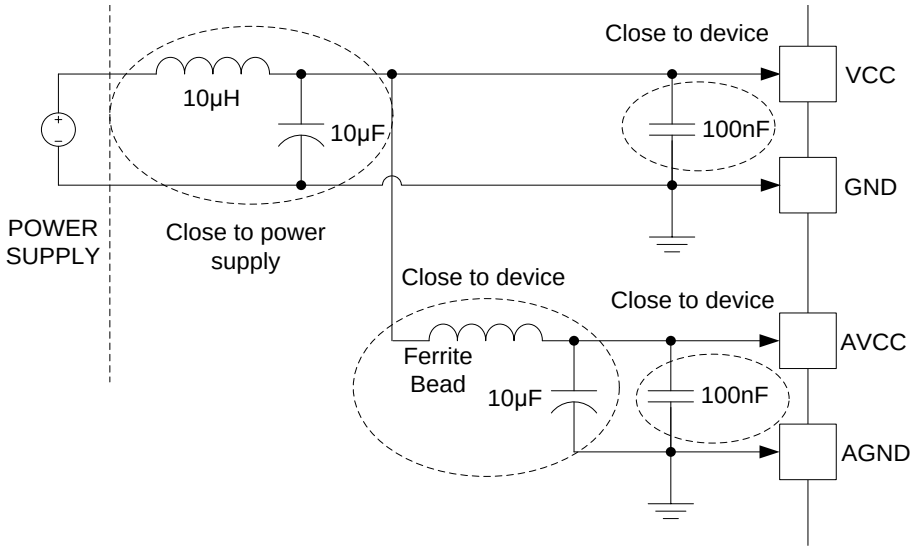


Table 1-1. Power supply checklist.

Signal name	Recommended pin connection	Description
V_{CC}	1.6V to 3.6V Decoupling/filtering capacitors 100nF (1)(2) and 10µF (1) Decoupling/filtering inductor 10µH (1)(3)	Digital supply voltage
AV_{CC}	1.6V to 3.6V Decoupling/filtering capacitors 100nF (1)(2) and 10µF (1) Ferrite bead (4) prevents the VCC noise interfering the AV_{CC}	Analog supply voltage
GND		Ground

Notes:
1. These values are given only as a typical example (that is, ceramic capacitors: 100nF, SMD 0402, X7R, 16V and 10µF, SMD1206, X5R, 6.3V) (that is, inductor: 10µH, 1.2A).
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group, low ESR caps should be used for better decoupling.
3. Wire wound inductor should be added between the external power and the V_{CC} for power filtering.
4. Ferrite bead has better filtering performance than the common inductor at high frequency. It can be added between V_{CC} and AV_{CC} for preventing digital noise from entering the analog power. The BEAD should provide enough impedance (for example, 220Ω at 100MHz, rated current 200mA, that is, Murata BLM15BB221SN1D) for separating the digital power to the analog power.

1.2 External analog reference connections

Atmel AVR XMEGA C proposes one ADC using internal references or an external analog reference (AREFA on PORTA).

The following schematic checklist is only recommended if the design is using the external analog reference. If the internal reference is used, the circuit is not necessary.

Figure 1-2. External V_{REF} schematic.

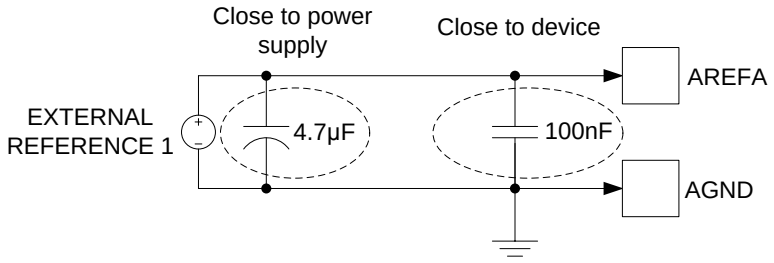


Table 1-2. External analog reference checklist.

Signal name	Recommended pin connection	Description
AREFA	1.0V to AV_{CC}-0.6V for ADC Decoupling/filtering capacitors 100nF (1)(2) and 4.7µF (1)	External reference from A_{REF} pin on PORT A
GND		Ground

Notes: 1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device.

2. External reset circuit

The external reset circuit is connected to /RESET pin only if the external reset function is used.

Figure 2-1. External reset circuit example schematic.

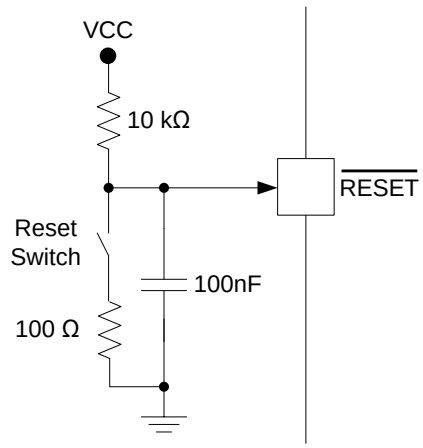


Table 2-1. Reset circuit checklist.

Signal name	Recommended pin connection	Description
$\overline{\text{RESET}}$	Reset low level threshold voltage V_{CC} = 2.7 - 3.6V: Below 0.45 × V_{CC} V_{CC} = 1.6 - 2.7V: Below 0.42 × V_{CC} (V_{CC} = 2.7V included)	Reset pin

Notes: The pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10kΩ or weaker, or be removed.

The pull-down resistor prevents from overvoltage on the RESET pin when the switch is pressed.

Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected

3. Clocks and crystal oscillators

3.1 External clock source

Figure 3-1. External clock source example schematic.

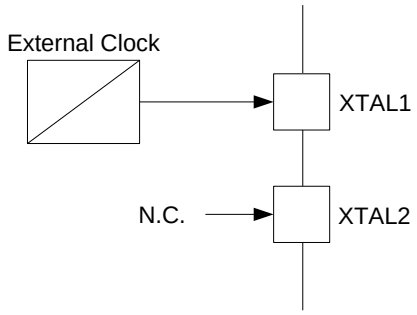


Table 3-1. External clock source checklist.

Signal name	Recommended pin connection	Description
XTAL1	XTAL1 is used as input for an external clock signal	Input for inverting oscillator pin 1
XTAL2	Can be left unconnected or used as GPIO	

3.2 Crystal oscillator

Figure 3-2. Crystal oscillator example schematic.

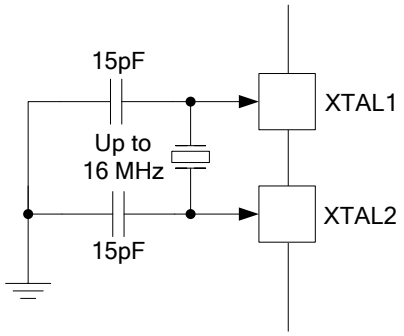


Table 3-2. Crystal oscillator checklist.

Signal name	Recommended pin connection	Description
XTAL1	Load capacitor 15pF (1)(2)	External crystal between 0.4MHz to 16MHz
XTAL2	Load capacitor 15pF (1)(2)	

Notes:
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note "AVR1003: Using the XMEGA Clock System".
2. Load capacitors should be placed close to the device and crystal pins.

3.3 Real-time oscillator

The low-frequency crystal oscillator is optimized for use with a 32.768kHz watch crystal. When selecting crystals, load capacitance and crystal's equivalent series resistance, ESR must be taken into consideration. Both values are specified by the crystal vendor.

The Atmel AVR XMEGA C oscillator is optimized for very low power consumption, and thus when selecting crystals, see Table 3-3 for maximum ESR recommendations on 9pF and 12.5pF crystals.

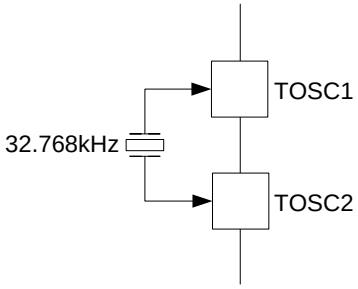
Table 3-3. Maximum ESR recommendation for 32.768kHz watch crystal.

Crystal CL [pF]	Maximum ESR [kΩ] (1)
9.0	65
12.5	30

Notes:
1. Maximum ESR is typical value based on characterization.

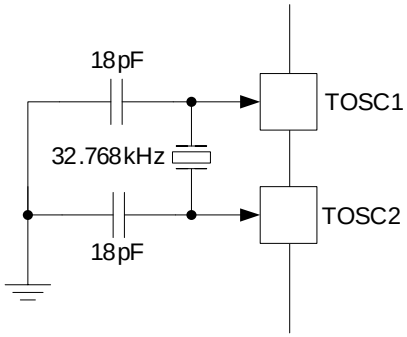
The low-frequency crystal oscillator provides an internal load capacitance of typical 3.0pF. Crystals with recommended 3.0pF load capacitance can be without external capacitors as shown in Figure 3-3.

Figure 3-3. Real-time oscillator without load capacitor.



Crystals specifying load capacitance (CL) higher than 3.0pF, require external capacitors applied as described in Figure 3-4.

Figure 3-4. Real-time oscillator with load capacitor.



To find suitable load capacitance for a 32.768kHz crystal, please consult the crystal datasheet.

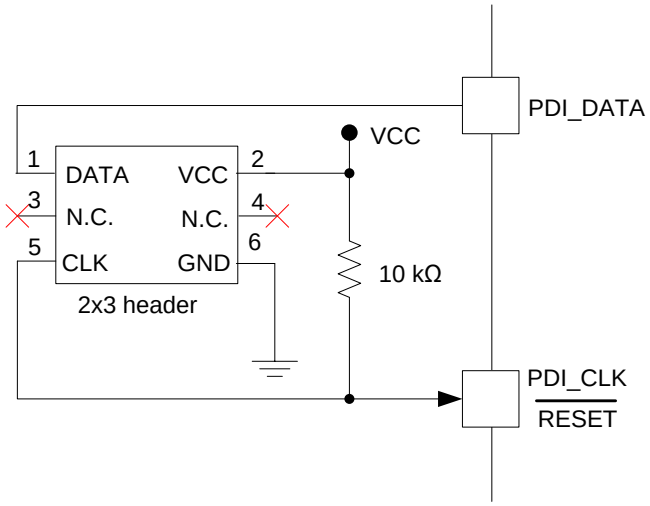
Table 3-4. External real-time oscillator checklist.

Signal name	Recommended pin connection	Description
TOSC1	Load capacitor 18pF (1)(2)	Timer oscillator pin 1
TOSC2	Load capacitor 18pF (1)(2)	Timer oscillator pin 2

Notes:
1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application notes “AVR1003: Using the XMEGA Clock System” and “AVR4100: Selecting and testing 32kHz crystal oscillators for Atmel AVR microcontrollers”.
2. Load capacitors should be placed close to the crystal, GND and device oscillator pins.

4. PDI interface

Figure 4-1. PDI interface example schematic.



The connector pinout that is shown in Figure 4-1 mates with Atmel tools like the Atmel AVR JTAGICE 3 and Atmel AVR ONE!

Table 4-1. PDI port interface checklist.

Signal name	Recommended pin connection	Description
PDI_CLK	This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10kΩ or weaker, or be removed. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.	PDI clock input / reset pin
PDI_DATA		PDI_DATA: PDI data input / output

5. USB interface

The impedance of the USB differential data line pair is 90Ω to each other and 45Ω to ground. The termination of the line is included within the Atmel AVR XMEGA C device as serial resistors. To ensure proper signal integrity, the two D+/D- signals must be closely routed on the PCB (Refer to "AVR1017: XMEGA - USB Hardware Design Recommendations" application note).

Figure 5-1. Low-cost USB interface example schematic.

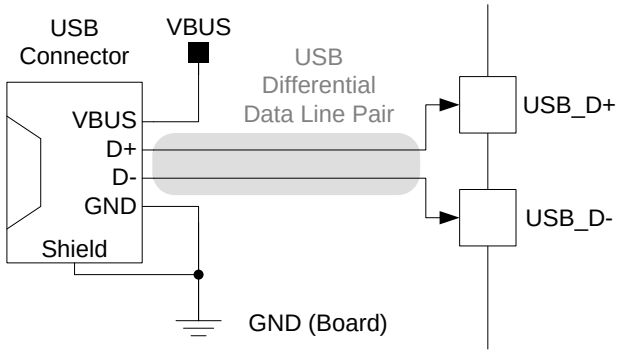


Figure 5-2. Protected USB interface example schematic.

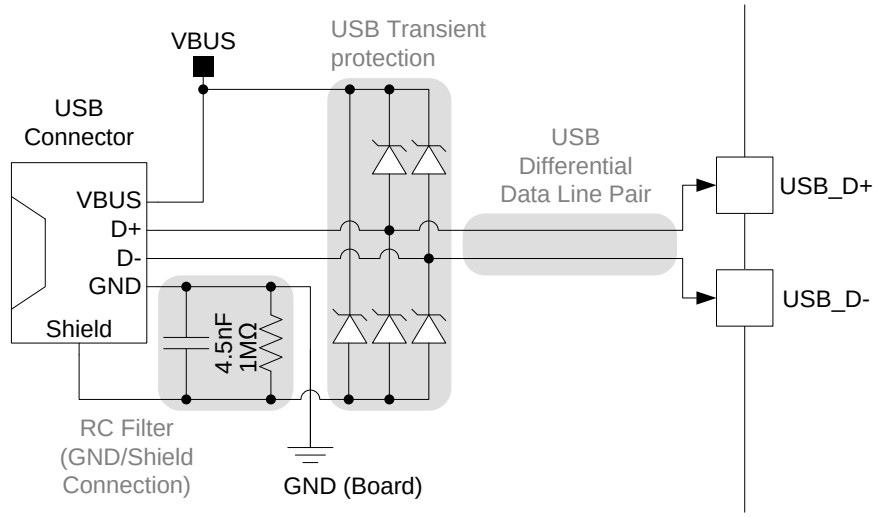


Table 5-1. USB interface checklist.

Signal name	Recommended pin connection	Description
D+	• The impedance of the pair should be matched on the PCB to minimize reflections • USB differential tracks should be routed with the same characteristics (length, width, number of vias, etc.) • Signals should be routed as parallel as possible, with a minimum number of angles and vias	USB full speed / low speed positive data upstream pin
D-		USB full speed / low speed negative data upstream pin

6. Suggested reading

6.1 Datasheets and manual

The datasheet and the manual contain block diagrams of the peripherals and details about implementing firmware for the device. The datasheet and the manual are available on http://www.atmel.com/AVR in the Datasheets & Manuals section.

7. Revision History

Doc. Rev.	Date	Comments
8466A	06/2013	Initial document release

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