Revolution EDA Preview Release First Steps

This document is written to help the users to get acquainted with Revolution EDA Preview Release. **Revolution EDA** is a complete custom IC design that currently includes:

1. Glade schematic and layout editors.
2. Xyce circuit simulator including direct access to AC, TRAN, HB, NOISE and DC analyses. SP analyses will be added soon.
3. Revolution EDA Waveform plotter with a notebook interface.
4. GCC and ADMS for inclusion of Verilog-a behavioural models.
5. Revolution EDA Verilog-A model importer and symbol generator.
6. Example Sky130 process symbols with callback functions.
7. Example Sky130 process layout parametric cells.
8. Example Sky130 process substrate taps and vias.
9. Revolution EDA simulation GUI including:
    a. Point-and-click drawing of waveforms.
    b. More than 20 performance parameters related to AC, TRAN, NOISE and HB analyses.
    c. Sweep of circuit parameters in steps or by choosing particular values.
    d. The order of sweeps can be changed.
    e. Process corners in the model libraries can be chosen.
    f. Node voltages, currents, some element values and small-signal parameters can be saved to be plotted after each simulation run.
    g. Simulation options such as transient integration methods, etc can be changed within GUI.

Revolution EDA preview release includes a few example schematics, behavioural models and layout parametric cells. In this document, we will concentrate on simulating the example transimpedance amplifier circuit that uses Sky130 process models.

We assume that the user has already installed Revolution EDA container image on his or her computer and has started the image.

First Steps

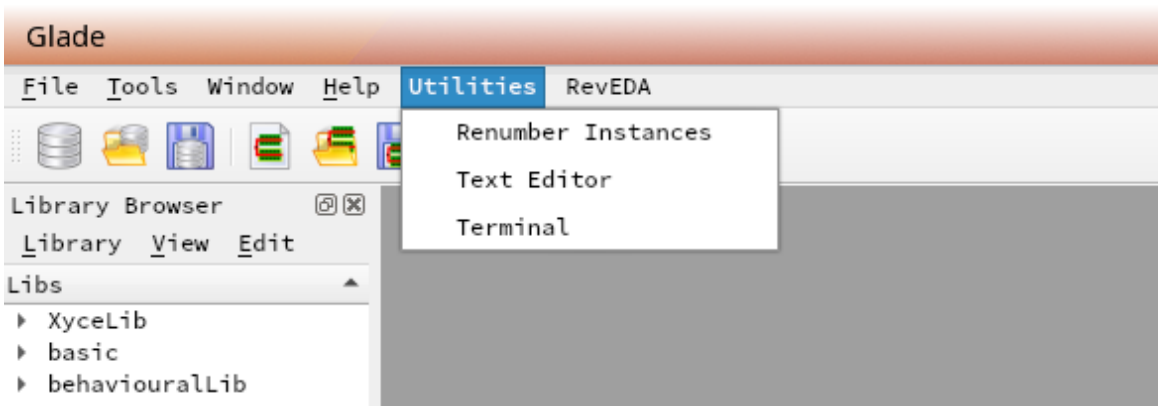
The user will be greeted with the following window once the container image is started.

As a start, we would like to review two last menu items on the menu bar.

1. Utilities

   Utilities menu has three items:

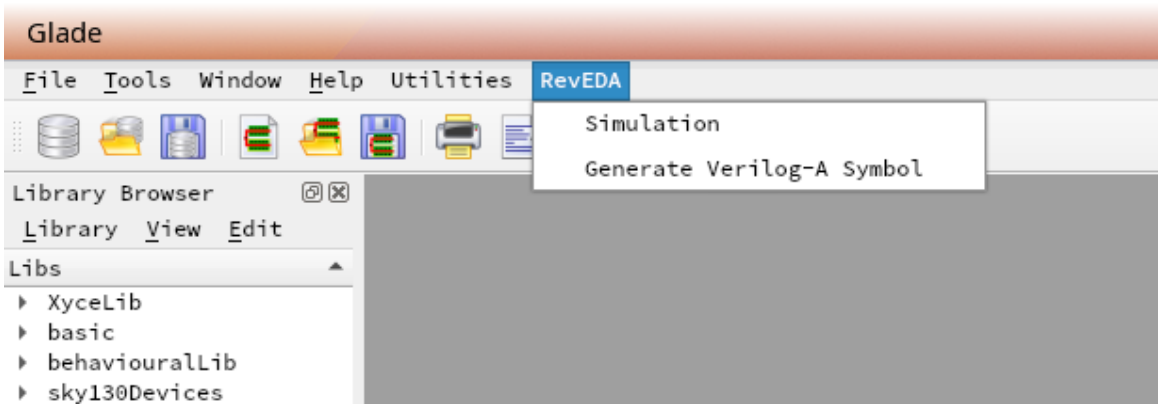
   a. *Renumber instances*: This is used to renumber instances in the schematic.
   b. *Text Editor*: It opens “Featherpad” editor to allow easy editing or viewing of text files.
   c. *Terminal*: This starts “QTerminal” to start a terminal in the container image.



2. RevEDA

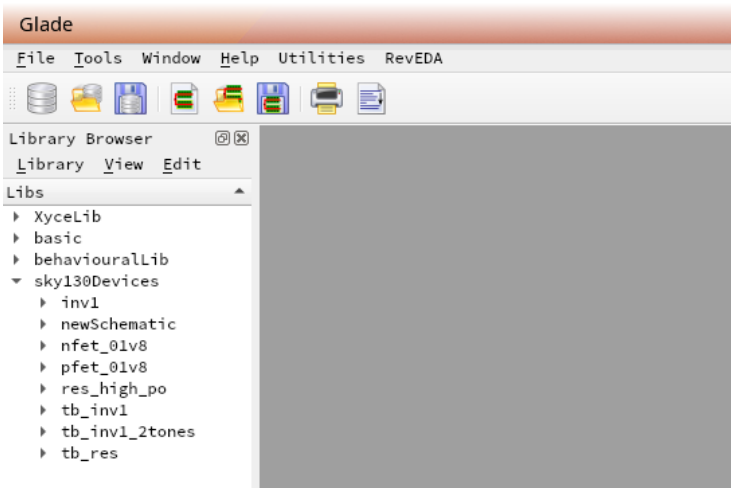
   a. *Simulation*: It starts the main simulation GUI for Revolution EDA environment.

b. *Generate Verilog-A model*: It starts a dialogue for easy integration of Verilog-A behavioural models in Xyce simulations.

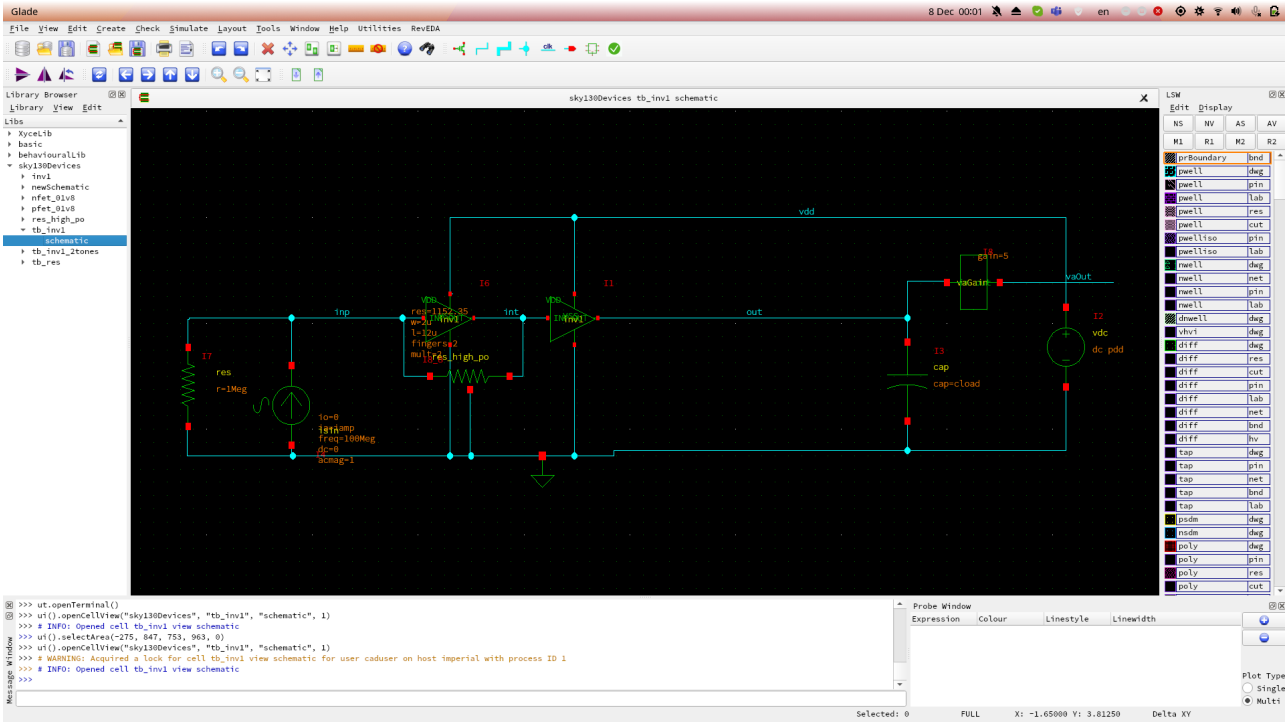


An example simulation flow

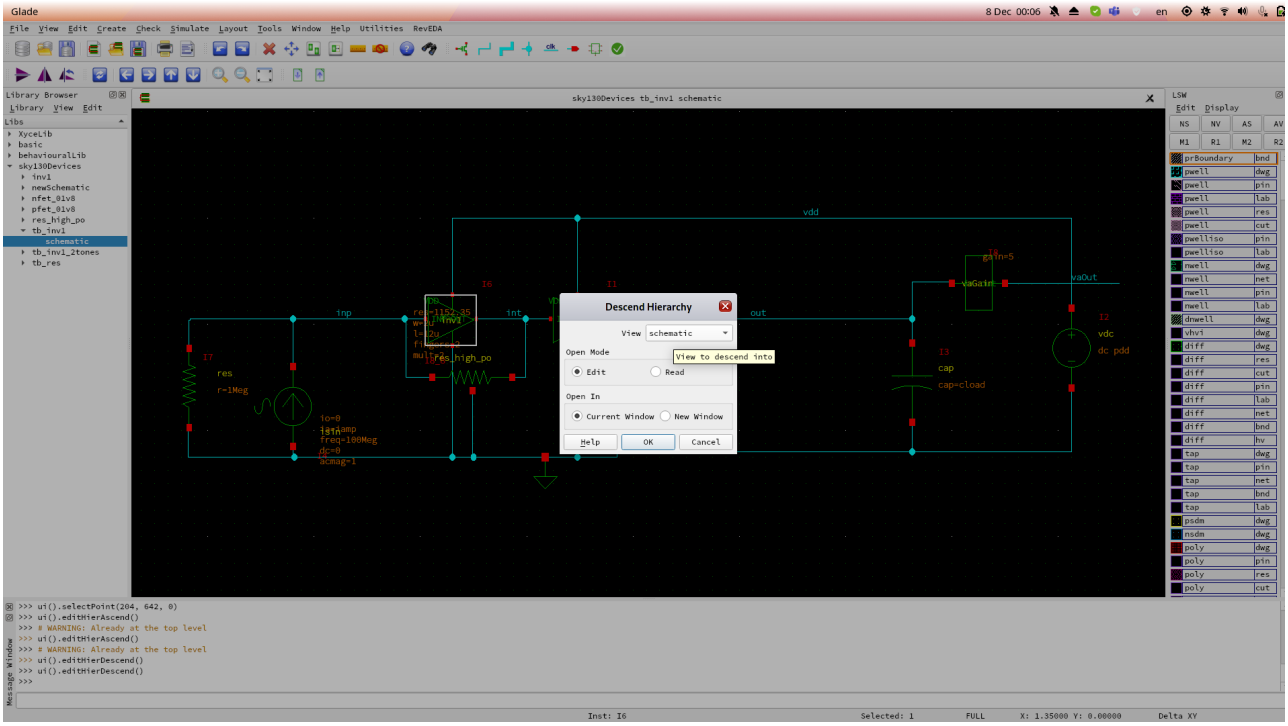
Now, click on the triangle left of the *sky130Devices* library to reveal the cells in this library:



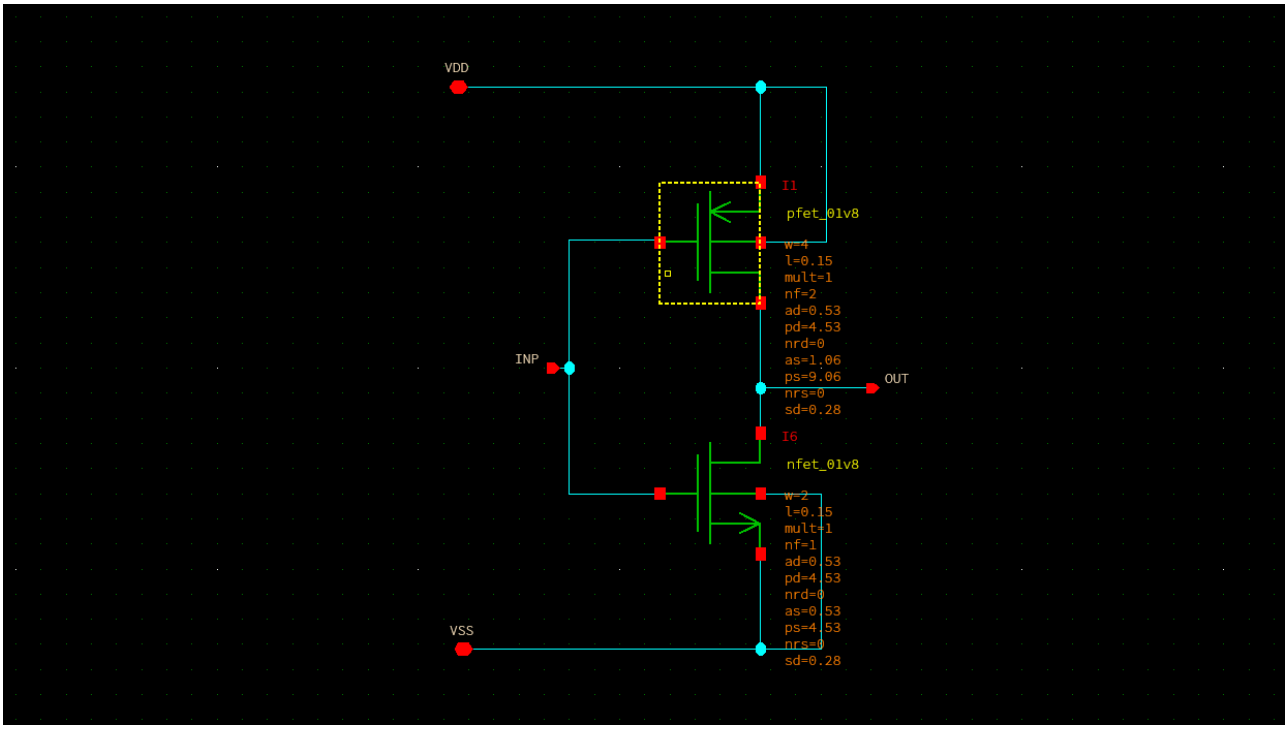
We will start with *tb_inv1* cell. Once again click on the triangle left of *tb_inv1* cell to reveal available schematic views. In this case, there is only *schematic* view. Double-click on schematic item, to open the schematic view.



Select one of the inverters denoted by *inv1* cellname in the schematic and then descend in the hiearchy. Either you could try *shift-X* key combination or click on down-arrow key on the second-row of toolbar.



We can now descend in the hierarchy to *inv1* cell. This is a simple digital inverter, used as a class-AB amplifier in this example. Note that *nfet* and *pfet* devices are annotated with not only with customary width (W), length (L), number of fingers (nf) and multiplication factor (mult), but also second-order geometry dependent parameters such as *nrd*, *nrs*, *pd*, *ps*, etc. This is one of the most important advantages of Glade schematic editor in Revolution EDA that allows the use of full Python-based **callback** functions to determine such parameters.



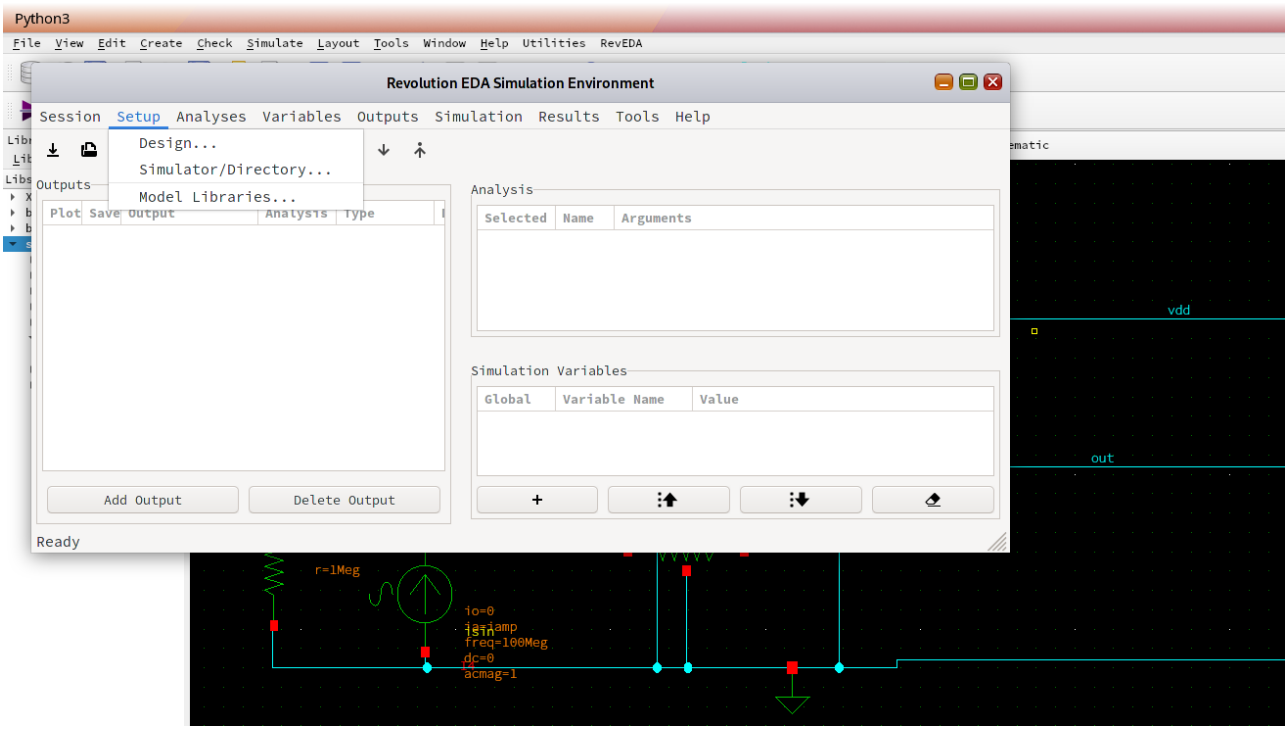
Simulation GUI

Now let's go back to the top-level test schematic and try few simulations. You could just use *Shift-B* key combination or click up-arrow on toolbar to do that.

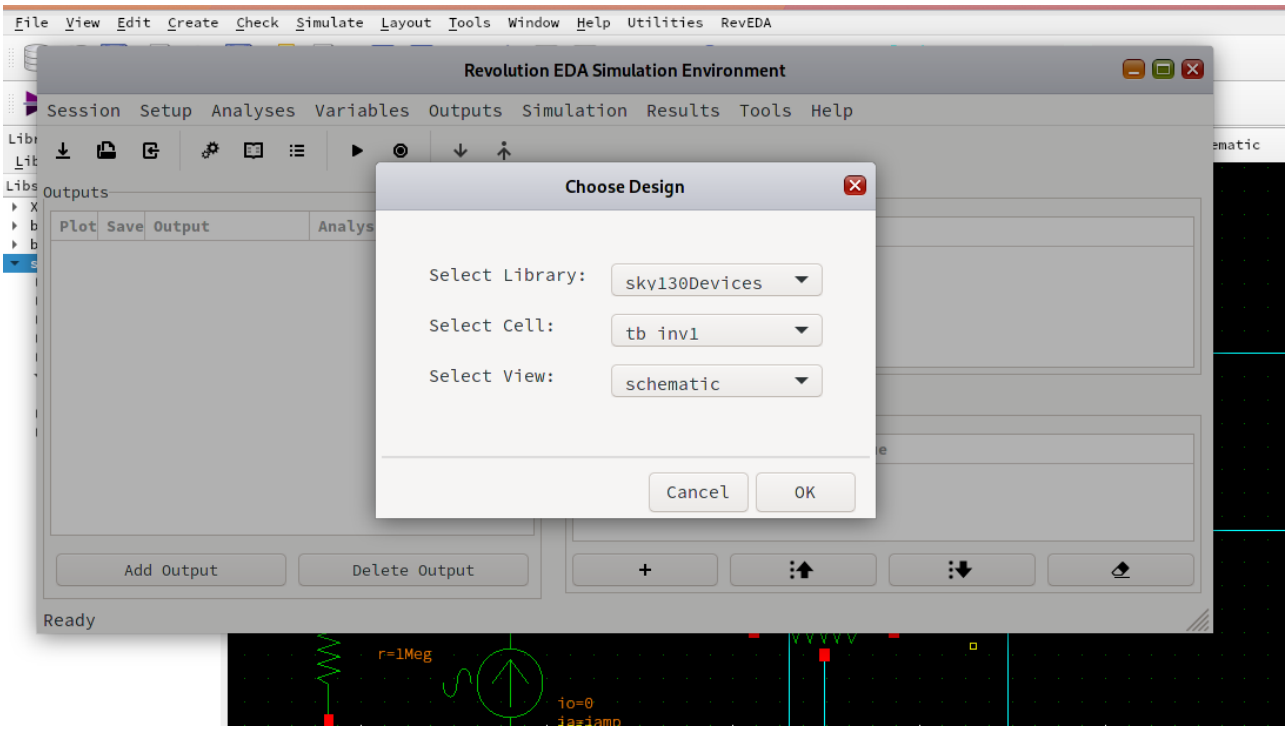
Click on RevEDA menu on the menubar and select *Simulation* menu item. You will be presented with a familiar analogue simulation environment. For this example, we will create our simulation setup from scratch. Once a simulation setup is created, it can be easily saved and restored in a YAML formatted text file. YAML files are easy to read and modify helping the reuse of such simulation setup files for other testbenches. Compare this to the legacy solutions from other EDA vendors which require lock-in to their tools.

Setup

The setup steps are logically laid out in the menubar. The first stop is *Setup* menu. Click on *Design* menu item to check if the right design is selected. This is important when more than one design is opened in Glade schematic editor.

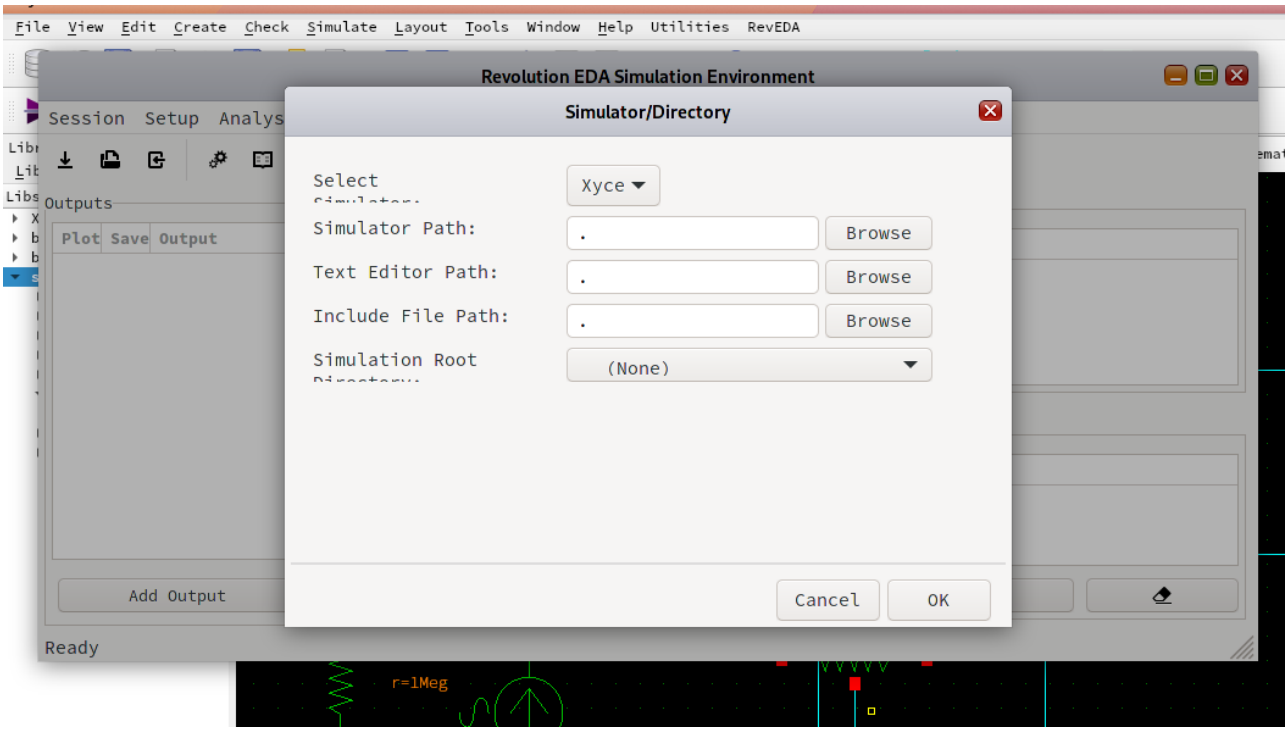


Default action is to use the schematic view when the *Revolution EDA* simulation environment is started. You could always select another library, cell and cellview in *Choose Design* dialogue.

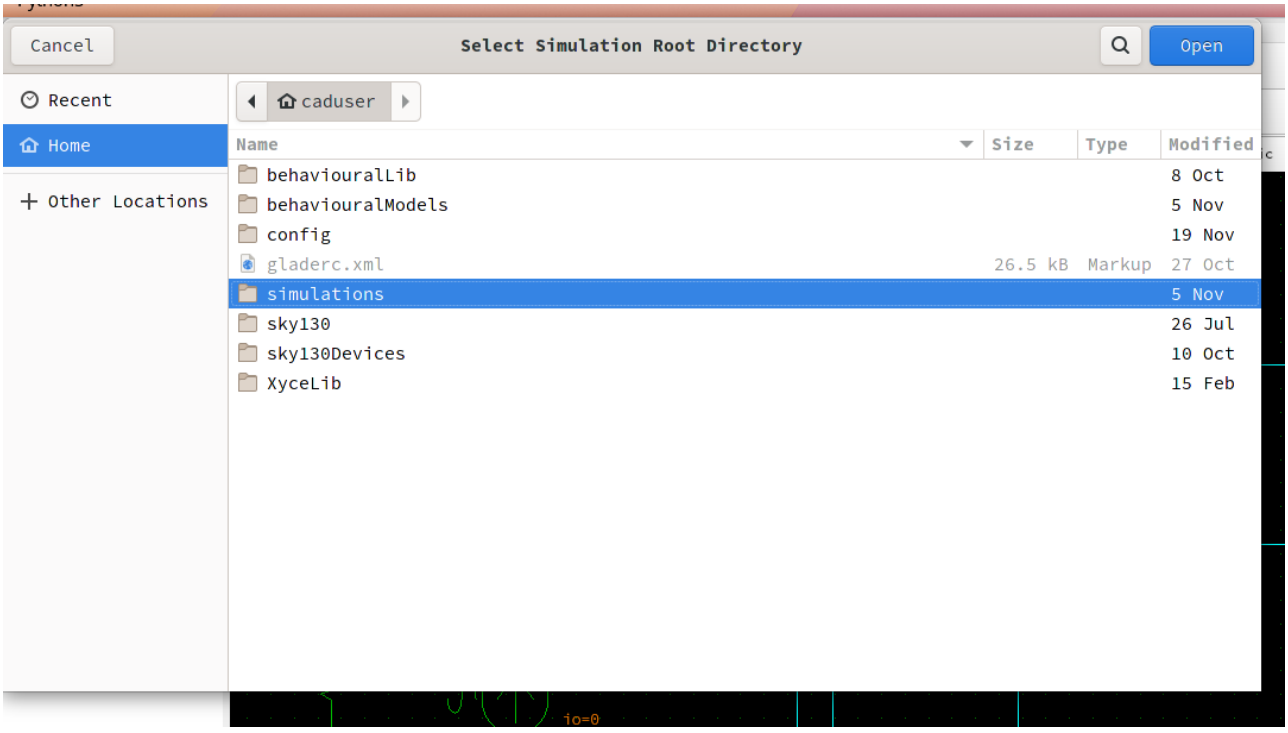


After selecting the right testbench, click OK and let's move to *Simulator/Directory...* dialogue. For the moment, only *Xyce* simulator can be used within Revolution EDA. In the future, we might add other circuit simulators as needed. The next step is the selection of the simulator path. In the container image, it is at */opt/Xyce/bin/Xyce* path. The next step is not essential for the operation of Simulation GUI is useful to be able to view simulation log and output files. Here, we are using *featherpad* editor. *Include File Path* is there when the user needs to use Xyce functions that are not yet implemented in the

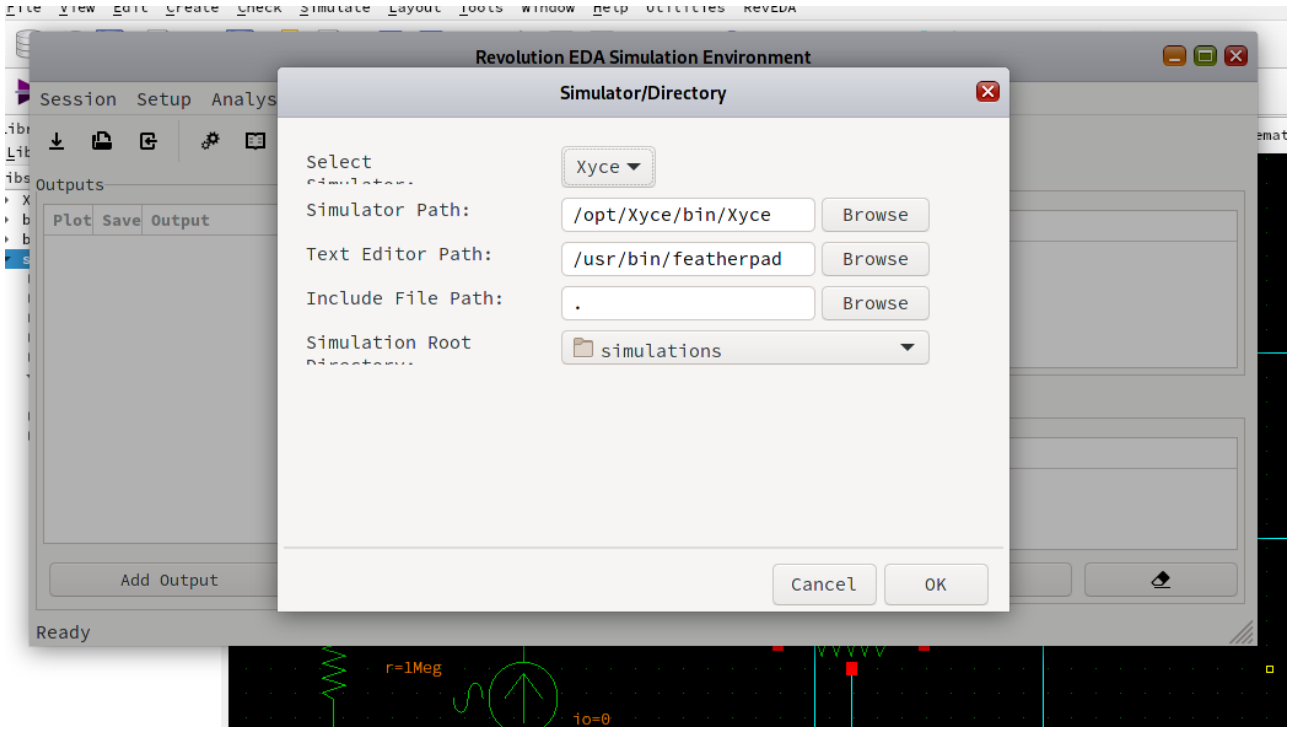
simulation GUI. We will leave empty for the moment. The next step is the selection of simulation output root directory. Revolution EDA will create a separate directory for each library and under that directory another directory with the name of testbench to store the simulation log, output and data files.



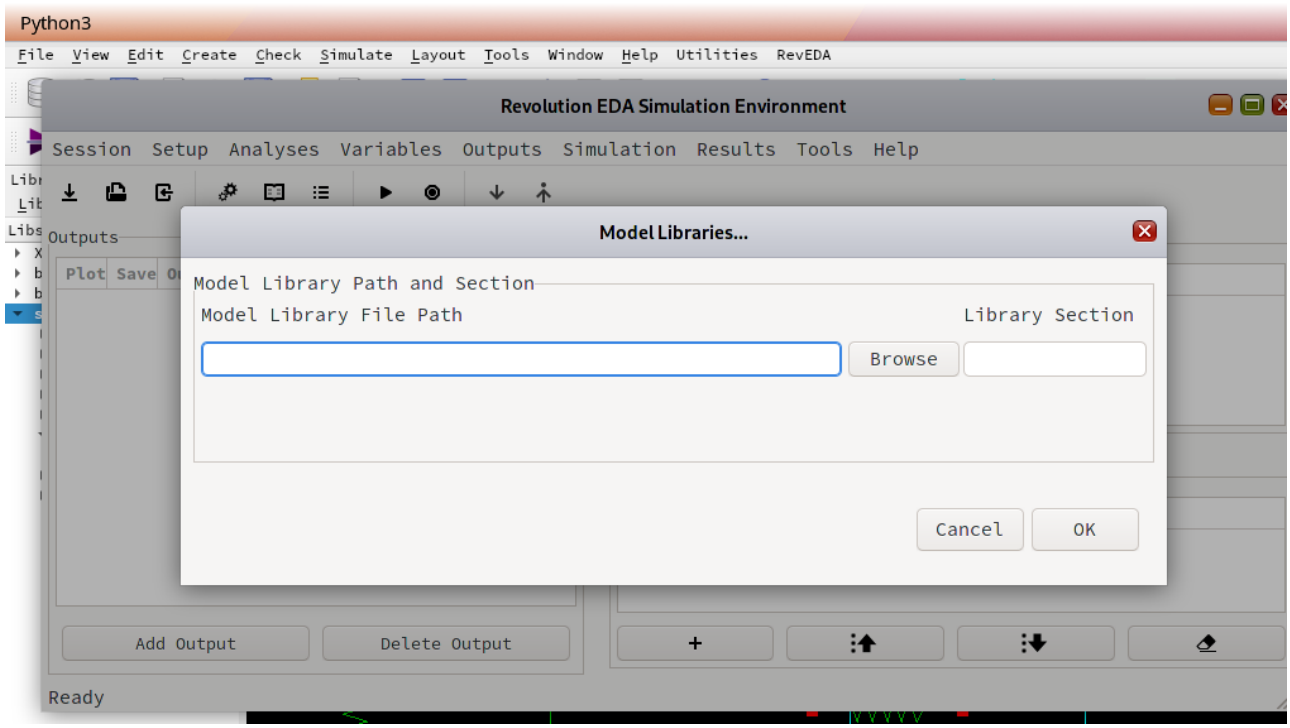
There is already a *simulations* directory under */home/caduser* path. Choose it as shown below and click *Open*.



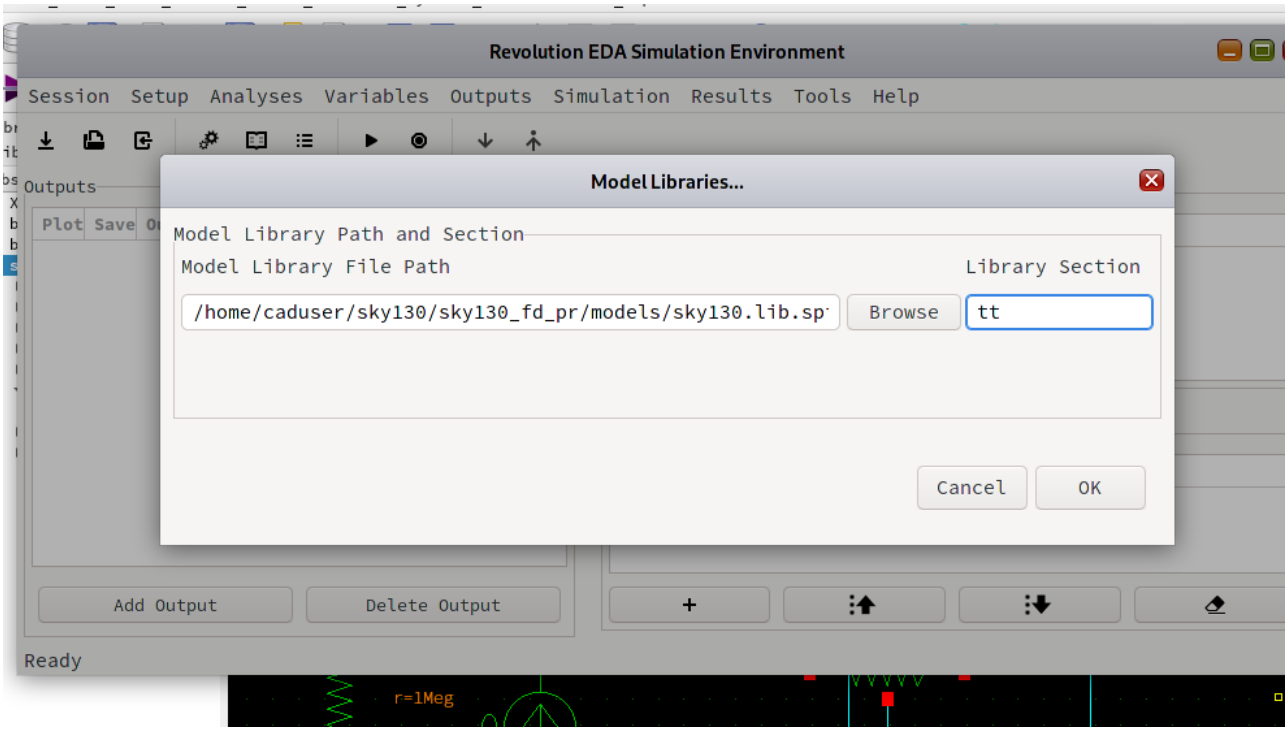
You should now the following have the following settings for your testbench:



Click *OK* to close this dialogue. The next step is the selection of simulation models using *Model Libraries...* dialogue. In this example, we will be using modified **Sky130** process models. Click on *Browse* to open file chooser dialogue.



Find and choose *sky130.lib.spice* file under */home/caduser/sky130/sky130_fd_pr/models/* path and click *Open* to return to *Model Libraries...* dialogue. Enter *tt* in the *Library Section* line and click OK.



Library section *tt* signifies that we selected so-called *typical-typical* models. We could also have used other process corners such as *fast-fast * by entering *ff* or *slow-slow* by entering *ss*. You need to check Sky130 model documentation to see which process corners are available. Now click *OK* to finish with the setup phase.

Analyses

The next step is setting up the simulation analyses. Revolution EDA currently can handle five analyses types:

1. TRAN
2. AC
3. DC
4. NOISE
5. HB

A sixth analysis type, SP, will be added soon.

Click on *Analyses* menu and select *Analyses...* menu item. This dialogue has a tabbed interface to allow setting up the parameters for one or more analyses. *Xyce* can normally do only one simulation analysis at each run. Revolution EDA sets a run for each selected analysis type and runs them as needed.

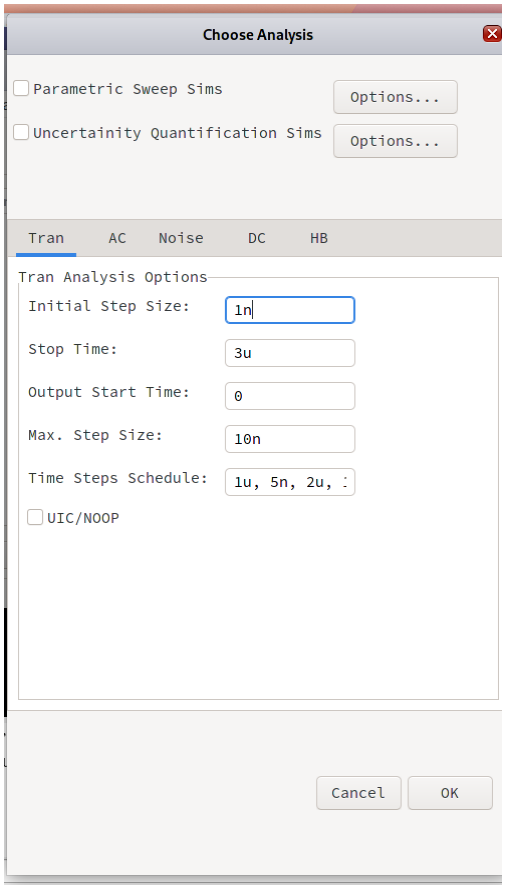
TRAN Analysis

TRAN analysis options follow Xyce transient analysis parameters. You can set here most important parameters related to Xyce transient analysis:

1. **Initial Step Size**: This is the value of first time step.
2. **Stop Time:** Duration of the transient analyses.
3. **Output Start Time:** The output will be saved at the output file starting at this time.
4. **Max. Step Time:** Sets the maximum time step. Xyce defaults to

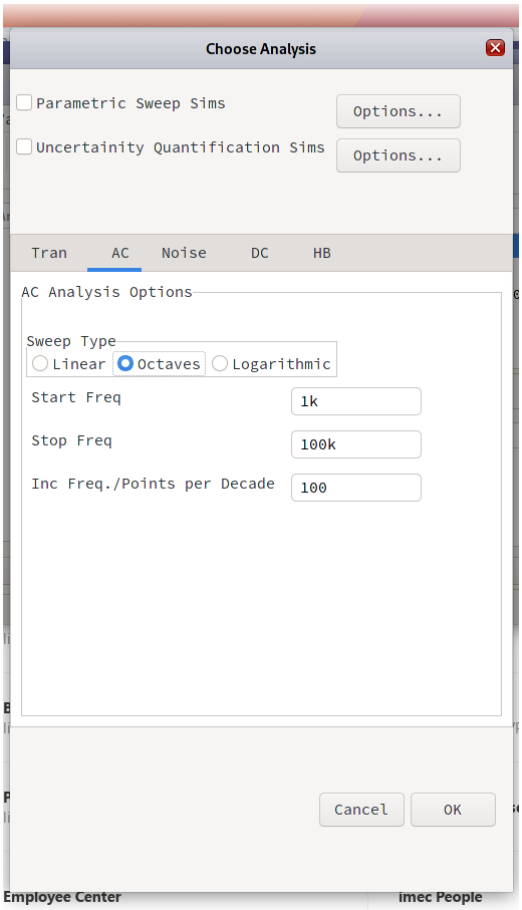
$$\text{Max. Step Time} = \frac{\text{Stop Time- Inital Step Size}}{10}$$

5. **Time Steps Schedule:** Defines a schedule of time steps for transient simulations. More information can be found in Xyce Reference Guide.
6. **UIC/NOOP**: If you prefer Xyce to skip the operating point calculation, then you can check this box. This is especially useful for circuits with more than one stable operating points or more oscillators. It is possible to set individual node voltage initial conditions inside Revolution EDA.



AC Analysis

In AC analyses, the frequency is swept. Frequency sweep type can be linear, or logarithmic in octaves or decades. For linear sweep, the number of frequency points is entered. For logarithmic sweeps number of frequency points per octave or decade is determined.



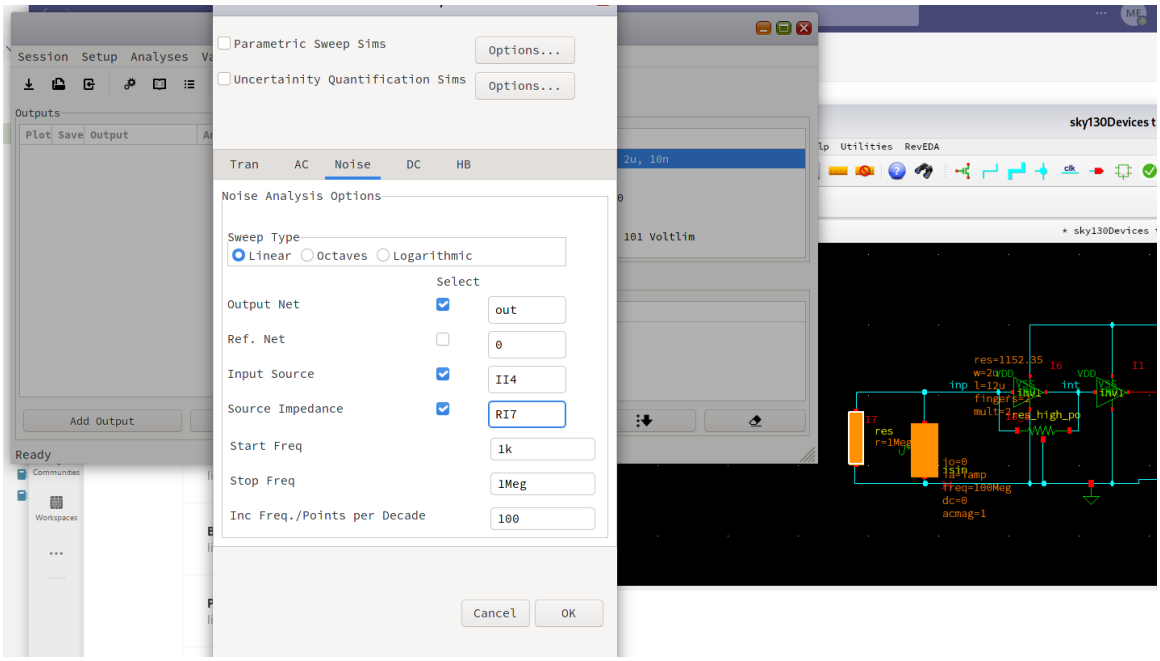
Noise Analysis

Noise analysis is similar to AC analysis. However it requires the input of some extra parameters. For more detailed information, please refer to Xyce Reference and User Guides.

Output Net: The circuit output node. To select a node on the schematic, just click checkbox under *Select* column, and then select a node on the schematic. Make sure that cursor is now in node name entry field and press *ESC* (escape key). Node name should be correctly displayed in the relevant field. The other fields can be also filled similarly. If *source impedance* field is filled, Revolution EDA can also calculate *noise figure* and *noise factor* over the simulation frequencies.

a. **Output Net**: Output net for the noise simulations.
b. **Ref Net:** Normally *0*, i.e. ground, but could be another node.
c. **Input Source**: Signal source to which output noise will be referred to.

d. **Source impedance:** Impedance of the signal source, important for *noise figure* and *noise factor* calculations.
e. **Start Freq**, **Stop Freq** and **Inc Freq./Points Per Decade**: Frequency specifications.



When an instance is selected for *input source* and *source impedance* fields, the selected instances will be marked by an orange rectangle over the instances. Once the dialogue is closed, this marking rectangles will be cleared.