ECE2029 --- Introduction to Digital Circuit Design

Homework 3: Due by 12 pm Friday 22 Nov 2013

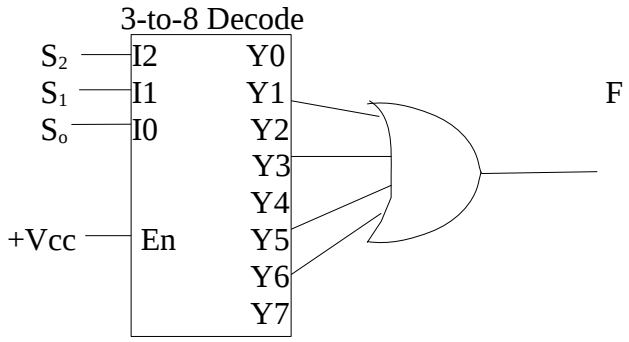
(place completed homework in the 2029 box outside MY office AK-011)

To ensure proper grading & return, attach the cover sheet to the FRONT of you homework

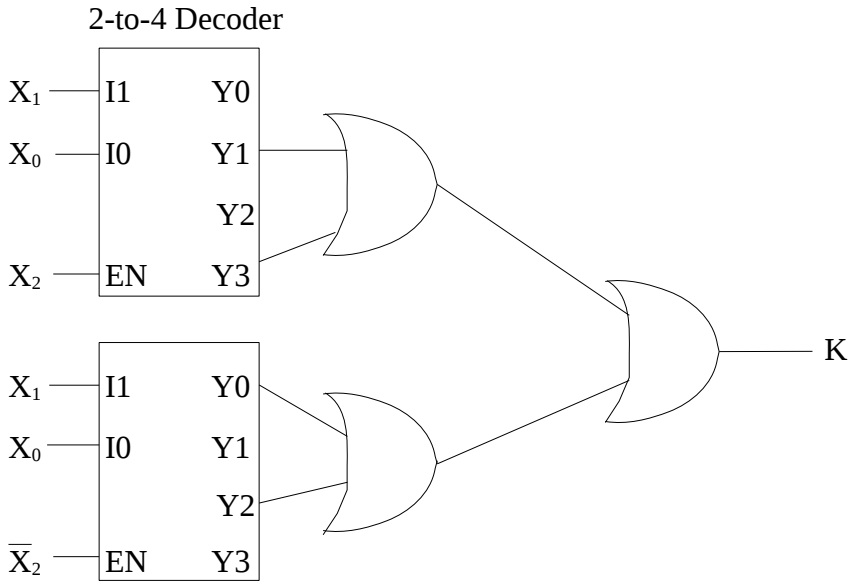
- Always complete the reading assignments *before* attempting the homework problems.
- Show *all* of your work. Underline, circle or box each result.
- *Always* write neatly. The grader can not be expected to GUESS what you meant to do!
- Points are as indicated.

Problem 1 (10 pts)

a) The circuit below uses a generic 3-to-8 decoder (see Vahid 2.9, class notes). What is the logic function *F* produced by this circuit? Complete a truth table and derive the logic expression of F (with S0, S1 and S2 as input and F as output). Notice that the decoder *is enabled*.



b) What is the logic expression implemented by the circuit below?



Problem 2 (10 pts)

a. Design an 8-to-1 by 1 bit MUX using two 4-to-1 by 1 bit multiplexers with enables. (*Hint*: Use the enables, EN).

b. Design a 4-to-1 by 4 bit MUX using four 4-to-1 by 1 bit multiplexers;

Problem 3 (10 pts) For logic expression $G = \overline{X}\, Y\, \overline{Z} + \overline{Y}\, Z + X\, \overline{Z}$

a. What is the full sum of minterm expression for F?

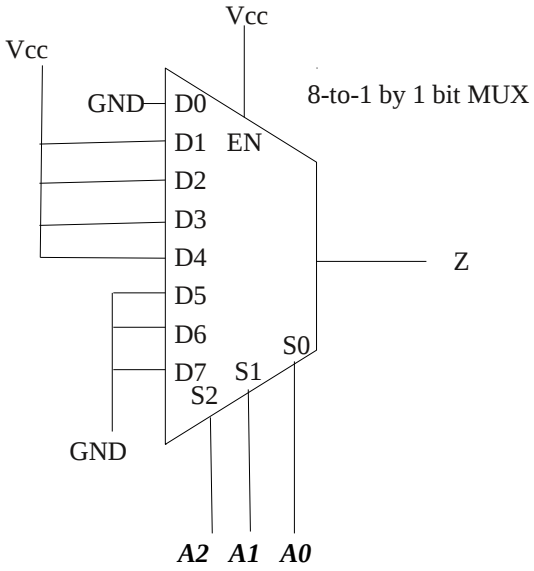
b. Use a 3-to-8 Decoder plus an OR gate to implement F.

Problem 4 (10 pts) = Vahid 2.76

Problem 5 (10 pts)

Fill in the truth table for this circuit

A2	***A1***	***A0***	***Z***



Problem 6 (10 pts)

a) Implement the logic function given by the truth table in Problem 5 in complete Verilog module using Boolean assign statements.

b) Implement the logic function given by the truth table in Problem 5 in complete Verilog module using conditional statements.

Problem 7 (10 pts)

a) Determine the shortest and worst case propagation delays for the circuit in Figure 2.17b (pg 49) assuming that $t_{p_{and}}$ = 1.5 ns $t_{p_{or}}$ = 1.5 ns and $t_{p_{not}}$ = 1.25 ns.

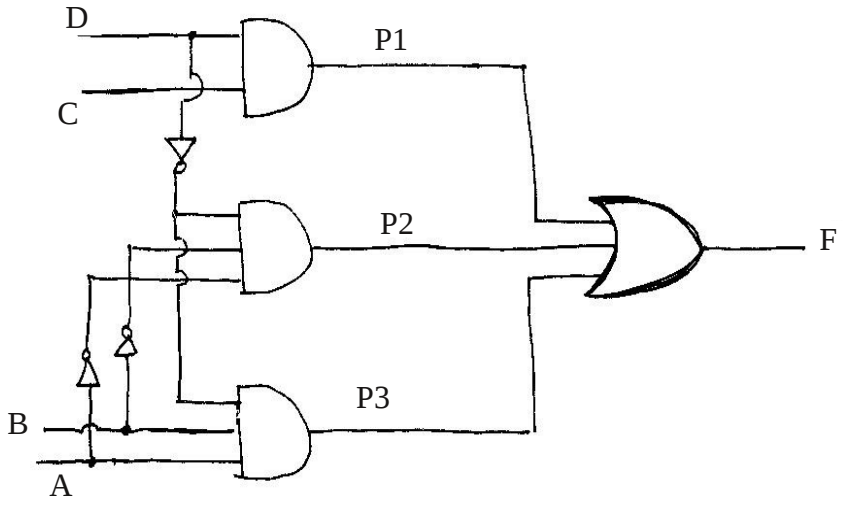
b) Draw a timing diagram showing the effects of the inputs *a* = 0, *b* = 0, c = 1 transitioning to *a* = 1, *b* = 0, *c* = 1 then transitioning to *a* = 1, *b* = 0, *c* = 0.

Problem 8 (10 pts)

a. What logic expression F comes most directly from this logic circuit?

b. Use a Karnaugh Map to identify any potential Static Hazards in this circuit.

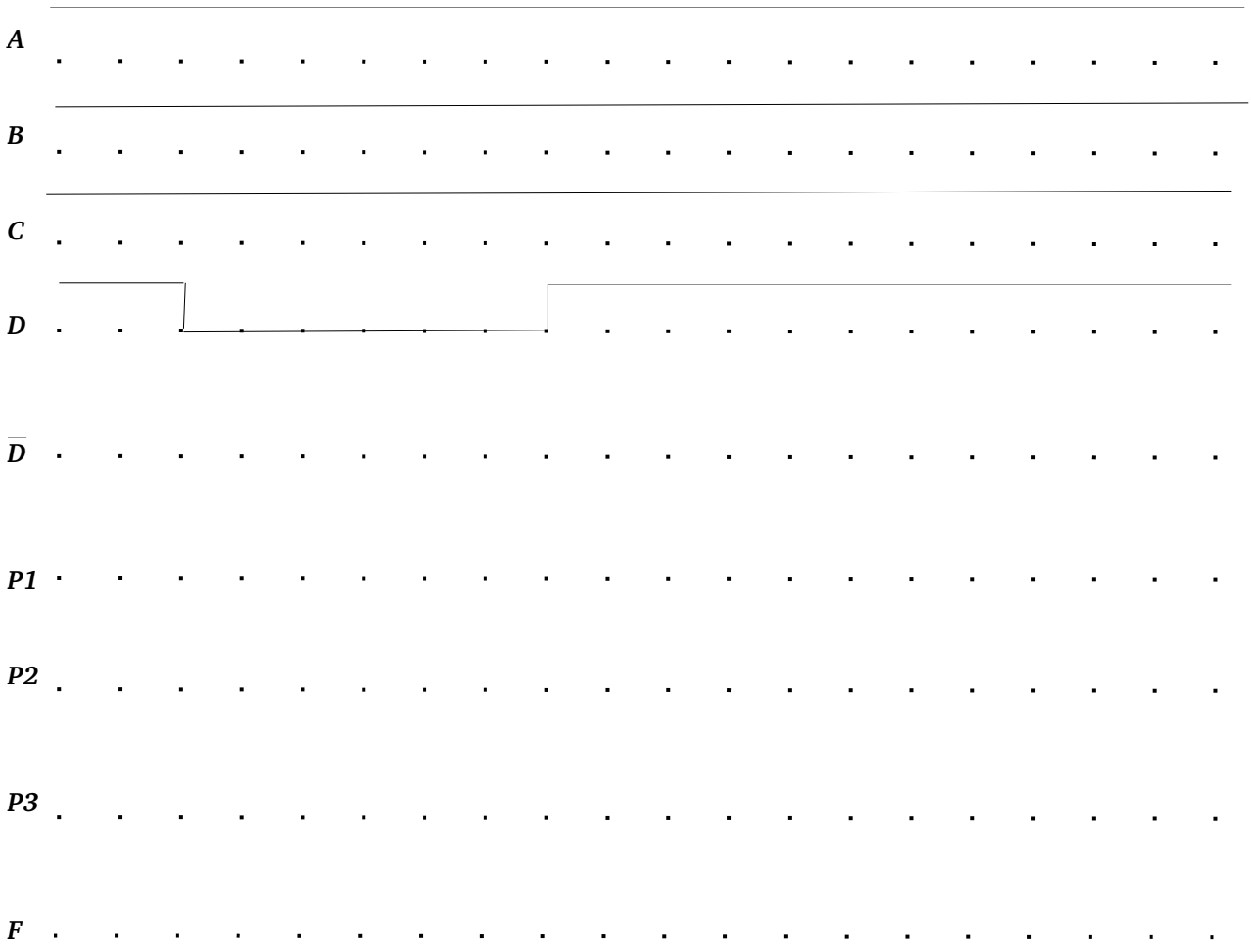
c. Find a hazard free expression for F and draw that circuit.



Problem 9 (10 pts)

Complete the timing diagram below for the original circuit in Problem 8 using the propagation delays given. Assume that the inputs X=Y=X=1 and input W transitions as shown. Assume each horizontal division is 1.0 ns. Circle any static hazards encountered.

	AND	**OR**	**NOT**
$t_{p_{HL}}$	2.0 ns	1.8 ns	2.2 ns
$t_{p_{LH}}$	2.0 ns	1.8 ns	2.4 ns


A
B
C
D
$\overline{D}$
P1
P2
P3
F

ECE2029 Homework #3

Submitted by:_____

ECE Box #:_____

Date:_____

Question	Grade
1	
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