RN8209C/RN8209D User Manual

Data: 2016-01-26

Rev: 3.5

Update Log

Version	Time	Contents
V3.5	2016-01-26	Translated from Chinese version V1.5

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1 Introduction

1.1 Features

√ Measurement

- Three channels of Σ-△ ADC are provided.
- The active energy accuracy is less than 0.1% (< 0.1%) over a dynamic range of 8000:1 with the IEC62053-22: 2003 Standard supported.
- The reactive energy accuracy is less than 0.1% (< 0.1%) over a dynamic range of 8000:1 with the IEC62053-23: 2003 Standard supported.
- Two-channel current and one-channel voltage RMS is provided, with the RMS accuracy <0.1% over the 1000:1 dynamic range.
- One pulse frequency generator which can be used for user-defined power electrical energy accumulation points.
- Provide instantaneous sample values of the three-way ADC.
- No-load threshold is adjustable.
- Reverse active power indication is provided.
- Provide voltage channel frequency measurement.
- Provide voltage channel zero-crossing detection.
- Reference baseline monitoring function

√ Software meter calibration

- The meter constant (HFConst) is adjustable.
- Gain and phase calibration is provided.
- Offset calibration is provided for active, reactive and RMS.
- Acceleration is provided for small-signal meter calibration.
- Automatic checksum is provided for configuration parameters.

√ SPI /UART interfaces are provided

√ Power supply monitoring is provided

√☐ Energy registers have timed freeze function

√ **UART's RX input pin along with pin reset function**

√☐ RN8209 + 5V / 3.3V power supply, the power consumption is typically 15mW @ 5V, 8mW @ 3.3V

√ Built-in 1.25V ± 1% reference voltage, with typical temperature coefficient of 5ppm / ℃,

√ SSOP24 lead-free package is adopted for RN8209D, SOP16 lead-free package is adopted for RN8209C.

1.2 Functions

RN8209 can measure active power, reactive power, active energy and reactive energy, and can provide two-channel independent active power and RMS, voltage RMS, line frequency, zero-crossing interrupt, etc. to achieve flexible anti-tampering solutions.

RN8209 supports all-digital gain, phase and offset calibration, with the active and reactive energy pulses

respectively output from the pins of PF and QF.

RN8209D provides two serial interfaces SPI and UART, to facilitate communication with the external MCU.RN8209C provides only one serial interfaces UART, and the baud rate is fixed at 4800bps

The internal power supply monitoring circuit of RN8209 can ensure reliable operation of the chip when power on and off.

1.3 Block Diagram of Functions

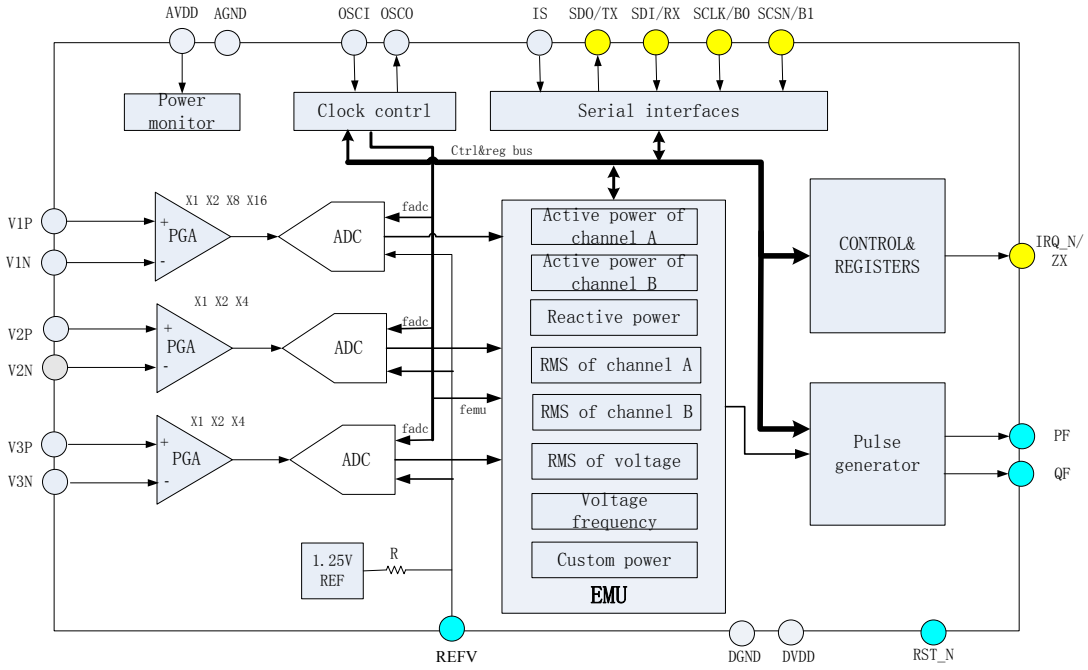


Figure 1-1 Block Diagram of system

1.4 Pin Definitions

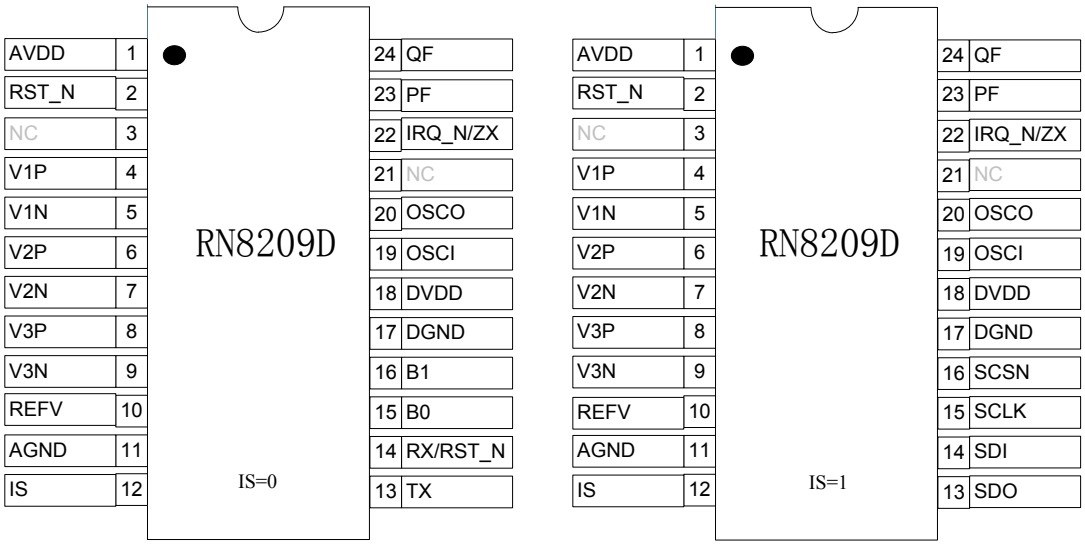


Figure 1-2 RN8209D-SSOP24 Pin Assignment

Table 1-1 RN8209D-SSOP24 Pin Functions

Pins	Signs	Features	Function Descriptions
1	AVDD	Power supply	The pin of analog power supply is used to provide power supply to the analog portion of the chip. This pin should use an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 3V-5.5V. When the typical power supply voltage (e.g. 5V or 3.3V) is selected, the fluctuation of the power supply should be guaranteed in the range of ±10%.
2	RST_N	Input	Reset pin, active at a low level. When at a low level, the chip is in a reset state. The pin should be connected to an external pull-up resistor.
3	NC	NC	Not connected
4,5	V1P, V1N	Input	Positive and negative analog input pins of current Channel A - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
6,7	V2P, V2N	Input	Positive and negative analog input pins of current Channel B - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
8,9	V3P,V3N	Input	Positive and negative analog input pins of the voltage channel - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
10	REFV	Input/Output	1.25V reference voltage input and output pins – The external reference source can be directly connected to this pin. Whether internal or external reference source is adopted, this pin should use a 1μF capacitor and a 0.1μF capacitor paralleled for decoupling.
11	AGND	Power supply	Analog ground
12	IS	Input	Serial communication type selection pin – it is used to determine the communication interface type of the chip. If IS = 0, choose UART as the communication interface; if IS = 1, choose SPI as the communication interface. Internal floating, external pull-up or pull-down is demanded.
13	SDO/TX	Output	SDO and TX multiplexed pins, When IS = 1, this pin will act as SPI serial data output SDO. After reset, this pin features a high impedance output. When IS = 0, it will act as TX the data output pin of the serial interfaces UART
14	SDI/RX /RST_N	Input	When IS = 1, this pin will be an SPI serial data input SDI, which is a 3.3V/5V compatible pin. When IS = 0, RX the data input pin of the serial interfaces UART, it is also the reset pin, which is a 3.3V/5V compatible pin. The interior reset circuit and UART communication circuit of RN8209D is fully independent, the reset function of this pin is the same as independent reset pin.

15	SCLK/B0	Input	When IS = 1, this pin will act as an SPI serial clock input pin, which is a 3.3V/5V compatible pin. When IS = 0, it will act as B0 which combined with B1 is used to determine the baudrate of UART. {B1,B0}=00 2400 baudrate; {B1,B0}=01 4800 baudrate {B1,B0}=10 9600 baudrate; {B1,B0}=11 19200 baudrate
16	SCSN/B1	Input	When IS = 1, this pin will be for an SPI chip-select signal pin (active at a low level), as well as a 3.3V/5V compatible pin. Internal floating, an external pull-up is demanded. When IS = 0, this pin will act as B1, see the description of B0.
17	DGND	Power supply	Digital ground
18	DVDD	Power supply	Digital power supply pin - Used to provide power supply to the digital part. This pin should have an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 3V-5.5V. When the typical power supply voltage (e.g. 5V or 3.3V) is selected, the fluctuation of the power supply should be guaranteed in the range of ±10%.
19	OSCI	Input	Input terminal of external crystal or external clock input – The crystal frequency is typically 3.579545MHz. External capacitor is typically 15Pf ~ 22pF, the interior has about 4M ohm resistor jumper, jumper no need to add external resistors. Require external crystal ESR of less than 50 ohms.
20	OSCO	Output	The output of an external crystal.
21	NC	NC	Not connected
22	IRQ_N /ZX	Output	Interrupt / indicator output when a zero-crossing is detected - After reset, it will serve as an interrupt pin. when Zxcfg = 0 (EMUCON-bit7) as an interrupt request IRQ_N; When Zxcfg = 1 (EMUCON-bit7), it will serve as ZX: it will output a signal when a zero-crossing in voltage channel is detected.
23	PF	Output	Pulse output of active energy, low-level output by default. It's frequency will indicate the value of transient active power, able to achieve a 5mA output and current sinking.
24	QF	Output	Pulse output of reactive energy or pulse output of user-defined energy, low-level output by default. It frequency will indicate the value of transient reactive power or of transient user-defined power. User-defined power can be select as active power of the second channel, vector sum of active power of the two channels the user-defined power register. It is able to achieve a 5mA output and current sinking.

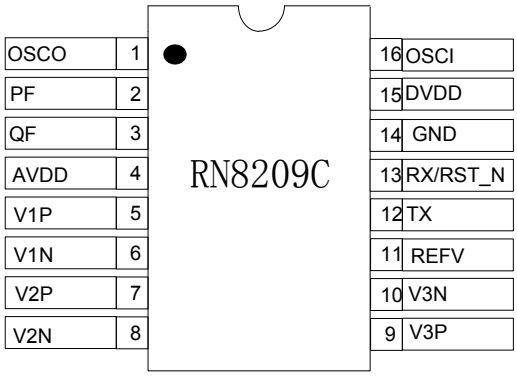


Figure 1-3 RN8209C-SOP16L Pin Assignment

Table 1-2 RN8209C Pin Functions

Pins	Signs	Features	Function Descriptions
1	OSCO	Output	The output of an external crystal.
2	PF	Output	Pulse output of active energy, low-level output by default. It's frequency will indicate the value of transient active power, able to achieve a 5mA output and current sinking.
3	QF	Output	Pulse output of reactive energy, low-level output by default. It frequency will indicate the value of transient reactive power, able to achieve a 5mA output and current sinking.
4	AVDD	Power supply	The pin of analog power supply is used to provide power supply to the analog portion of the chip. This pin should use an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 3V-5.5V. When the typical power supply voltage (e.g. 5V or 3.3V) is selected, the fluctuation of the power supply should be guaranteed in the range of ± 10%.
5,6	V1P, V1N	Input	Positive and negative analog input pins of current Channel A - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
7,8	V2P, V2N	Input	Positive and negative analog input pins of current Channel B - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
9,10	V3P,V3N	Input	Positive and negative analog input pins of the voltage channel - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 1000mV, and the maximum withstand voltage is ± 6V.
11	REFV	Input/Output	1.25V reference voltage input and output pins – The external reference source can be directly connected to this pin. Whether internal or external reference source is adopted, this pin should use a 1μF capacitor and a 0.1μF capacitor paralleled for decoupling.
12	TX	Output	TX the data output pin of the serial interfaces UART.
13	RX/RST_N	Input	RX the data input pin of the serial interfaces UART, also the reset pin of the chip, when the input level of this pin is maintained at low for more than 20msm, the RN8209C will reset. The interior reset circuit and UART communication circuit of RN8209C is fully independent, the reset function of this pin is the same as independent reset pin.
14	GND	Ground	**Ground of chip, be attention that the pin should not be directly connected to the decoupling capacitor of DVDD and other ground points with lots of digital noise, but to keep away from those.**
15	DVDD	Input	Digital power supply pin - Used to provide power supply to the digital part. This pin should have an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 3V-5.5V. When the typical power supply voltage (e.g. 5V or 3.3V) is selected, the fluctuation of the power supply

			should be guaranteed in the range of ±10%.
16	OSCI	Input	Input terminal of external crystal or external clock input – The crystal frequency is typically 3.579545MHz. External capacitor is typically 15Pf ~ 22pF, the interior has about 4M ohm resistor jumper, jumper no need to add external resistors. Require external crystal ESR of less than 50 ohms.

1.5 Typical Application

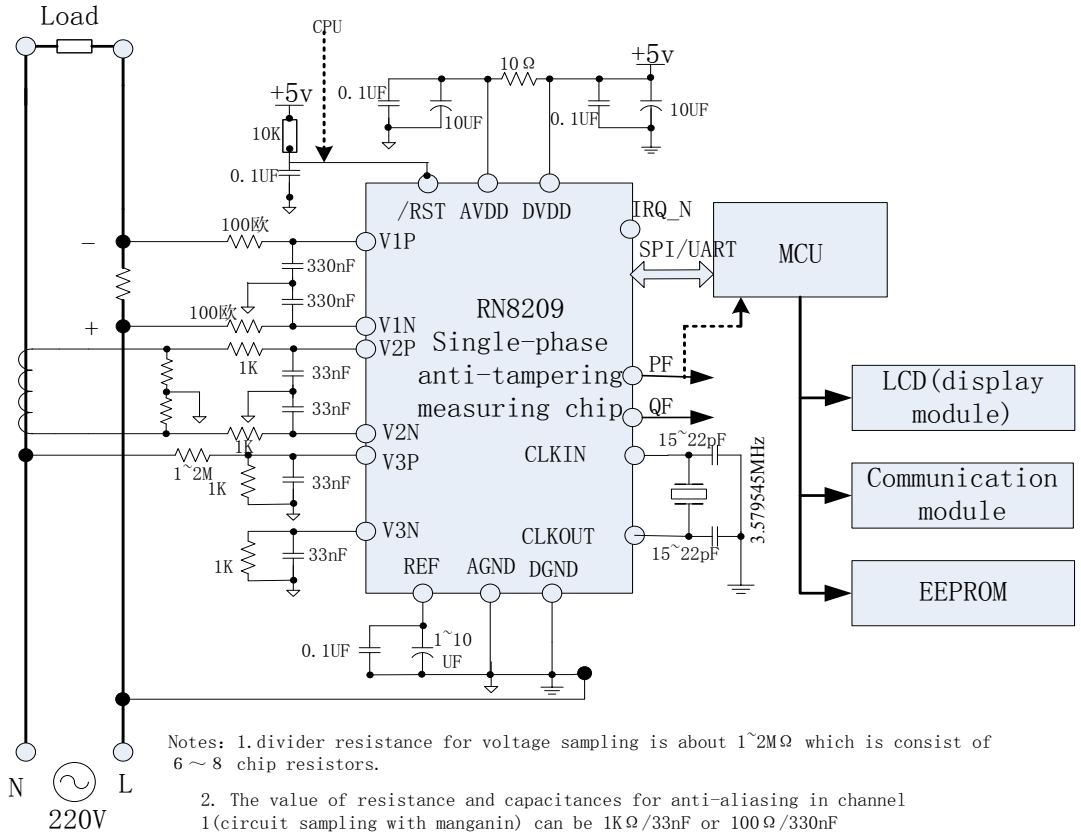


Figure 1-4 Typical Application of Single-phase Anti-tampering Meter

2 System Functions

2.1 Power Supply Monitoring

The RN8209 includes an internal power supply monitoring circuit, able to continuously monitor the analog supply (AVDD). When the power supply is lower than 2.6V ± 0.1V, the chip will be reset, and when the supply is higher than 2.75V ± 0.1V, the chip will work normally.

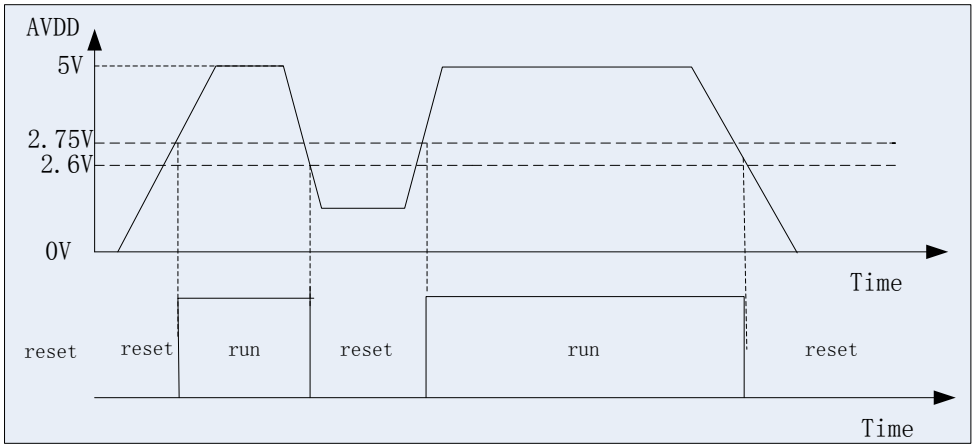


Figure 2-1 Power Detection Features

☐ Normal range of applications: 3V-5.5V, the selected typical supply voltage (eg, 5V or 3.3V), should ensure the power fluctuation within ± 10% range.

2.2 System Reset

RN8209 supports three global reset methods:

- Power ON/OFF
- External pin reset or RX Pin Reset
- Reset command

When any global reset occurs, the register will be restored to its reset initial value, and the external pins will recover to the initial states.

Chip reset will be completed after 15us it received the reset command.

The external reset pin of RN8209D should go from high to low for more than 50us, and then turn to high for 300us to complete reset actions.

The RX pin of RN8209C/D is also a reset pin, when the input signal to this pin is low for more than 20ms, it will be taken as reset command. This feature saves the number of optocouplers in isolated applications. RN8209C/D internal reset circuit and UART communication circuit is completely independent, this pin reset function is exactly the same as individual pin reset.

Suggested RX pin reset operation is: first to keep RX pin low for 25ms, then high for 20ms, and finally start a normal UART communications.

Relevant registers:

In the system status register, RST is a reset sign: when the external RST_N pin or the power-on reset has ended, this bit will be set as 1, cleared after read and can be used as a meter calibration data request after reset.

It is recommended CPU to conduct a reset operation by pin reset or reset command before initializing the measurement chip.

2.3 Analog-digital conversion

RN8209 includes three channels of ADC, respectively used for phase current sampling, neutral current sampling and voltage sampling. The bit of ADC2ON in the system control register is used to turn on/off the current Channel B.

ADC uses a fully differential input. The current and voltage channels have the maximum signal input amplitude at 1000mv of the peak.

By configuring bit5 ~ bit0 in the system control register (SYSCON 0x00H), the gain magnification of the three channels of ADC can be configured separately with 1, 2, 8, and 16 for current channel A, 1, 2, and 4 for current channel B and voltage channel. The current Channel A has its gain magnification as 16 times by default.

2.4 Active Power

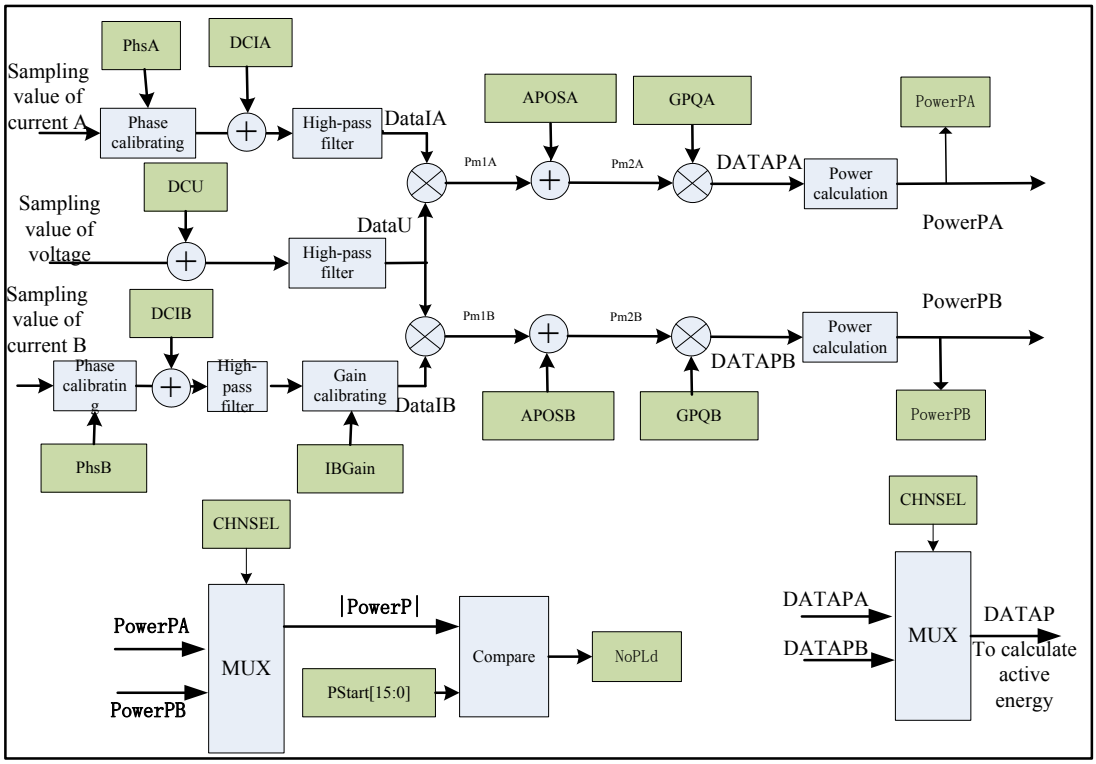


Figure 2-2 Active Power Diagram

RN8209C provides two channels of active power calculation and correction, respectively, the active power calculation and calibration of Current A and voltage, and the active power calculation and calibration of Current B and voltage.

Registers also contain two sets (A / B) of phase calibration, active offset calibration, active gain calibration and average power registers. In addition, in order to ensure the consistency of the two channels, it also provides the gain calibration register IBGain of the current channel B which can affect active power and current effective value of channel B.

The special commands can be used to determine which channels of the average active power (PowerP) currently used to determine the no-load and start status, as well as the instantaneous active power channel (DATAP) currently used to calculate the active energy come from, with the details referring to the section related to special commands.

Users can select and configure the channels by special commands, and the configuration results can be queried by the CHNSEL register bit.

The digital high-pass filter in the diagram is mainly used to remove the DC component in current and voltage sampling data.

The DIA, DIB and DCU in figure are used for ADC channel's DC bias correction. When RN8209C/D is used for DC measurement applications, users should commit DC bias correction and turn off the high-pass filter.

2.5 Reactive Power

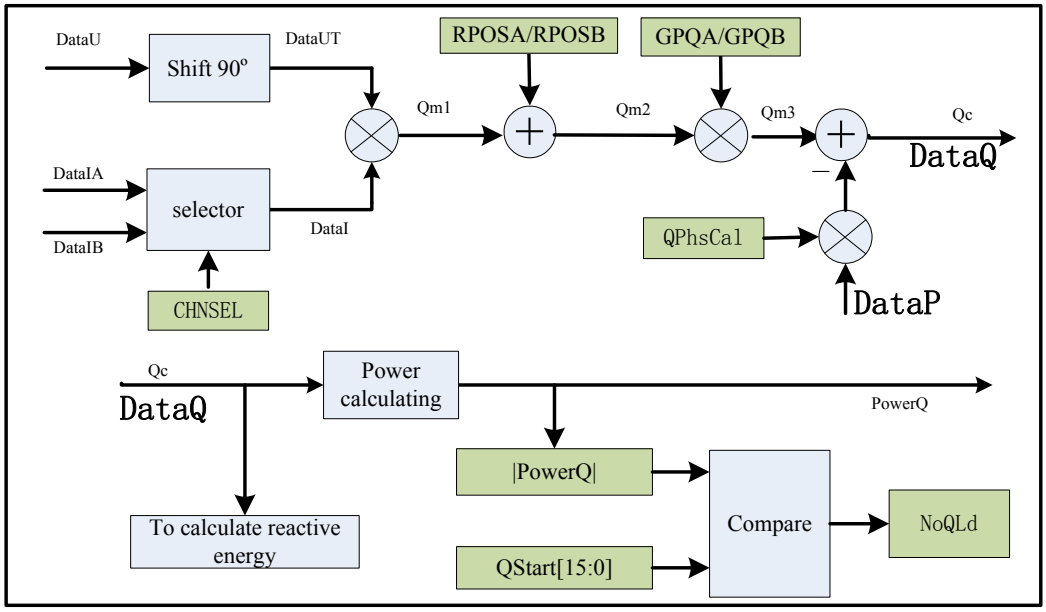


Figure 2-3 Reactive Power Diagram

RN8209 contains a circuit for reactive power measurement. Therein, the DataUT for measurement results from 90 degrees' phase shift of DataU; DataI comes from DataIA or DataIB, which can be configured by special commands, and the configuration results can be queried by the CHNSEL register bit.

2.6 RMS

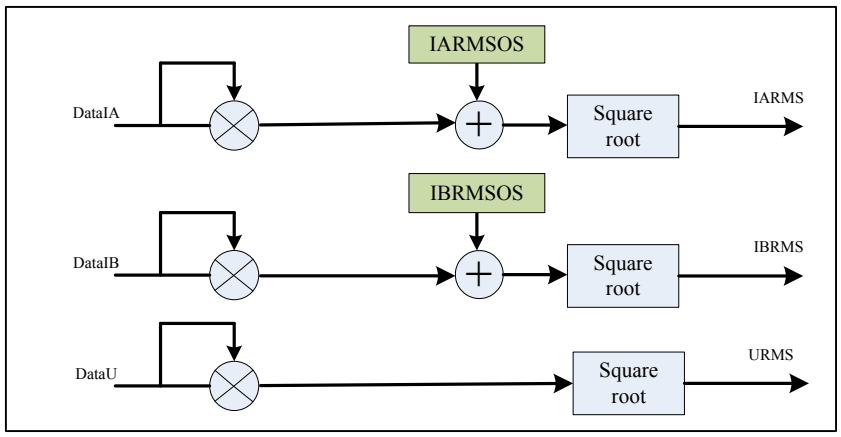


Figure 2-4 RMS Calculation Diagram

RN8209 provides the true RMS parameter output of three channels, including URMS, IARMS and IBRMS. The register length is 24bit, refresh - at 3.495Hz or 13.982Hz. In addition, it also includes two RMS Offset registers: IARMSOS and IBRMSOS.

Note: The gain calibration of channel B (IBGain) will affect the IBRMS output, but phase calibration, power gain calibration and power offset calibration will have no effect on the RMS calculation results.

2.7 Energy Calculation

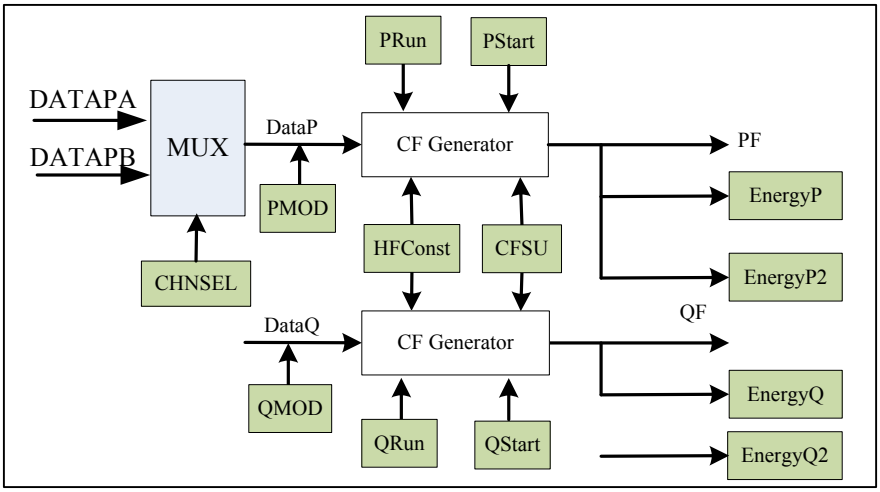


Figure 2-4 Energy Calculation

Energy pulse output:

The pulse output, namely, the meter calibration pulse output, can be directly connected to a standard meter for error comparison.

The PF / QF output meets the following timing relationship:

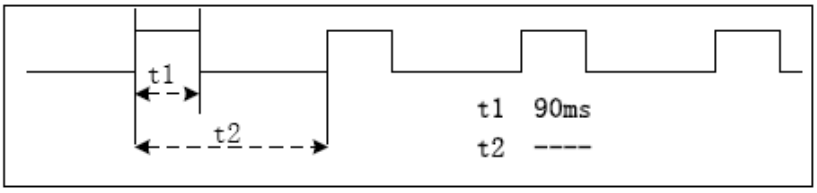


Figure 2-5 The width of output pulse

Note: When the pulse output period is less than 180ms, the pulse will be output in form of equal duty.

PFcnt, HFConst, pulse output and energy registers have the relationship as follows:

When 2*|PFcnt| (0x20H) = HFConst (0x03H), PF has a pulse output. Simultaneously, the energy registers EnergyP (0x29H) and EnergyP2 (0x2AH) will increase 1respectively.

When 2*|QFcnt| (0x21H) = HFConst (0x03H), QF has a pulse output. Simultaneously, the energy registers EnergyQ (0x2BH) and EnergyQ2 (0x2CH) will increase 1 respectively.

Relationship among pulse output, energy register, PRun / QRun and PStart / QStart:

Active / reactive energy registers and PF / QF output are also controlled by PRun / QRun and PStart / QStart.

- When PRun = 0 or |P| is less than PStart, PF does not output any pulse; PFcnt and active registers will not be increased.
- When QRun = 0 or |Q| is less than QStart, QF does not output any pulse; QFcnt and reactive energy registers will not be increased.

Custom pulse output:

The default source of DataD is DataD DATAQ (reactive power), you can set it's source to DATAPA (the active power of channel 2), DATAPA + DATAPB (the vecor sum of the active power of the two channels), D2FP (defined by user) by register D2FM.

Pulse output speedup:

To speed up the calibration of small-signal, it provides the function of pulse output speedup. While correcting small signals, you can configure **CFSUEN** and **CFSU [1:0]** bits of the EMUCON (0x01H) register, so that the PF / QF output frequency could be increased, by 16 times at most.

Indicating of negative power:

When the active or reactive power is negative, the EMUStatus register will have its REVP bit or REVQ bit changed to 1, with REVP bit and PF pulse, as well as REVQ bit and QF pulse synchronously refreshed.

2.8 Channel Switch

RN8209 specially provides one channel of ADC used for measurement of neutral current RMS and active power, and provides the function to switch the phase current and neutral current channels for users to choose which current they like to measure the active energy.

The current channels can be switched by special commands, with the details referring to the section for special command registers. The configuration results can be queried by the register bit CHNSEL.

2.9 Frequency Measurement

RN8209 can directly output line frequency parameter (UFreq 0x25H 2 bytes lenth), measurement of fundamental frequency and measurement bandwidth of 250Hz。The minimum measuring frequency is 6.8Hz.

2.10 Zero-crossing Detection

Configure ZXCFG (EMUCON.7) of RN8209D to enable/disable zero-crossing output of pin IRQ_N / ZX .

Configure ZXD1 (EMUCON.9) and ZXD0 (EMUCON.8) register bits of RN8209D to select four kinds of zero-crossing output.

2.11 Interrupt

The interrupt of RN8209D includes an interrupt enable register IE, 2 interrupt status register IF and RIF, a multiplex interrupt request pin IRQ_N / ZX. Wherein, RIF is associated with IF, for example when reading RIF can clear IF, or vice versa.

1. The interrupt request signal IRQ_N

IRQ_ N / ZX pin is a multiplexing pin of IRQ and zero-crossing detection output ZX, which can be configured by the ZXCFG bit of EMUCON register (0x01H).

.

When the corresponding interrupt bits of the interrupt enable register is enabled and the corresponding interrupt events occur, the IRQ_N pin will output low level, and it will turn to high level until the falling edge of SCLK of the last bit (LSB) of the command which was send by CPU through SPI interface to read RIF or IF.

2.Interrupt Processing

Hardware:

- The IRQ_N of RN8209D is usually connected to the MCU external interrupt pin /INT, and when IRQ_N is changing from high to low, the MCU will generate the /INT interrupt.
- The MCU serves as a SPI or UART Host, while RN8209D as an SPI or UART slave.

Interrupt handler:

Step 1: MCU interrupt initialization

1. The MCU reads RN8209D RIF to clear IF and RIF interrupt flags;

2 Configure RN8209D IE register to enable the necessary interrupt permit bit to generate IRQ_N;

3. The MCU enables the / INT external interrupt to wait for RN8209D interrupt event occurring. The IRQ_N output triggers the / INT interrupt, and jump into the /INT interrupt entry address.

Step 2: MCU interrupt service procedure

1 Close MCU global interrupt and /INT interrupt;

2. The MCU reads RIF register via the SPI to clear the IF and RIF registers and to make sure the IRQ_N back to a high level.

3. The MCU determines RN8209D interrupt source by the RIF interrupt flag, and then execute the corresponding interrupt handler.

4. After the interrupt handler has been executed, the MCU will enable the global interrupt and /INT interrupt again, and back to normal program after it have restored the status of CPU registers.

After interrupt return, if any /INT interrupt flag is detected, the program will enter the external interrupt ISR, and repeat 2. If no /INT interrupt flag is detected, it indicates that there is no interrupt event occurring in interrupt processing, and the program will continue

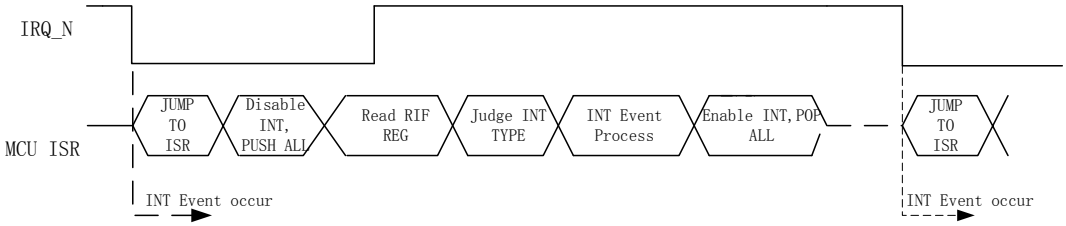


Figure 2-6 RN8209D Interrupt Processing

2.12 Register

2.12.1 List of Registers

Table 2-3 List of RN8209 Registers

Address	Name	R/W	Length	Reset Value	Descriptions
Calibration Parameter and Measurement Control Registers					
00H	SYSCON	R/W	2	0003h	System control register, write-protect
01H	EMUCON	R/W	2	0003h	Energy measure control register, write-protect
02H	HFConst	R/W	2	1000h	High frequency impulse const register, write-protect
03H	PStart	R/W	2	0060h	Active power start threshold setup register, write-protect
04H	QStart	R/W	2	0120h	Reactive power start threshold setup register, write-protect
05H	GPQA	R/W	2	0000h	Channel A power gain register, write-protect

06H	GPQB	R/W	2	0000h	Channel B power gain register, write-protect
07H	PhsA	R/W	1	00h	Channel A phase calibration register, write-protect
08H	PhsB	R/W	1	00h	Channel B phase calibration register, write-protect
09H	QPhsCal	R/W	2	0000h	Reactive power phase calibration, write-protect
0AH	APOSA	R/W	2	0000h	Channel A active power offset register, write-protect
0BH	APOSB	R/W	2	0000h	Channel B active power offset register, write-protect
0CH	RPOSA	R/W	2	0000h	Channel A reactive power offset register, write-protect
0DH	RPOSB	R/W	2	0000h	Channel B reactive power offset register, write-protect
0EH	IARMSOS	R/W	2	0000h	Current Channel A RMS offset calibration, write-protect
0FH	IBRMSOS	R/W	2	0000h	Current Channel B RMS offset calibration, write-protect
10H	IBGain	R/W	2	0000h	Current Channel B gain setting, write-protect
11H	D2FPL	R/W	2	0000h	The low 16 bits of custom power register D2FP, write protection
12H	D2FPH	R/W	2	0000h	The high 16 bits of custom power register D2FP, you need to write D2FPH firstly, then write D2FPL, to enable electric energy integration of D2FP only, write-protected.
13H	DCIAH	R/W	2	0000h	The high 16 bits of IA channel DC offset correction register, write protection
14H	DCIBH	R/W	2	0000h	The high 16 bits of IB channel DC offset correction register, write protection
15H	DCUH	R/W	2	0000h	The high 16 bits of U-channel DC offset correction register, write protection
16H	DCL	R/W	2	0000h	The low 4 bits of the three DC offset correction registers: DC [11: 0] = {DCU [3: 0], DCIBL [3: 0], DCIAL [3: 0]}, write protection
17H	EMUCON2	R/W	2	0000h	Metering control register 2, write-protected
Measurement Parameter and Status Registers					
20H	PFCnt	R/W	2	0000h	Active energy counter register, write-protect
21H	DFCnt	R/W	2	0000h	Custom energy counter register, write-protect
22H	IARMS	R	3	000000h	Current A RMS
23H	IBRMS	R	3	000000h	Current B RMS
24H	URMS	R	3	000000h	Voltage RMS
25H	UFreq	R	2	0000h	Voltage frequency

26H	PowerPA	R	4	00000000h	Active Power A
27H	PowerPB	R	4	00000000h	Active Power B
28H	PowerQ	R	4	00000000h	Reactive power
29H	EnergyP	R	3	000000h	Active energy, configurable for being cleared or not after read by EnergyCLR register, with defaulf of being not cleared after read.
2AH	EnergyP2	R	3	000000h	Active energy, configurable for register being cleared after read or freezing register, with defaulf of being cleared after read.
2BH	EnergyD	R	3	000000h	Reactive energy or user-defined energy, configurable for register being cleared or not after read, with register being not cleared after read as default which is controlled by the bit of EnergyCLR register.
2CH	EnergyD2	R	3	000000h	Reactive energy or user-defined energy, configurable for register being cleared after read or freezing register, with register being cleared after read as default
2DH	EMUStatus	R	3	00EE79h	Energy measurement status and checksum register
30H	SPL_IA	R	3	000000h	Sample value of IA channel ADC
31H	SPL_IB	R	3	000000h	Sample value of IB channel ADC
32H	SPL_U	R	3	000000h	Sample value of U channel ADC
35H	UFreq2	R	3	000000h	Voltage frequency register 2 with extended range of frequency measurement, it will output the same value with UFreq(0x25H) when the frequency is 50Hz on voltage channel.
Interrupt Registers					
40H	IE	R/W	1	00h	Interrupt enable register, write-protect
41H	IF	R	1	00h	Interrupt flag register, cleared after read
42H	RIF	R	1	00h	Reset interrupt flag register, cleared after read
System Status Registers					
43H	SysStatus	R	1	--	System status register
44H	RData	R	4	--	Previous SPI /UART data read out
45H	WData	R	2	--	Previous SPI /UART data written
7FH	DeviceID	R	3	820900h	RN8209 Device ID

2.12.2 Calibration parameter registers

System control registers

SYSTEM Control Register (SYSCON) Address: 0x00 H Default Value: 0003H

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Descriptions</th></tr>
<tr><td>15</td><td>Reserved</td><td>The default value is 0, do not write 1 to this bit</td></tr>
<tr><td>14-8</td><td>Uartbr[6:0]</td><td>UART baud rate selection, read-only, and its value is determined by the hardware pin B1 and B0..
{B1, B0} = 00, Uadrbr = 7'h2E, 2400 baud
{B1, B0} = 01, Uadrbr = 7'h16, 4800 baud
{B1, B0} = 10, Uadrbr = 7'h0B, 9600 baud
{B1, B0} = 11, Uadrbr = 7'h05, 19200 baud
It only makes sense when the UART is selected as the communication interface, and when SPI is selected, it will be 0.
Note: The uartbr[6:0] will be added in the checksum calculation, so that it will influce the result of the checksum when the UART is chosen as the communication interface. The baudrate of RN8209C is fixed at 4800.</td></tr>
<tr><td>7</td><td>Reserved</td><td>The default value is 0, do not write 1 to this bit</td></tr>
<tr><td>6</td><td>ADC2ON</td><td>ADC2ON = 1: indicates that ADC Current Channel B is on; = 0: ADC Current Channel B closed, ADC output is fixed to 0.</td></tr>
<tr><td>5-4</td><td>PGAIB[1:0]</td><td>Analog gain selection of current Channel B
<table>
<tr><th>PGAIB1</th><th>PGAIB0</th><th>current channel B</th></tr>
<tr><td>0</td><td>0</td><td>PGA=1</td></tr>
<tr><td>0</td><td>1</td><td>PGA=2</td></tr>
<tr><td>1</td><td>0</td><td>PGA=4</td></tr>
<tr><td></td><td>1</td><td>PGA=4</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>PGAU[1:0]</td><td>Voltage channel analog gain selection
<table>
<tr><th>PGAU1</th><th>PGAU0</th><th>voltage channel</th></tr>
<tr><td>0</td><td>0</td><td>PGA=1</td></tr>
<tr><td>0</td><td>1</td><td>PGA=2</td></tr>
<tr><td>1</td><td>0</td><td>PGA=4</td></tr>
<tr><td>1</td><td>1</td><td>PGA=4</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>PGAIA[1:0]</td><td>Current Channel A analog gain selection, 16 times by default.
<table>
<tr><th>PGAIA1</th><th>PGAIA0</th><th>current channel A</th></tr>
<tr><td>0</td><td>0</td><td>PGA=1</td></tr>
<tr><td>0</td><td>1</td><td>PGA=2</td></tr>
<tr><td>1</td><td>0</td><td>PGA=8</td></tr>
<tr><td>1</td><td>1</td><td>PGA=16</td></tr>
</table></td></tr>
</table>

Measurement Control Registers

Measurement control registers are used for settings of energy measurement functions.

<table>
<tr><th colspan="3">Energy Measure Control Register (EMUCON) Address: 0x01 H Default Value: 0003H</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Descriptions</th></tr>
<tr><td>15</td><td>EnergyCLR</td><td>The default value is 0
= 0: 29 / 2B-accumulated energy registers;
= 1: 29 / 2B energy register is cleared after read;</td></tr>
</table>

<table>
<tr><td>14</td><td>HPFIBOFF</td><td>HPFIBOFF = 0: Enable the digital high-pass filter of IB channel
HPFIBOFF = 1: Disable the digital high-pass filter of IB channel</td></tr>
<tr><td>13-12</td><td>QMOD[1:0]</td><td>Custom energy accumulation mode selection:
<table>
<tr><td>QMOD1</td><td>QMOD0</td><td>Accumulative power Qm</td></tr>
<tr><td>0</td><td>0</td><td>If Qm = DataQ, the positive and negative power will be involved in accumulation, and the negative power will have an REVQ symbol.</td></tr>
<tr><td>0</td><td>1</td><td>Only positive power is accumulated.</td></tr>
<tr><td>1</td><td>0</td><td>If Qm=|DataQ|, the positive and negative power will be involved in accumulation, and the negative power will have no REVQ symbol.</td></tr>
<tr><td>1</td><td>1</td><td>Qm = DataQ (reserved)</td></tr>
</table></td></tr>
<tr><td>11-10</td><td>PMOD[1:0]</td><td>Active energy accumulation mode selection: same as the reactive energy accumulation in the table above.</td></tr>
<tr><td>9</td><td>ZXD1</td><td>The ZX output initial value is 0, and different waveforms will be output according to ZXD1 and ZXD0 configuration:
When ZXD1 = 0, it means that only at the selected zero-crossing, the ZX output changes;
When ZXD1 = 1, it means that at the positive and negative zero-crossing points, the ZX outputs changes.</td></tr>
<tr><td>8</td><td>ZXD0</td><td>When ZXD0 = 0, it means that the positive zero-crossing point is selected as a zero-crossing detection signal;
When ZXD0 = 1, it means that the negative zero-crossing point is selected as a zero-crossing detection signal;</td></tr>
<tr><td>7</td><td>ZXCFG</td><td>ZXCFG = 0: the pin IRQ_N / ZX / SIG serves as IRQ_N.
ZXCFG = 1: the pin IRQ_N / ZX / SIG serves as ZX.</td></tr>
<tr><td>6</td><td>HPFIOFF</td><td>HPFIOFF = 0: Enable IA channel digital high-pass filters
HPFIOFF = 1: Disable IA channel digital high-pass filters</td></tr>
<tr><td>5</td><td>HPFUOFF</td><td>HPFUOFF = 0: Enable U-channel digital high-pass filters
HPFUOFF = 1: Disable U-channel digital high-pass filters</td></tr>
<tr><td>4</td><td>CFSUEN</td><td>CFSUEN is the control bit of the PF / QF pulse output acceleration module. When CFSUEN = 1, the pulse acceleration module will be enabled, and the pulse output rate will be increased by 2^ (CFSU [1:0] +1) times. When CFSUEN = 0, the pulse acceleration module will be disabled, and the pulse will have normal output.</td></tr>
<tr><td>3,2</td><td>CFSU[1:0]</td><td>This bit will work with the help of CFSUEN. See CFSUEN instructions.</td></tr>
<tr><td>1</td><td>DRUN</td><td>When QRUN = 1, enable the QF pulse output and custom energy register accumulation;
When QRUN = 0, disable the QF pulse output and custom energy register accumulation, with the default of 1.</td></tr>
<tr><td>0</td><td>PRUN</td><td>When PRUN = 1, enable the PF pulse output and active energy register accumulation;
When PRUN = 0, disable the PF pulse output and active energy register accumulation, with the default of 1.</td></tr>
</table>

Pulse frequency registers

High Frequency Impulse Const Register (HFConst)				Address: 0x 02H Default Value : 1000H				
	Bit15	14	13	12	11	10	9	Bit8
Read:	HFC15	HFC14	HFC13	HFC12	HFC11	HFC10	HFC9	HFC8
Write:								
Reset:	0	0	0	1	0	0	0	0
:	Bit7	6	5	4	3	2	1	Bit0
Read	HFC7	HFC6	HFC5	HFC4	HFC3	HFC2	HFC1	HFC0
Write:								
Reset:	0	0	0	0	0	0	0	0

HFConst is a 16-bit unsigned number, it should be compared with 2 times of the absolute value of the fast pulse counter register PFCNT / DFCNT register value. If the result is greater than or equal to the HFConst, then there will be corresponding PF / QF pulse output.

No-load and start threshold registers

Start Power Threshold Setup Register (PStart)				Address: 0x 03h Default Value : 0060H				
	Bit15	14	13	12	11	10	9	Bit8
Read:	PS15	PS 14	PS 13	PS 12	PS11	PS10	PS 9	PS 8
Write:								
Reset:	0	0	0	0	0	0	0	0
	Bit7	6	5	4	3	2	1	Bit0
Read:	PS7	PS 6	PS 5	PS 4	PS 3	PS 2	PS 1	PS 0
Write:								
Reset:	0	1	1	0	0	0	0	0

Start Power Threshold Setup Register (DStart)				Address: 0x 04h Default Value : 0120H				
	Bit15	14	13	12	11	10	9	Bit8
Read:	QS15	QS 14	QS 13	QS 12	QS11	QS10	QS 9	QS 8
Write:								
Reset:	0	0	0	0	0	0	0	1
	Bit7	6	5	4	3	2	1	Bit0
Read:	QS7	QS 6	QS 5	QS 4	QS 3	QS 2	QS 1	QS 0
Write:								
Reset:	0	0	1	0	0	0	0	0

The start threshold can be configured by PStart and QStart registers. They are 16-bit unsigned numbers, and when compared, they should be compared with the high 24-bit absolute value of PowerP and DataD (a 32-bit signed number) to judge the start status.

When |PowerP| is smaller than PStart, PF does not output any pulse.

When |DataD| is smaller than DStart, QF does not output any pulse.

Gain calibration register

Power Gain Register A(GPQA)			Address: 0x05h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GPQA_15	GPQA_14	GPQA_13	GPQA_12…GPQA_3	GPQA_2	GPQA_1	GPQA_0
Write:							
Reset:	0	0	0	0	0	0	0

Power Gain Register B(GPQB)			Address: 0x06h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GPQB_15	GPQB_14	GPQB_13	GPQB_12…GPQB_3	GPQB_2	GPQB_1	GPQB_0
Write:							
Reset:	0	0	0	0	0	0	0

Two registers are included: GPQA and GPQB (in a binary complement format), and the MSB is a symbol bit.

GPQA is used for active power calibration of the current Channel A and the voltage channel. GPQB is used for active gain calibration of the current Channel B and the voltage channel.

Correction formula: P1 = P0 (1 + GPQS)

Q1 = Q0 (1 + GPQS)

Where, GPQS is the normalized value of gain correction register. See Chapter III Calibration Method for its usage.

Phase calibration register

Phase Calibration Register A(PhsA)			Address: 0x 07H Default Value : 00H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PhsA_7	PhsA_6	PhsA _5	PhsA _4	PhsA _3	PhsA _2	PhsA _1	PhsA _0
Write:								
Reset:	0	0	0	0	0	0	0	0

Phase Calibration Register B(PhsB)			Address: 0x08 H Default Value : 00H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	PhsB _7	PhsB _6	PhsB _5	PhsB _4	PhsB _3	PhsB _2	PhsB _1	PhsB _0
Write:								
Reset:	0	0	0	0	0	0	0	0

IA and U-channel phase calibration PhsA and IB and U-channel phase calibration PhsB are included. Such two registers are both signed binary complement codes, with Bit0 ~bit7 valid, in which bit7 is the sign bit. Refer to Chapter III Calibration Method for detailed use.

1 LSB represents the delay of 1/895 kHz = 1.12us/LSB, and under 50HZ, 1 LSB represents 1.12 us * 360 ° * 50 / 10 ^ 6 = 0.02° /LSB phase calibration.

Phase calibration range: at 50HZ, ± 2.56 °

Note: The accuracy of phase correction can be improved to 0.01^{o} by two bits of metering control register 2 (EMUCON2 Address: 0x17H).

Reactive power phase calibration register

Reactive Power Phase Calibration Register (QPhsCal)				Address: 09H Default Value : 0000H				
	Bit15	14	13	12..3		2	1	Bit0
Read: / Write:	QPC15	QPC14	QPC13	QPC12.. QPC3		QPC2	QPC1	QPC0
Reset:	0	0	0	0	0	0	0	0

Reactive power phase calibration register is used for phase calibration of U-channel 90° phase-shift filter in the reactive calculation. Reactive power phase calibration register adopts a 16-bit binary complement form, and the MSB is a sign bit. Refer to Chapter III Calibration Method for detailed use.

Calibration formula: Q2 = Q1-QPhs * P1

Where, P1 is active power, Q1 is reactive power before calibration, and Q2 is reactive power after calibration.

Active Power Offset Calibration Registers

Active Power Offset Register A(APOSA)			Address: 0AH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSA_ 15	APOSA _14	APOSA _13	APOSA _12…APOSA _3	APOSA _2	APOSA _1	APOSA _0
Reset:	0	0	0	0	0	0	0

Active Power Offset Register B(APOSB)			Address: 0BH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSB_15	APOSB _14	APOSB _13	APOSB _12…APOSB _3	APOSB _2	APOSB _1	APOSB _0
Reset:	0	0	0	0	0	0	0

Active power offset calibration registers apply to accurate calibration of small signals. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III Calibration Method for detailed use.

The APOSA register is the Offset value of the current channel-A and U active power.

The APOSB register is the Offset value of the current channel-B and U active power.

Reactive Power Offset Calibration Register

Rective Power Offset Register (RPOSA)			Address: 0CH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0

Read: / Write:	RPOSA_15	RPOSA _14	RPOSA _13	RPOSA _12…RPOSA _3	RPOSA _2	RPOSA _1	RPOSA _0
Reset:	0	0	0	0	0	0	0

Rective Power Offset Register (RPOSB)			Address: 0DH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	RPOSB_ 15	RPOSB _14	RPOSB _13	RPOSB _12…RPOSB _3	RPOSB _2	RPOSB _1	RPOSB _0
Reset:	0	0	0	0	0	0	0

Reactive power offset calibration register applies to accurate calibration of small reactive signals. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III Calibration Method for detailed use.

The RPOSA register is the Offset value of the current channel-A and U reactive power. The PPOSB register is the Offset value of the current channel-B and U reactive power.

RMS Offset Calibration Registers

IA RMS Offset Register(IARMSOS)			Address: 0EH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	IARMS_15	IARMS _14	IARMS _13	IARMS _12…IARMS _3	IARMS _2	IARMS _1	IARMS _0
Reset:	0	0	0	0	0	0	0

IB RMS Offset Register(IBRMSOS)			Address: 0FH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	IBRMS_15	IBRMS _14	IBRMS _13	IBRMS _12…IBRMS _3	IBRMS _2	IBRMS _1	IBRMS _0
Reset:	0	0	0	0	0	0	0

RMS Offset calibration registers apply to accurate calibration of small signal of current RMS. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III Calibration Method for detailed use.

The IARMSOS register is the RMS Offset value of Current A. The IBRMSOS register is the RMS Offset value of Current B.

Current B Gain Settings

Current B Gain Register (IBGain)			Address: 10H Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	IBG15	IBG14	IBG13	IBG12…IBG3	IBG2	IBG1	IBG0

Write:							
Reset:	0	0	0	0	0	0	0

Current B gain setting registers are used for consistency calibration of the two current channels in the anti-tampering meter. The consistency calibration is to be completed at 100% Ib point. Refer to Chapter III Calibration Method for detailed use.

Channel B current gain register adopts a binary complement format with the MSB of a symbol bit within (-1, +1).

If IBGain> = 2 ^ 15, then GainI2 = (IBGain-2 ^ 16) / 2 ^ 15

Otherwise, GainI2 = IBGain / 2 ^ 15

I2a (before calibration) and I2b (after adjustment) will have the following relationship: I2b = I2a + I2a * GainI2

Custom Power Register

Custom power register is a 32-bit signed number which is composed of high 16-bit D2FPH (0x12H) and low 16-bit D2FPL (0x11H). The MSB of D2FPH is the sign bit.

If D2FM register (EMUCON2 of bit5 ~ 4) is configured as a custom power, the custom power register of RN8209 will be integrated automatically according to the pulse constant, as soon as it is set by user, and the integral result energy is stored in EnergyD (0x2BH) and EnergyD2 (0x2CH), and the pulse will be output at QF pin.

Users need to write D2FPH firstly, then D2FPL, to make sure that D2FP to take effect.

DC-offset correction register

There are three channel DC-offset correction registers in RN8209 used when high-pass filter is disabled, each one is a 20-bit register. Refer RN8209 application notes for the method of DC offset correction.

Metering control register 2

Energy Measure Control Register2 (EMUCON2) Address: 0x17 H Default Value: 0000H		
Bit	Bit Name	Descriptions
15~14	reserved	The default value is 0, do not write 1 to this bit
13,12	FreqCnt	=00:the period for frequency measuring is 32 cycles =01: the period for frequency measuring is 4 cycles; =10: the period for frequency measuring is 8 cycles; =11: the period for frequency measuring is 16 cycles;
11,10	reserved	The default value is 0
9	PhsB0	It can served as the last bit of phase correction register with PhsB(0x08H) register, to improve the accuracy of phase correction to 0.01degree from 0.02degree. It will have no effect, when it is 0,
8	PhsA0	It can served as the last bit of phase correction register with PhsA(0x07H) register, to improve the accuracy of phase correction to 0.01degree from 0.02degree. It will have no effect, when it is 0,
7	**UPMODE**	**=0，refreshing time of power or RMS register is 3.495Hz;** **=1，refreshing time of power or RMS register is 13.982Hz;**
6	ZXMODE	=0，the source of zero-cross signal is normal voltage signal for measuring with harmonic components =1，the source of zero-cross signal is the voltage signal after low-pass filter.
5,4	D2FM[1:0]	=00: set the reactive power for custom energy =01: set the vector sum of the active power of channel A and B for custom energy =10: set the custom power register D2FP for custom energy

		=11: set the active power of channel B for custom energy
3	Energy_fz	=0，disable the freezing function of energy register 2, and it is cleared after read by default. =1，enable the freezing function of energy register 2(address 29 and 2B),then the value of energy register 1 will be loaded to energy register 2 per 572.1397ms(2048*1024 cycles of the crystal oscillator) while the energy register 1 is cleared at the same time.
2~0	reserved	The default value is 0, do not write 1 to this bit

2.12.3 Measurement parameter registers

Fast pulse counter

Active Energy Counter Register (PFCNT)				Address: 0x20h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	PFC15	PFC14	PFC13	PFC12…PFC3	PFC2	PFC1	PFC0
Reset:	0	0	0	0	0	0	0

Reactive Energy Counter Register (QFCNT)				Address：0x21h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	QFC15	QFC14	QFC13	QFC12…QFC3	QFC2	QFC1	QFC0
Reset:	0	0	0	0	0	0	0

In order to prevent energy loss when power on and off, the MCU will read and save the register PFCnt / QFCnt values in case of power-fall, and then the MCU will re-write such values into PFCnt / QFCnt when later power-on.

When 2 times of the absolute value of the fast pulse counter register PFCnt/DFCnt is greater than or equal to HFconst, the corresponding PF / QF will output pulse, and the energy register will have its value plus 1 accordingly.

Current and Voltage RMS Registers

Current A Rms Register (IARms)				Address： 0x22h			
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IAS23	IAS22	IAS21	IAS20…IAS3	IAS2	IAS1	IAS0

Current B Rms Register (IBRms)				Address： 0x23h			
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IBS23	IBS22	IBS21	IBS20…IBS3	IBS2	IBS1	IBS0

Voltage Rms Register (Urms)				Address： 0x24h			
	Bit23	22	21	20 … 3	2	1	Bit0

Read:	US23	US22	US21	US20…US3	US2	US1	US0

Rms is a 24-bit signed number, the MSB = 0 indicates valid data, and the MSB = 1 indicates that the reading is treated as zero; the parameter refresh frequency will be 3.4Hz or 13.982Hz.

Voltage Frequency Register

Voltage Frequency Register (UFreq)			Address： 0x25h				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	Ufreq15	Ufreq14	Ufreq13	Ufreq12…Ufreq3	Ufreq2	Ufreq1	Ufreq0

It will mainly measure the fundamental frequency, with the measurement bandwidth of 250Hz or so.

The frequency value is a 16-bit unsigned number, with the parameter formatting formula as follows:

f=CLKIN/8/UFREQ

For example, if the system clock CLKIN = 3.579545MHz, UFREQ = 8948, then the actual frequency measured should be:

f=3579545/8/8948=49.9908Hz。

The default update period of the voltage frequency is 0.64s which can be configured by measuring control register 2.

It also includes a voltage register 2 UFreq2 which address is 0x35H with 3 bytes length and can measure the fundamental frequency with range of 250Hz and minimal measuring frequency of 1Hz. When the voltage frequency is 50Hz, it will be read as the same as UFreq(0x25H).

Average active power register

Active Power Register (PowerPA)			Address： 0x26h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APA23	APA22	APA21	APA20…APA3	APA2	APA1	APA0

Active Power Register (PowerPB)			Address： 0x27h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APB23	APB22	APB21	APB20…APB3	APB2	APB1	APB0

The active parameter PowerP is a 32-bit number in a binary complement format, with the MSB of a symbol bit. The power parameter has its refresh frequency of 3.4Hz or 13.982Hz optionally.

POWERPA is the average active power register of Channel U and Channel IA, while POWERPB is the average active power register of Channel U and Channel IB.

Average reactive power register

Reactive Power Register (PowerQ)			Address： 0x28h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	RP23	RP22	RP21	RP20…RP3	RP2	RP1	RP0

The reactive parameter PowerQ is a 32-bit number in a binary complement format, with the MSB of a symbol bit. Its refresh frequency is the same as PowerPA and PowerPB.

This register results from reactive power calculation of Channel U and user-selected current channel, and Channel A shall be selected by default.

Active energy register

Active Energy Register (EnergyP)			Address： 0x29h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

EnergyP register is an accumulative active energy register by default. If selected as an accumulative register (bit 15 of EMUCON register = 0), the overflow flag POIF(see IF 0x41H) will be set when it's value go from 0xFFFFFF to 0x000000, on the contrary(bit 15 of EMUCON register = 1) it will be cleared to 0 after read.

Energy parameters is unsigned numbers, register values of EnergyP represent respectively the number of accumulated pulses at PF pin. Energy register for the smallest unit represents 1 / EC kWh. Where the EC is meter constant.

Active Energy Register 2

Active Energy Register2 (EnergyP2)			Address： 0x2AH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

When the energy_fz bit of metering control registers is 0, this register is an active energy register which will be cleared after read. When 1, it will enable freezing function to load the value of active energy register (address 29) to this register per 572.1397ms (2048*1024 cycles of the crystal oscillator) while the active energy register is cleared at the same time.

Reactive or custom energy register

REActive Energy Register (EnergyQ)			Address： 0x2BH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

EnergyD register is an accumulative active energy register by default. If selected as an accumulative register (bit 15 of EMUCON register = 0), the overflow flag QOIF(see IF 0x41H) will be set when it's value go from 0xFFFFFF to 0x000000, on the contrary(bit 15 of EMUCON register = 1) it will be cleared to 0 after read.

Energy parameters is unsigned numbers, register values of EnergyD represent respectively the number of accumulated pulses at QF pin. Energy register for the smallest unit represents 1 / EC kWh. Where the EC is meter constant.

EnergyD is a reactive energy register by default which can be configured by EMUCON2 register.

Reactive or Custom Energy Register 2

REActive Energy Register2 (EnergyQ2)			Address： 0x2CH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

When the energy_fz bit of metering control registers is 0, this register is an custom energy register which will be cleared after read. When 1, it will enable freezing function to load the value of custom energy register (address 2B) to this register per 572.1397ms (2048*1024 cycles of the crystal oscillator) while the custom energy register is cleared at the same time.

EMU Status Registers

The EMU status registers include measurement status registers and checksum registers.

EMU STATUS Register (EMUStatus) Address：0x2D h read-only register		
Bit	Bit Name	Descriptions of Functions
23	Reserved	read as 0.
22	VREFLOW	Read-only register, to indicate the status of VREF = 1, VREF pin voltage is too low, the external circuit is abnormal; = 0, voltage at REFV pin is normal.
21	CHNSEL	Status sign bit for current channel selection: = 1 indicates that the current channel currently used to calculate the active power is Channel B; = 0 indicates that the current channel currently used to calculate the active power is Channel A. This bit is 0 by default, and indicate that Channel A is used to measure the energy.
20	Noqld	When custom power is less than the starting power, Noqld is set as 1; when custom power is greater than / equal to the starting power, Noqld is reset.
19	Nopld	When active power is less than the starting power, NoPld is set as 1; when active power is greater than / equal to the starting power, NoPLd is reset.
18	REVQ	Indication and identification signal of inverse custom power - When negative power is detected, this signal is 1. When positive power is detected again, this signal is 0. This value will be updated when QF outputs pulse.
17	REVP	Indication and identification signal of inverse active power - When negative active power is detected, this signal is 1. When positive reactive power is detected again, this signal is 0. This value will be updated when PF outputs pulse.
16	ChksumBusy	Status of the calculation of checksum of calibration data registers ChksumBusy = 0 indicates that the calculation of checksum of calibration data registers has been completed. The checksum value is available. ChksumBusy = 1 indicates that the calculation of checksum of calibration data registers has not been completed. The checksum value is not available.
15:0	Chksum	Checksum value

EMUStatus [15:0] is a register specifically provided by RN8209 to store the 16-bit checksum of calibration parameter configuration registers, and the external MCU can detect this register to monitor whether the calibration data is confused.

The checksum is calculated with double-byte accumulation then inversed. For the single-byte register PHSA / PHSB, it should be accumulated after extended to be a double byte, and the extended byte should be 00H.

The addresses of registers which should participate the calculation of checksum are 00H-17H. When SPI communication interface is set, the default checksum of the RN8209D is 0xEE79. When UART communication interface is set, the high bits (read only) will participate the calculation of

checksum, and the default checksum value is 0xC079 while the baudrate is 2400, and 0xD879 for 4800, 0xE379 for 9600, 0xE979 for 19200.

The default checksum value of RN8209C is 0xD879.

Given the following three cases, re-start a checksum calculation: the system is reset, any registers with address 00H-17H has WRITE operations, and EMUStatus register has READ operations. One time of checksum calculation needs 11.2us.

2.12.4 Interrupt Register

Interrupt configuration and enable register

This register applies to SPI and UART. When the interrupt enable bit is configured as 1 and the interrupt occurs, the IRQ_N pin will output a low level. Write-protect register – Before configuration of this register, the write enable needs to be opened.

Interrupt Enable Register (IE) Address: 0x40H default: 0x00H readable and writable		
Bit	Bit Name	Descriptions of Functions
7	Reserved	Reserved, read as 0
6	FZIE	FZIE = 0: disable energy freeze interrupt; = 1: Enable energy freeze interrupt
5	ZXIE	ZXIE = 0: Disable the zero-crossing interrupt; ZXIE = 1: Enable the zero-crossing interrupt.
4	QEOIE	QEOIE = 0: Disable custom energy register overflow interrupt; QEOIE = 1: Enable custom energy register overflow interrupt.
3	PEOIE	PEOIE = 0: Disable active energy register overflow interrupt; PEOIE = 1: Enable active energy register overflow interrupt.
2	QFIE	QFIE = 0: Disable the QF interrupt; QFIE = 1: Enable the QF interrupt.
1	PFIE	PFIE = 0: Disable the PF interrupt; PFIE = 1: Enable the PF interrupt.
0	DUPDIE	DUPDIE = 0: Disable the data update interrupt; DUPDIE = 1: Enable the data update interrupt. The data PowerPA / PowerPB, IARMS / IBRMS and URMS registers have the refresh frequency of 3.495Hz or 13.982Hz, and when the above-mentioned data is updated, the IRQ_N pin will output a low level.

Interrupt status register

Interrupt Flag Register (IF) Address: 0x41H read-only		
Bit	Bit Name	Descriptions of Functions
7	Reserved	Reserved, read as 0
6	FZIE	FZIE = 0: no energy freeze event occurs t; = 1: energy freeze event occurs
5	ZXIF	ZXIF = 0: No zero-crossing event occurs; ZXIF = 1: zero-crossing event occurs.
4	QEOIF	QEOIF = 0: There is no reactive energy register overflow event occurring; QEOIF = 1: There is some reactive energy register overflow event occurring.
3	PEOIF	PEOIF = 0: There is no active energy register overflow event occurring; PEOIF = 1: There is some active energy register overflow event occurring.
2	QFIF	QFIF = 0: No QF pulse output event occurs; QFIF = 1: Some QF pulse output event occurs.

1	PFIF	PFIF = 0: No PF pulse output event occurs; PFIF = 1: PF pulse output event occurs.
0	DUPDIF	DUPDIF = 0: No data update event occurs; DUPDIF = 1: data update event occurs.

IF applies to SPI and UART interfaces. When some interrupt event occurs, the hardware will set the corresponding interrupt flag as 1.

IF interrupt flags can be generated not subject to the control of interrupt enable register IE, but to the occurrence of the interrupt event.

IF is a read-only register and will be cleared after read.

Reset Interrupt Flag Register

Reset Interrupt Flag Register (RIF)			Address： 0x42H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	RZXIF	RQEOIF	RPEOIF	RQFIF	RPFIF	RDUPDIF

The function of this register is the same as IF.

2.12.5 System Status Register

System Status Register

System Status Register (SysStatus) Address: 0x43H read-only		
Bit	**Bit Name**	**Descriptions of Functions**
7-5	Reserved	Reserved
4	WREN	Write enable flag: = 1 means that it allows writing in registers with write-protection; = 0 means that it allows no writing in registers with write-protection
3	Reserved	Reserved
2	IS	RN8209D :Pin status bit of the selection of serial communication type, used to determine the type of chip communication interfaces. IS = 0 means that UART is selected as the communication interface; IS = 1 means that SPI is selected as the communication interface. RN8209C: read as 0
1	SOFTRST	Soft-reset flag-When there is a soft-reset occurred, this bit will be set to 1, it will be cleared after read. It can be used as a calibration data request after reset.
0	RST	Hardware reset flag - When the external RST_N pin or power-on reset has ended, this bit is set as 1. Reset after read. It can be used as a calibration data request after reset.

SPI / UART checkout register

The RData (0x44H) register holds the previous SPI/UART read-out data, able to be used for checkout when SPI/UART has read out data.

SPI / UART write checkout register

The WData (0x45H) register holds the previous SPI/UART written data, able to be used for checkout when SPI/UART has written data.

2.12.6 Special commands

Command Name	Command Register	Data	Description

Write enable command	0xEA	0xE5	Enable WRITE operations
Write-protect command	0xEA	0xDC	Disable WRITE operations
Current Channel A Selection Command	0xEA	0x5A	Current Channel A setting command – To specify the current channel A as the current channel currently used to calculate the active energy.; Only when the write has been enabled, the system can accept this command; the CHNSEL register bit in the energy measurement status register reflects the implementation results of this command.
Current Channel B Selection Command	0xEA	0xA5	Current Channel B setting command – To specify the current channel B as the current channel currently used to calculate the active energy; Only when the write has been enabled, the system can accept this command; the CHNSEL register bit in the energy measurement status register reflects the implementation results of this command.
Command resets	0xEA	0xFA	Reset command is equivalent to external PIN reset; Only when the write has been enabled, the system can accept this command; It is suggested to commit command reset or pin reset before CPU take measuring initialization.

Scope of write protection:

0x00h-0x17h calibration parameter configuration registers, 0x20h-0x21h fast pulse registers and 0x40h interrupt enable registers, can not be modified unless special commands are adopted to enable the write, and the specific command formats are as shown in the above table.

3 Calibration Methods

3.1 Overview

RN8209 provides many calibration means to achieve software calibration, and the calibrated meter can have the accuracy of active and reactive power up to 0.5S. RN8209 includes the following calibration means:

- Provide adjustable meter constant (HFConst)
- Provide Channel A / B gain and consistency calibration
- Provide Channel A / B phase calibration
- Provide Channel A / B active, reactive and RMS offset calibration
- Provide reactive phase calibration
- Provide small-signal speedup calibration
- Provide automatic checksum of calibration data

3.2 Calibration Flow and Parameter Calculation

The calibration can be carried by standard meter, in which active and custom energy pulse PF / QF

can be connected to standard meter to calibrate measuring accuracy of RN8209 by the error shown on standard meter.

3.2.1 Calibration Flow

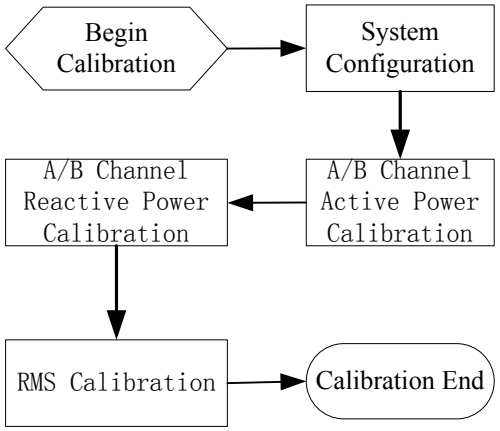


Figure 3-1 Calibration Flow

3.2.2 Parameter Settings

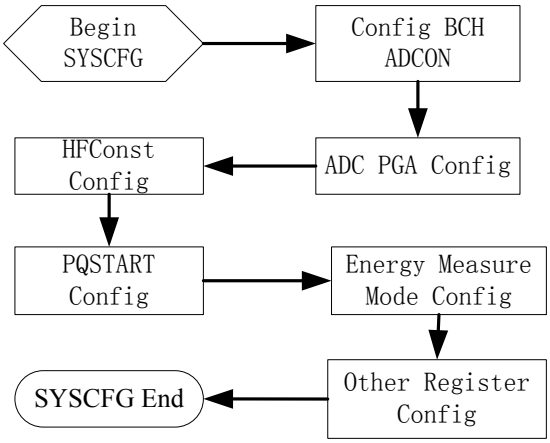


Figure 3-2 Parameter Settings Flow

HFConst parameter calculation:

When osci = 3.579545MHz, HFConst is calculated as follows:

HFConst＝INT[16.1079*Vu*Vi*10^11/(EC*Un*Ib)]

Vu: In time of rated voltage input, the voltage of voltage channel (pin voltage × magnification)

Vi: In time of rated current input, the voltage of current channel (pin voltage × magnification)

Un: Rated input voltage; Ib: Rated input current; EC: meter constant

3.2.3 Active Calibration

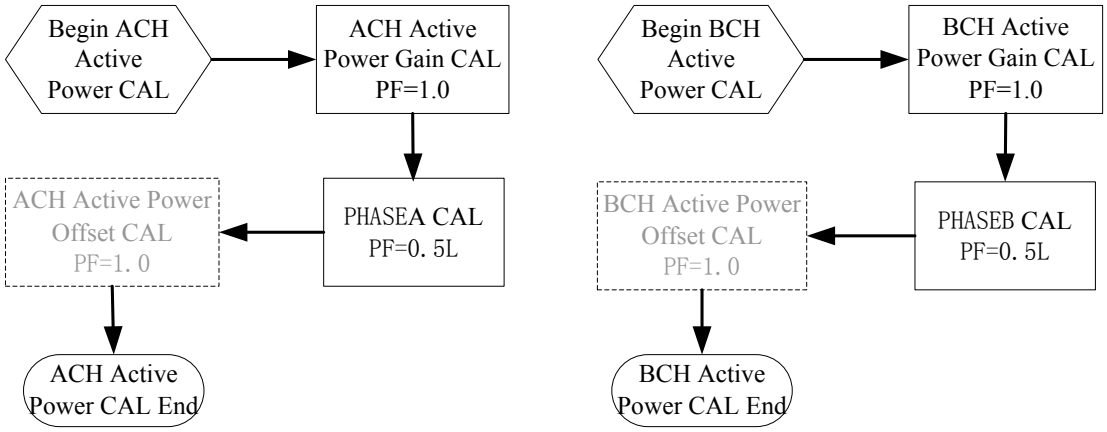


Figure 3-3 Active Calibration Flow

1. Channel A power gain calibration can be achieved by configuring a GPQA register, with GPQA calculated as follows:

Suppose the standard meter has the read error of err when Channel A is 100% Ib and PF = 1:

$$Pgain = \frac{-err}{1+err}$$

If Pgain>=0, then GPQA=INT [Pgain*2^{15}]

Otherwise, Pgain<0, then GPQA=INT [2^{16}+Pgain*2^{15}]

Channel B power gain calibration can be achieved by configuring a GPQB register, same as GPQA.

2. Calculation of Channel A / B phase calibration registers:

If the standard meter has the read error of err in Channel A / B, 100% Ib, PF = 0.5L, then the phase calibration formula is as follows:

$$\theta = \text{Arcsin}\ \frac{-err}{\sqrt{3}}$$

For 50HZ, PHSA/B features the relation of 0.02^0/LSB, then

If θ>=0, PHSA/B = INT (θ/0.02^0)

If θ<0, PHSA/B =INT (2^8+θ/0.02^0)

3. Active offset calibration is an effective means to improve the small-signal active accuracy if the external noise (PCB noise, transformer noise, etc.) is greater and the integrated energy has impact on the accuracy of small signals. If the external noise has comparatively small impact on the small-signal active accuracy, this step can be ignored.

3.2.4 Reactive Calibration

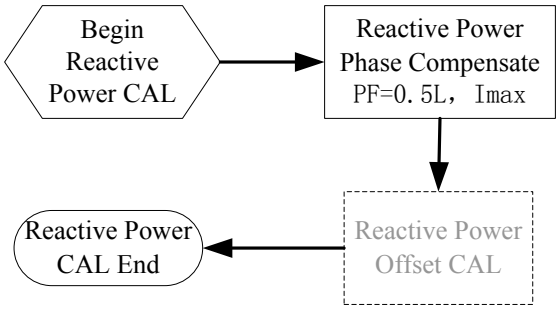


Figure 3-4 Reactive Calibration Flow

1. Reactive phase calibration registers are used as phase calibration of U-channel 90° phase-shift filter in the reactive calculation under large-signal conditions. Reactive phase calibration registers are calculated as follows:

If the standard meter has the read-out error of err in Channel A, Imax and PF = 0.5L (30 °), then:

α= error / cot (θ) = error * 0.5774

If α>=0, then Qphs=INT [$\alpha*2^{15}$]; if α< 0, then Qphs=INT [$2^{16}+\alpha*2^{15}$]

Note: Qphs calculation needs Channel A active power, so the calibration of this step must be completed after active calibration.

2. Reactive offset calibration is an effective means to improve the small-signal reactive accuracy if the external noise (PCB noise, transformer noise, etc.) is greater and the integrated energy has impact on the accuracy of small signals. If the external noise has comparatively small impact on the small-signal active accuracy, this step can be ignored.

3.2.5 RMS Calibration

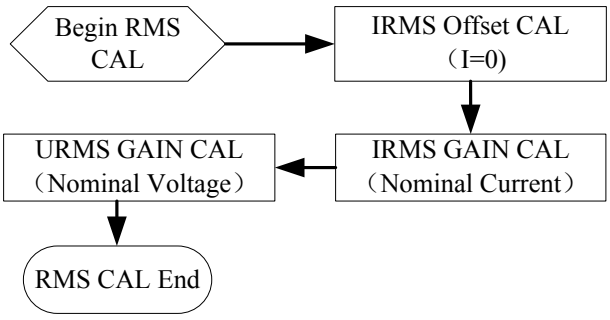


Figure 3-5 RMS Calibration Flow

Descriptions:

1. Current offset calibration can improve the small-signal current RMS accuracy.

The process for IARMSOS register calculation is as follows:

1) A standard meter support shall be configured so that U = Un and the current input is Vi = 0;

2) Wait for updates of DUPDIF identification bit (refresh at about 3.4Hz);

3) MCU takes the IARMS register value for temporary storage;

4) Repeat Step 2 and Step 3 for eleven times, with the first data able to be ignored. The MCU takes the following data to obtain the average of lave;

5) Find the lave ^ 2;

6) Find its 32-bit binary complement code, take the sign bit to fill in bit15 of the IARMSOS register, and take bit23 ~ bit8 to fill in IRMSOS bit14 ~ bit0 to obtain IRMSOS;

7) The rms offset calibration is completed.

So do the IBRMS calibration formula and the process of IBRMSOS register calculation.

2. When the current offset is well calibrated, then calibrate the current conversion factor KiA / KiB and the voltage conversion factor Ku of Channel A / B, which shall be completed by the MCU, with the calculation process as follows:

If the IARMS register has its reading as RMSIAreg in case of the rated current Ib, then

KiA＝Ib/RMSIAreg

Where, KiA is the ratio of the rated value and corresponding register in case of rated input.

Channel B conversion factor KiB can be calculated the same as the voltage conversion factor Ku.

3.3 Examples

Assuming a sample meter features a 220v (Un), 5A (Ib) rated input, with the meter constant of 3200 (EC). Channel A current sampling adopts 350 micro-ohm Manganin shunt, and Channel A has its analog gain of 16 times; Channel B current sampling adopts current transformers, and Channel B has its analog gain selected as 1 time (1X); the voltage channel adopts resistor divider input, the analog channel gain features 1 time and the chip pin voltage value is 0.22v.

1. Calculate HFConst

Vu＝0.22V; Vi＝5*0.00035*16＝0.028V; EC=3200; Un=220; Ib=5.

HFConst=INT[16.1079*Vu*Vi*10^11/(EC*Un*Ib)]=INT[2818.8825]=2818

After rounded, HFConst will be B02H(2881). And just write this value in HFCONST register.

2. Channel A Active Calibration

1) Channel A gain calibration

If the power source outputs a 220v and 5A signal with the power factor of 1, and the error displayed on the standard meter is 1.2%, then

Pgain＝-0.012/(1+0.012)=–0.01186

If this number is less than 0 and needs to be converted into a complement code, then

0.01186*2^15+2^16=0xFE7BH

Write FE7Bh into the GPQA register to complete gain calibration of Channel A.

2) Channel A phase calibration

After the resistive gain has been calibrated, the power factor will be changed to 0.5L, and if the error displayed on the standard meter is -0.4%, then

θ=ArcSin（-(-0.004)/1.732）=ArcSin 0.0023 ＝ 0.1323^0

phs=INT[0.1323/0.02]=6

After rounded, it will be 0x06H, and just write it into the angle calibration register PHSA.

3) Channel A active OFFSET calibration

If the current input is zero, the active power register has its value read as 0Xfffff50f (several times of average can be read), and its 32-bit complement code is 0x00000AF1. Take the latter 4 digits (0X0AF1) and write into the active offset calibration register.

Channel B active calibration is similar to Channel A.

3. Reactive Power Calibration

1) Reactive phase calibration

After the active calibration is completed, the reactive power only needs to accept phase calibration.

At the reactive power point 0.5L (30°), the error displayed on the standard meter is -0.04%, then

α= -0.0004*0.577= -0.0002308<0, Qphs=INT (2^16-.0002308*2^15) = 65528=0xfff8

Write the hexadecimal FFF8 into the reactive phase calibration register.

2) Reactive Offset

If the current input is zero, the reactive power register has its value read as 0XFFFFF47D (several times of average can be read), and its 32-bit complement code is 0x00000B83. Take the latter 4 digits (0X0B83) and write into the reactive offset calibration register.

4. RMS Calibration

The chip provides the current RMS offset calibration register, and if the current input is zero, the current rms register has its value read as 0x000483 (several times of average can be read), with the decimal number of 1155.

Square it to find its complement code: 1155*1155=1334025=0x145B09, 32-bit complement code to be 0Xffeba4f7.

Take the middle four digits 0xeba4 and write in the current rms offset calibration register.

The conversion factor shall be calculated by the MCU.

4 Communication Interfaces

- Two kinds of serial communication interfaces are supported by RN8209D: SPI and UART;and only UART is supported by RN8209C; the two types of communication interface both work under slave mode.
- The option of serial communication interfaces of RN8209D shall be set via the external pin IS;
- Both SPI and UART interfaces are compatible with 5V/3.3V;

4.1 SPI Interface

4.1.1 Descriptions of SPI Interface Signals

SCSN: SPI slave device chip select signal, active at low levels, input signal, internal floating, and external pull-up resistors recommended.

When SCSN is changing from high to low, it indicates that the current chip is selected and in the communication state; when SCSN from low to high, it means that the communication has ended, and the communication port is reset to an idle state.

SCLK: serial clock input pin – it decides the transmission rate of data in or out of the SPI port.

All data transmission operations are synchronized with SCLK, RN8209D outputs data from the SDO pin at the rising edge; the host outputs data from the SDI pin at the rising edge. RN8209D and the host will read data at the falling edge.

SDI: Serial data input pin – Used to transmit the master data to RN8209D inside.

SDO: serial data output pin- Used to output the RN8209D data to the master. It stays in high impedance when SCSN is in a high level.

4.1.2 SPI Frame Format

SPI frames include reading frames, writing frames and special command frames. Each frame has its transmission process as follows:

When RN8209D detects SCSN falling edge, SPI will enter the means of communication, and in this mode, RN8209D will wait for the MCU to transmit the command bytes to the command register.

The command register is a 8-bit wide register. For the read and write operations, bit7 of the command register will be used to determine whether this data transmission operation is a read or write

operation, and bit6-0 of the command register is a read-write register address. For the special command operations, the command register has its bit7-0 fixed to be 0xEAH.

After the command register has been written, chip analysis and response the command, the data transmission will start. After data transmission is completed, SPI will enter a communication mode again, waiting for the CPU to transmit new command bytes to the command register.

These three types of SPI frame formats are described in Table 4-1.

Table 4-1 SPI Frame Formats

Command Name	Command Register	Data	Descriptions
Read command	{0,REG_ADR[6:0]}	RDATA	Read data from a register with the address of REG_ADR [6:0]. Note: If an invalid address is read, the return value is 00h.
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register with the address of REG_ADR [6:0].
Write Enable Command	0xEA	0xE5	See Section 2.11.6 Special Commands
Write-Protect Command	0xEA	0xDC	
Command for Current Channel A Selection	0xEA	0x5A	
Command for Current Channel B Selection	0xEA	0xA5	
Command resets	0xEA	0xFA	

4.1.3 SPI Write Operation

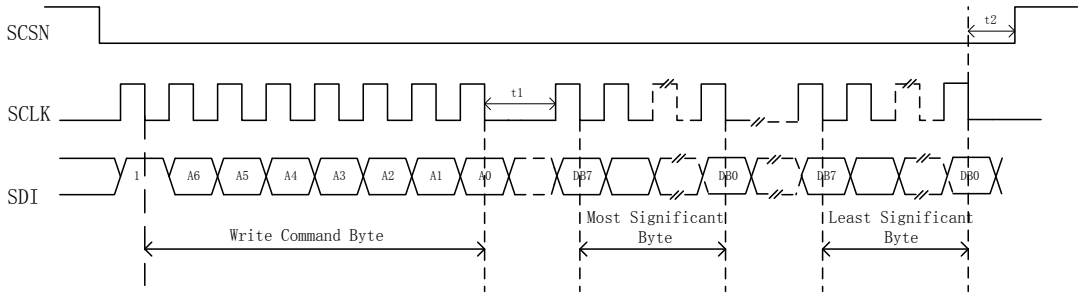


Figure 4-1 SPI Write Timing

Work process:

If the SCSN is valid, then the host will write in command bytes (8bit, including the register addresses) via SPI, and then write in data bytes. Note:

1. Transmit in bytes, high bit first while low bit later;
2. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;
3. The host writes in data at the SCLK rising edge while the slave reads data at the SCLK falling edge;
4. The time t1 between data bytes should be greater than or equal to half SCLK cycle;
5. After the LSB of the last byte has been transmitted, the SCSN will change from low to high and end data transmission. The time t2 between the SCLK falling edge and the SCSN rising edge should be greater than or equal to half SCLK cycle.

Note: The registers with write protection should have write enable command written in at first before write operations.

4.1.4 SPI Read Operation

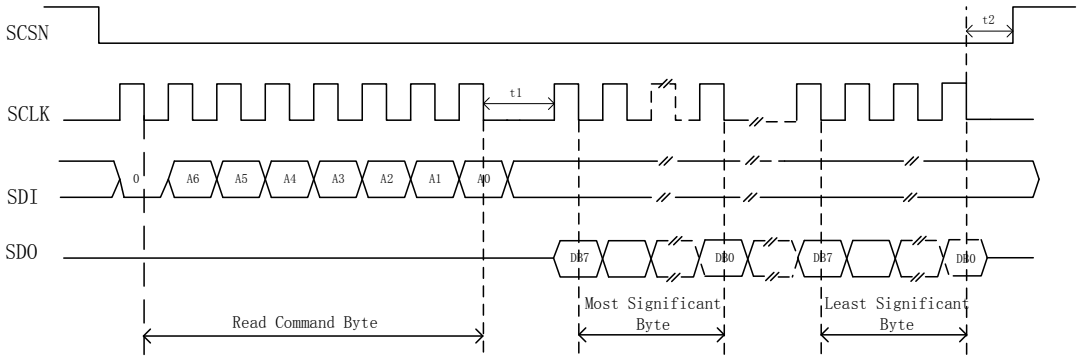


Figure 4-2 SPI Read Timing

Work process:

If the SCSN is valid, then the host will write in command bytes (8bit, including the register addresses) via SPI, and the slave will output the data in bytes from the SDO pin at the SCLK rising edge. Note:

1. Transmit in bytes, high bits first while low bits later;

2. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;

3. The host writes in command bytes at the SCLK rising edge while the slave outputs data from SDO at the SCLK rising edge;

4. The time t1 of data bytes should be greater than or equal to half SCLK cycle;

5. After the LSB of the last byte has been transmitted, the SCSN will change from low to high and end data transmission. The time t2 between the SCLK falling edge and the SCSN rising edge should be greater than or equal to half SCLK cycle.

4.1.5 SPI Interface Reliability Design

The SPI interface reliability design includes the following contents:

- . Checkout functions

1. Provide the checkout register EMUStatus (0x2DH) to store the checksum of internal calibration registers.

2. Provide the SPI read checkout register RData (0x44H) to save the previous SPI read-out data.

3. Provide the SPI write checkout register WData (0x45H) to save the previous SPI written-in data.

. Write protection

Provide write-protect features for all readable and writable registers.

Application circuit design

The SPI transmission signal lines may vibrate subject to interference so the external resistors and capacitors are necessary for filtering. The parameters can be selected according to needs.

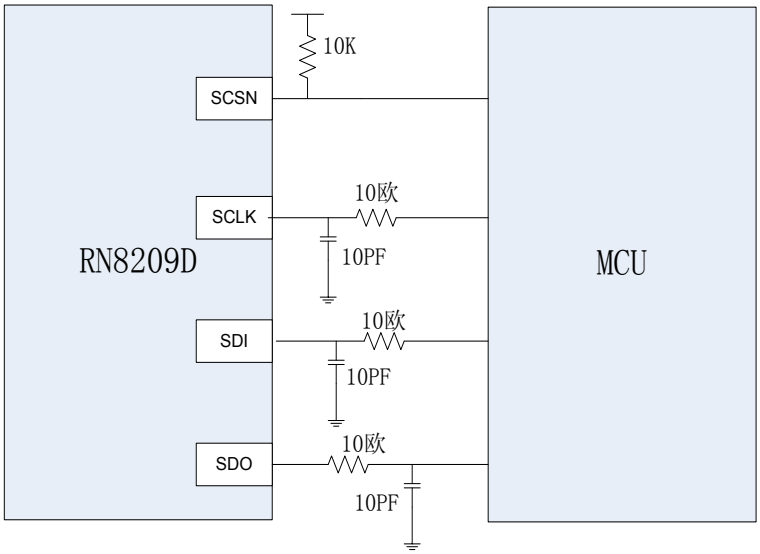


Figure 4-3 SPI Typical Connection

4.2 UART Interface

The main features of RN8209's UART are as follow:

- Work uder slave mode, half duplex communication, 9-bit UART(including parity bit), meat standard UART protocol.
- The baudrate of RN8209D's UART is set by pin as 2400/4800/9600/19200bps.
- The baudrate of RN8209C's UART is fixed to 4800.
- It is safe and reliable, since there is a parity bit in the frame.
- 5V/3.3V compatible.

4.2.1 Signal Description of the UART interface

TX: Data transmitting pin of UART slave (RN8209) ;

RX: Data receiving pin of UART slave (RN8209);

B1 / B0: Baud rate selecting pin, used to configure RN8209D's UART baud rate, the different configuration of B1 / B0will result different value of the system control register SYSCON:[14:8] , the correspondence relationship is shown below;

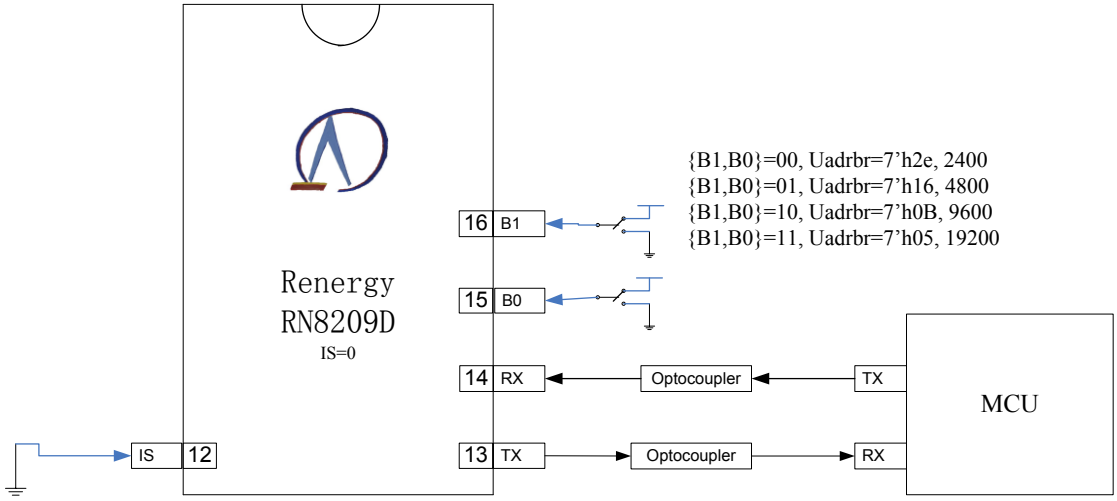
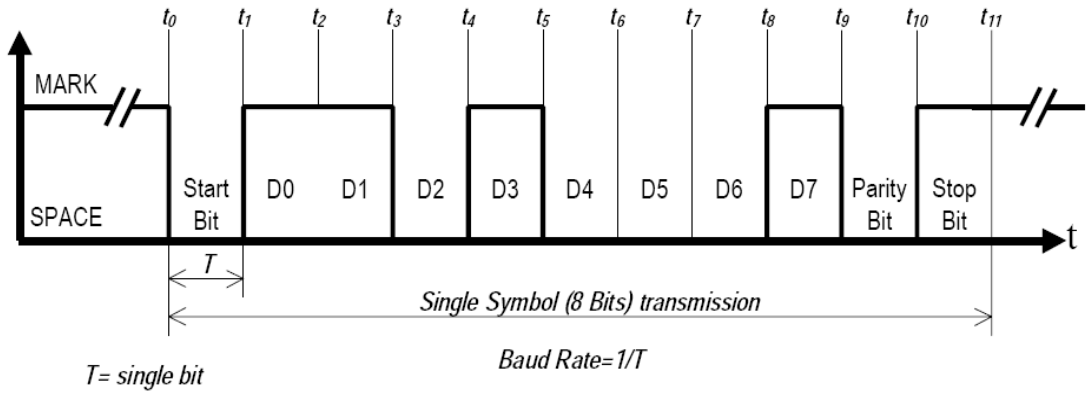


Figure 4-4 Typical wiring diagram of RN8209D's UART

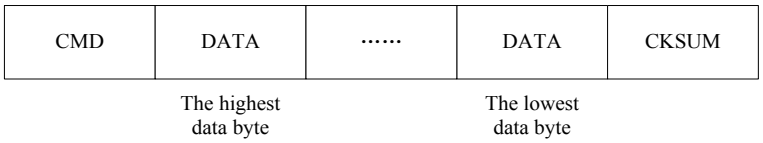
4.2.2 UART data byte format

UART is a 9-bit asynchronous communication port, it will send/receive 11-bit, including start bit (StartBit, 0), data bits (low bit first), and a even parity bit (Parity Bit, the 9th bit of data bits) for one byte information. The format is shown as below.



4.2.3 UART frame format

RN8209 UART communication frame format is shown in the following figure and table:



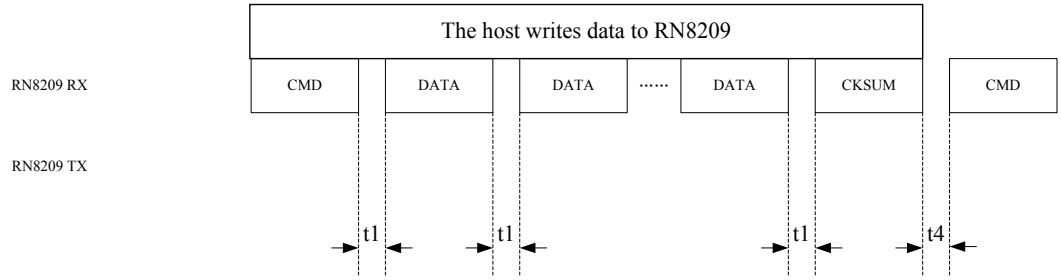
Name	Explanation
CMD	Command byte send by host CMD[7]: indicating command type; 0, read command 1: write command CMD[6:0]：the register address of the selected RN8209, if CMD[7]＝1，and CMD[6:0]=0x6A，it means that it is a special command.
DATA	Data byte: send by slave in reading operation, by host in writing operation. If the operated register is multi-bytes register, the highest byte is transmitted firstly.
CKSM	Checksum byte; send by slave in reading operation, by host in writing operation. The algorithm of the checksum is as follow: CheckSum[7:0] = ~(CMD[7:0] + DATAn[7:0] + …… +DATA1[7:0]) which is to sum CMD and data bytes, and ignore carry bit, then flip each bit of the result.

Command Name	Command Register	Data	Descriptions
Read command	{0,REG_ADR[6:0]}	RDATA	Read data from a register with the address of REG_ADR [6:0]. Note: If an invalid address is read, the return value is 00h.
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register with the address of REG_ADR [6:0].
Write Enable Command	0xEA	0xE5	See Section 2.11.6 Special Commands
Write-Protect	0xEA	0xDC	

Command			
Command for Current Channel A Selection	0xEA	0x5A	
Command for Current Channel B Selection	0xEA	0xA5	
Command resets	0xEA	0xFA	

4.2.4 UART Write Operation

UART Write Operation is started by host to send a command byte, if it is a write command, the slave will receive the following data bytes and checksum byte. The UART write operation process is shown at below:

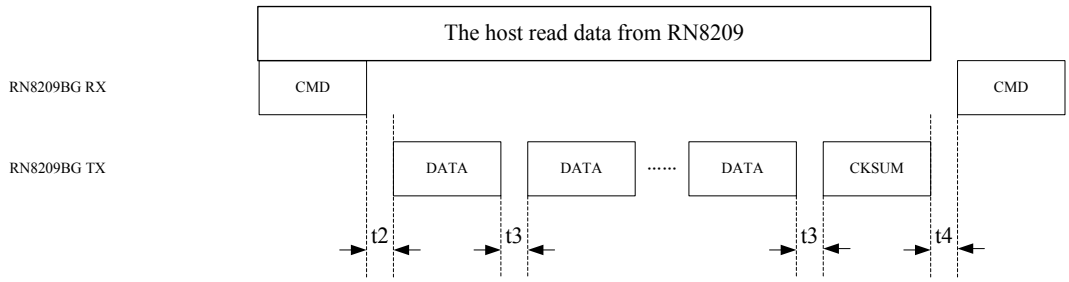


Notes:

1. One byte of 9-bit UART is consist of 11 bits which includes a start bit (0), data bit (low firstly), a even parity bit (the 9th data bits) and a stop bit (1).
2. The sender will calculate and send checksum, the receiver will judge the validation of the byte base on the checksum, if the byte is invalid, the following bytes will be taken as a new frame;
3. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;
4. The time t1 between data bytes sent by host is controlled by host, it can be any value for RN8209, that is it is fine when t1 is greater than or equal to 0ns;
5. The time t4 between frames is controlled by host, it can be any value for RN8209, which is fine when t4 is greater than or equal to 0ns;
6. The registers with write protection should have write enable command written in at first before write operations.
7. The host will calculate and send checksum, the slave will judge whether the transmission succeeds base on the checksum.

4.2.5 UART Read Operation

UART Read Operation is started by host to send a command byte, than RN8209 will send the following data bytes and checksum byte. The UART read operation process is shown at below:



1. One byte of 9-bit UART is consist of 11 bits which includes a start bit (0), data bit (low firstly), a even parity bit (the 9th data bits) and a stop bit (1);
2. The sender will calculate and send checksum, the receiver will judge the validation of the byte base on the checksum, if the byte is invalid, the following bytes will be taken as a new frame;
3. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;
4. The time t1 between data bytes sent by host is controlled by host, it can be any value for RN8209, that is it is fine when t1 is greater than or equal to 0ns;
5. The time t2 between bytes send by host and bytes send by slave is controlled by slave, t2=T/2 (T is the time for one bit transmission);
6. The time t3 between bytes send by slave is controlled by slave, t3=T (T is the time for one bit transmission);
7. The time t4 between frames is controlled by host, it can be any value for RN8209, which is fine when t4 is greater than or equal to 0ns;
8. The slave will calculate and send checksum, the host will judge whether the transmission succeeds base on the checksum.

4.2.6 UART Interface Reliability Design

The UART interface reliability design includes the following contents:

- The UART baudrate is set by hardware pin which is safe and reliable.
- There is a checksum bit (an even parity bit) in byte transmission
- There is a checksum byte in frame transmission
- The configuration of pin for baudrate can be referred in register.
- Checksum for registers

  1. Provide the checkout register EMUStatus (0x2DH) to store the checksum of internal calibration registers.
  2. Provide the read checkout register RData to save the previous read-out data.
  3. Provide the write checkout register WData to save the previous written-in data.

. Write protection

Provide write-protect features for all readable and writable registers.

5 Electrical Specification

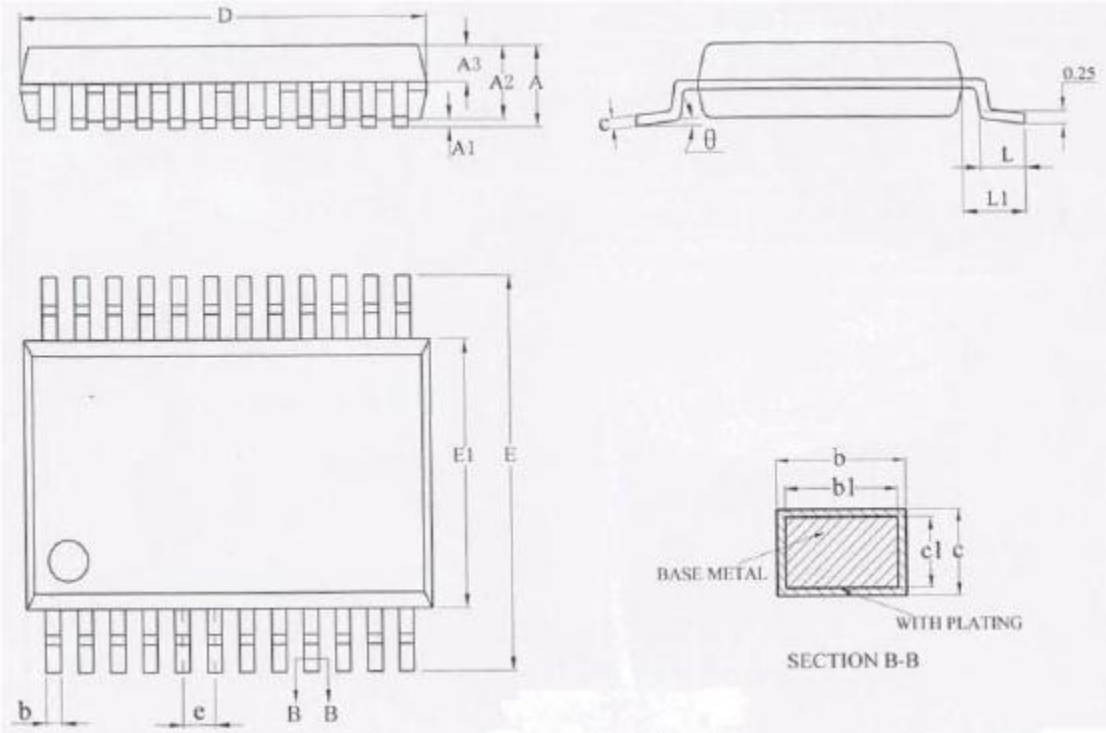
Accuracy (V_{dd}=AV_{dd}=5V±5%, room temperature)						
Measured Items	**Symbol**	Min.	Typical	Max.	Unit	Test Conditions and Notes
Active energy	Err			±0.1%		At room temperature

measurement error						8000:1 dynamic range
Active energy measurement bandwidth	BW		7		kHz	OSCI=3.579545MHz
Reactive energy measurement error	Err			±0.1%		At room temperature 8000:1 dynamic range
RMS measurement error	Err			±0.1%		At room temperature 1000:1 dynamic range
Analog Input						
Maximum signal level	V_{xn}			±1000	mV	
DC input impedance	Z_{DC}	300			kΩ	
ADC offset error	DC_{off}		1		mV	
-3dB bandwidth	B_{-3dB}		7		kHz	OSCI=3.579545MHz
Reference Voltage (V_{dd}=AV_{dd}=5V±5%, temperature range: -40 ℃ ~ +85 ℃)						
Output voltage	Vref		1.25		V	
Temperature coefficient	Tc		5	15	ppm/℃	
Input impedance			4		kΩ	
Clock Input						
Range of input clock frequency	OSCI	1	3.58	4	MHz	
Digital input and output interfaces						
SPI interface speed				1.2M	Hz	
UART interface speed		2400		192000	Hz	
High level of output at RSTN、A0、A1	V_{IH}	0.7 * vdd	--	DV_{DD}	V	DV_{dd} =5V，-40-85℃
Low level of output at RSTN、A0、A1	V_{IL}	DGND	--	0.3* Vdd	V	DV_{dd} =5V，-40-85℃
High level of input at SDI/RX 、SCLK/B0 、SCSN/B1	V_{IH}	2.5	--	DV_{DD}	V	DV_{dd} =5V，-40-85℃
Low level of input at SDI/RX 、SCLK/B0 、SCSN/B1	V_{IL}	DGND	--	1.7	V	DV_{dd} =5V，-40-85℃
High level of output at IRQN/ZX	V_{OH}	4	--	DV_{DD}	V	DV_{dd} =5V，room temperature；Isource=3.5mA
Low level of output at IRQN/ZX	V_{OL}	--	--	0.5	V	DV_{dd} =5V，room temperature；Isink=8mA
High level of output at PF、QF、SDO	V_{OH}	4	--	DV_{DD}	V	DV_{dd} =5V，room temperature;

						Isource=5mA
Low level of output at PF、QF、SDO	V_{OL}	DGND	--	0.5	V	DV_{dd} =5V , room temperature Isink=12mA
Power Supply						
Analog power	AVDD	4.5		5.5	V	5V±10% or 3.3V±10%
Digital power	DVDD	4.5		5.5	V	5V±10% or 3.3V±10%
Analog Current 1	Aldd1		1.5		mA	Channel B ADC closed
Analog Current 2	Aldd2		1.8		mA	Channel B ADC open
Digital current	Dldd		1.3		mA	OSCI=3.579545MHz
Absolute Maximum Ratings						
Digital supply voltage	DVDD	-0.3	--	+7	V	
Analog supply voltage	AVDD	-0.3	--	+7	V	
DVDD to DGND		-0.3	--	+7	V	
DVDD to AVDD		-0.3		+0.3	V	
V1P,V1N,V2P,V2N		-6		+6	V	
Digital input voltage relative to GND	V_{IND}	-0.3	--	DV_{DD} +0.3	V	
Digital output voltage relative to GND	V_{outD}	-0.3	--	DV_{DD} +0.3	V	
Analog input voltage to AGND	V_{INA}	-0.3	--	AV_{DD} +0.3	V	
Range of operating temperature	T_A	-40	--	85	℃	
Range of storage temperature	T_{stg}	-65	--	150	℃	

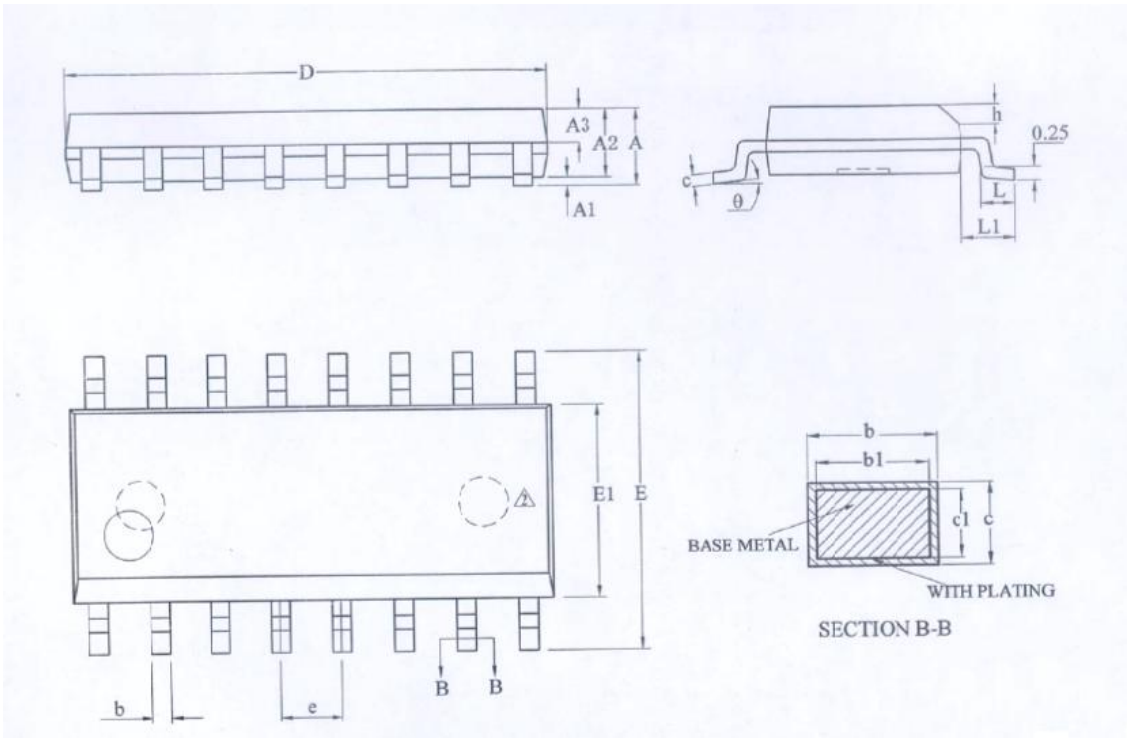
6. Package

Package dimensions of RN8209D-SSOP24:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.85
A1	0.05	0.15	0.25
A2	1.30	1.50	1.70
A3	0.57	0.67	0.77
b	0.29	---	0.37
b1	0.28	0.30	0.33
c	0.15	---	0.20
c1	0.14	0.15	0.16
D	8.00	8.20	8.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.75	0.90	1.05
L1	1.25BSC		
θ	0	-----	8°

Package dimensions of RN8209C-SOP16L:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.75
A1	0.05	---	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	---	0.48
b1	0.38	0.41	0.43
c	0.21	---	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	---	0.5
L	0. 5	---	0.8
L1	1.05BSC		
θ	0	-----	8°