

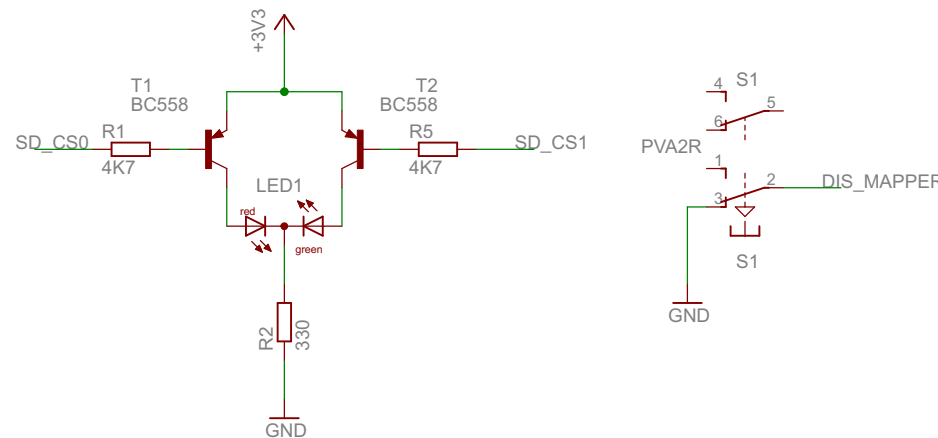
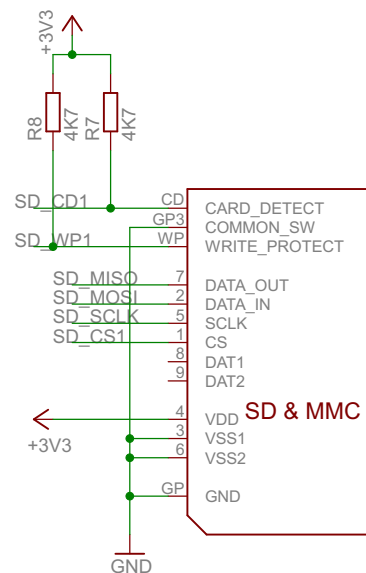
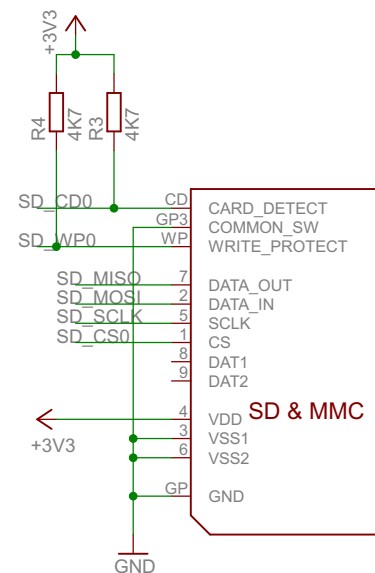
The diagram illustrates the connection of the AM29F010J EPROM to the CPU_A[0..15] and CPU_D[0..7] buses. The EPROM is connected to CPU_A[0..15] via JP1 and to CPU_D[0..7] via IC1. The diagram includes pin numbers and signal names for both connections.

JP1 Connections:

JP1 Pin	Signal	Direction
A0	D0	Out
A1	D1	Out
A2	D2	Out
A3	D3	Out
A4	D4	Out
A5	D5	Out
A6	D6	Out
A7	D7	Out
A8	BUSDIR	In
A9	INT	In
A10	WAIT	In
A11	MT	In
A12	RESET	In
A13	RFSH	In
A14	CLOCK	In
A15	MREQ	In
SW1	MREQ	In
SW2	I/O	In
SW	WR	In
+12V	RD	In
-12V	CS1	In
GND2	CS2	In
GND1	CS12	In
+5V2	SLTSL	In
+5V1	RES	In
SOUNDIN	RES	In

IC1 Connections:

IC1 Pin	Signal	Direction
12	A0	Out
11	A1	Out
10	A2	Out
9	A3	Out
8	A4	Out
7	A5	Out
6	A6	Out
5	A7	Out
27	A8	Out
26	A9	Out
23	A10	Out
25	A11	Out
4	A12	Out
28	A13	Out
29	A14	Out
3	A15	Out
2	A16	Out
22	ROM_CS	In
24	CPU_RD	In
31	ROM_WE	In
13	O0	Out
14	O1	Out
15	O2	Out
17	O3	Out
18	O4	Out
19	O5	Out
20	O6	Out
21	O7	Out
1	CE	In
30	OE	In
	WE	In



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