HunterSun HS6620D

Bluetooth Low Energy Compliant and 2.4-GHz Proprietary System-on-Chip

Version 3.0

2019/5/15

Wireless connect anywhere by HunterSun technology

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Revision History

version	summery	date	author
1.0	Initial version	2018-03-13	

1 System Overview

1.1. General Description

The HS6620D is a power-optimized true system-on-chip (SoC) solution for both Bluetooth low energy and proprietary 2.4-GHz applications. It integrates a high performance and low power RF transceiver with Bluetooth baseband and rich peripheral IO extension. HS6620D also integrates a power management to provide high-efficient power management. It targets 2.4-GHz Bluetooth low energy systems, proprietary 2.4-GHz systems, Human-Interface Devices (keyboard, mouse, and remote control), sports and leisure equipment, mobile phone accessories and consumer electronics.

HS6620D on-chip Bluetooth system compliant with version 4.2, support all Bluetooth standard 4.2 feature.

The chip integrates 48Mhz high-performance MCU, DMA, GPIO, I2S, i2C, SPI, UART, TIMER, RTC, watch dog, supports 24Mhz external crystal, integrates multi-purpose 12 bit ADC.

The HS6620D integrates on chip 256KB ROM, 128K SRAM and supports user defined IDE system, on chip SFLASH MCU development and JTAG software upgrade.

1.2. Features

- RF transceiver
  - -93 dBm sensitivity Bluetooth® low energy
  - TX Power -20 to +2 dBm
  - 10mA peak RX, 10mA peak TX (0dBm)
  - Active-mode MCU: 108 µA/MHz
  - RSSI (1 dBm resolution)
- CPU
  - ARM® Cortex™-M3, max 48MHz
  - Serial Wire Debug (SWD)
- Memory
  - 128KB SRAM
  - 256KB ROM
  - 1MB SFLASH
- Clocks
  - 24MHz crystal, 24MHz RC, 32.768KHz crystal, 32.768KHz RC

- Link Controller
  - BT 4.2 LE PHY, link controller
  - Proprietary 2.4-GHz link controller
- Power Management
  - Deep sleep power 5uA
  - Supply voltage range 2.7V to 3.6V
  - Built-in charger
- Software
  - Full compliant with BLE version 4.2, complete power-optimized stack, including controller and host
  - Supports mesh network
  - Network processor interface for applications running on an external microcontroller
  - Sample applications and profiles
  - Supports 6LowPAN
  - Supports OTA
  - SWD interface
- Peripherals
  - four channels DMA
  - Two UART interface, one share with 7816 interface
  - I2S interface
  - Up to 31 bits general-purpose I/O GPIO
  - I2C master or slave interface
  - Two SPI master or slave interface
  - Watchdog to prevent system dead lock
  - RTC
  - Three 32bit timers
  - Keyboard controller, up to 8x18
  - Three way QDEC
  - Eight single-end or differential-end 12bits GP-ADC
  - AES HW encryption

1.3. Chip Applications

The HS6620D integrated circuit has a fully integrated radio transceiver and baseband processor for Bluetooth® Smart. It can be used as an application processor as well as a data pump in fully hosted systems.

Figure 1 HS6620D chip wireless applications

1.4. System Function Block Diagram

HS6620D is a low power Bluetooth wireless transceiver chip. The chip integrates Bluetooth base band, PHY and proprietary 2.4GHz protocol. The MCU accesses system hardware resource by AHB bus, ROM, RAM, DMA, SFLASH, GPIO exchange data through AHB bus, and all other peripheral is accessed through AHB to APB Bridge and APB bus.

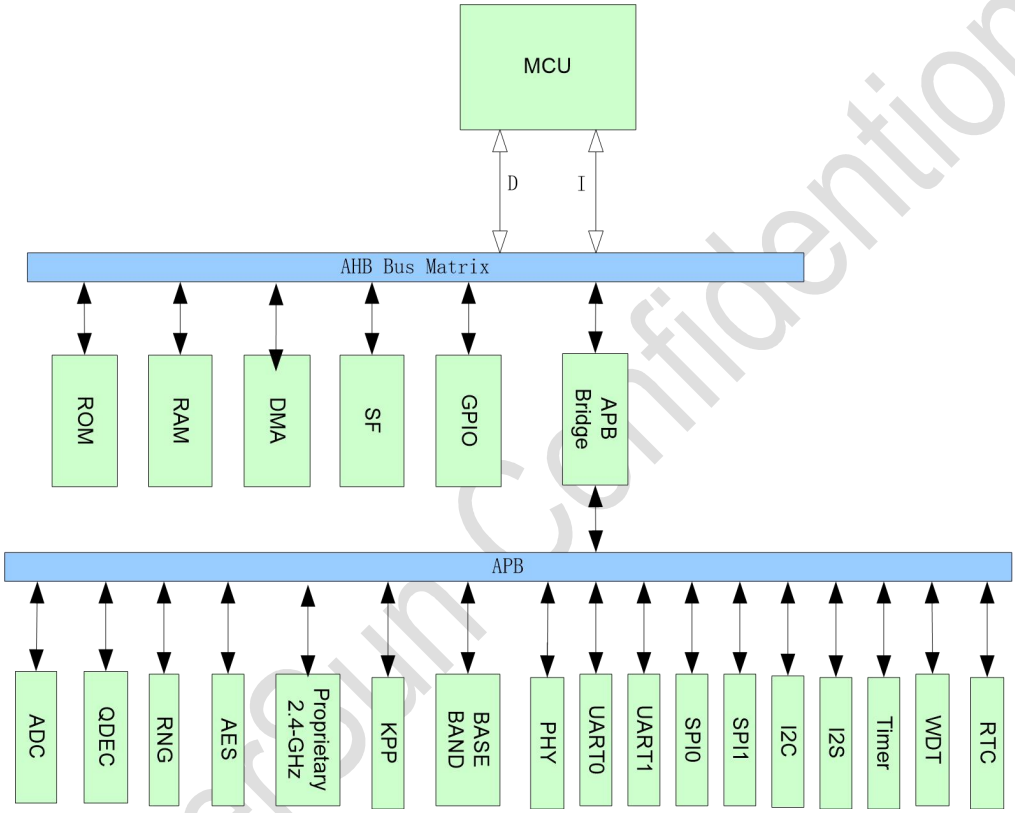

Figure 2 HS6620D system block diagram

2 Chip Description

2.1 Pin Definition

The HS6620D is in the 6mmx6mm QFN48 package. The chip pin definition is as below:

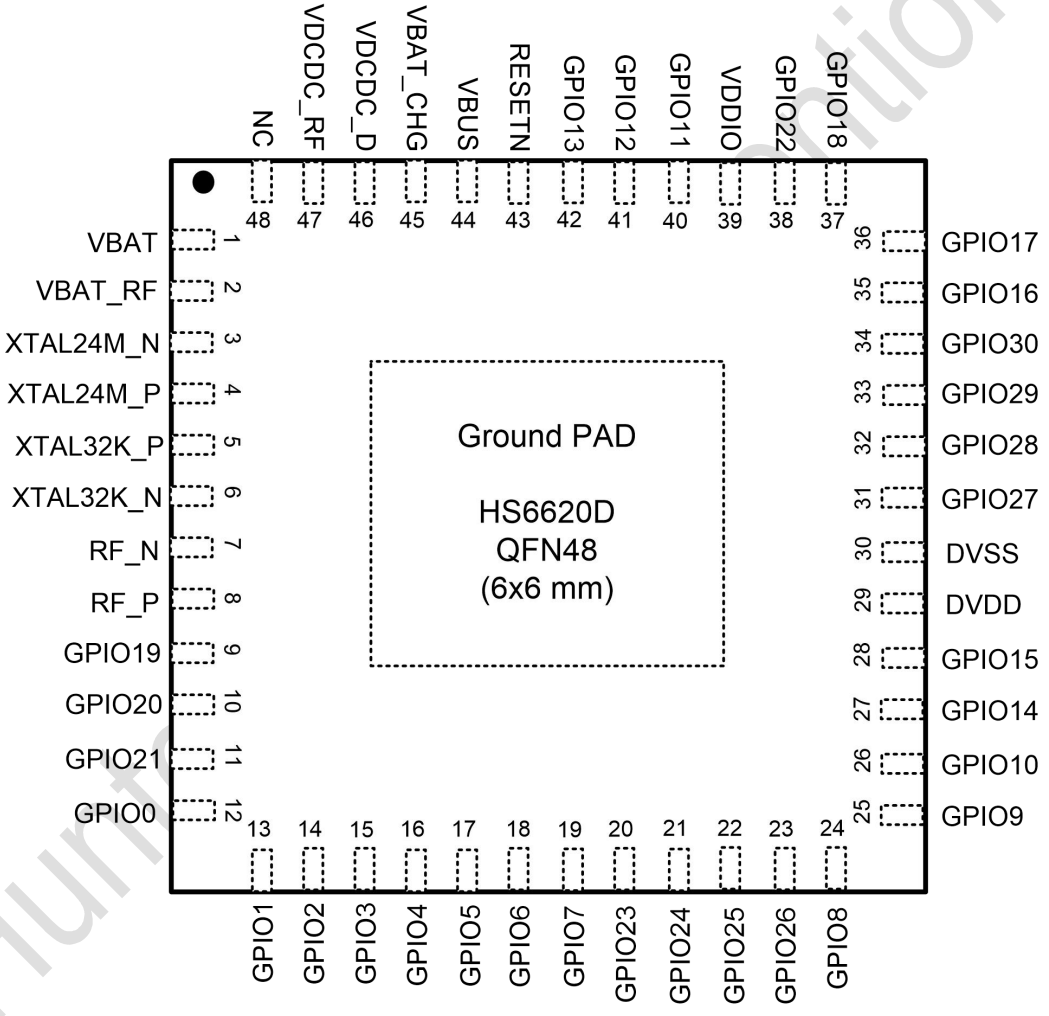

Figure 3 HS6620D chip pin definition

2.2 Pin Description

PIN	NAME	TYPE	Description	NOTE
1	VBAT	Power	Connect to battery	
2	VBAT_RF	Power	Connect to VBAT on PCB	
3	XTAL24M_N	Analog	Crystal 24M output	
4	XTAL24M_P	Analog	Crystal 24M input	
5	XTAL32K_P	Analog	Crystal 32.768K input	
6	XTAL32K_N	Analog	Crystal 32.768K output	
7	RF_N	Analog	RF ground	
8	RF_P	Analog	RF input/output	
9	GPIO19	Digital	Digital GPIO	Note 1
10	GPIO20	Digital	Digital GPIO	Note 1
11	GPIO21	Digital	Digital GPIO	Note 1
12	GPIO0	Digital/Analog	Digital GPIO/GP-ADC input	It is JTAG clock by default. Note 1
13	GPIO1	Digital/Analog	Digital GPIO/GP-ADC input	It is JTAG data I/O by default. Note 1
14	GPIO2	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
15	GPIO3	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
16	GPIO4	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
17	GPIO5	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
18	GPIO6	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
19	GPIO7	Digital/Analog	Digital GPIO/GP-ADC input	Note 1
20	GPIO23	Digital	Digital GPIO	Note 1
21	GPIO24	Digital	Digital GPIO	Note 1
22	GPIO25	Digital	Digital GPIO	Note 1
23	GPIO26	Digital	Digital GPIO	Note 1
24	GPIO8	Digital	Digital GPIO	Note 1
25	GPIO9	Digital	Digital GPIO	Note 1
26	GPIO10	Digital	Digital GPIO	Note 1
27	GPIO14	Digital	Digital GPIO	Note 1
28	GPIO15	Digital	Digital GPIO	Note 1
29	DVDD	Power	Digital power supply	
30	DVSS	Power	Digital ground	
31	GPIO27	Digital	Digital GPIO	Note 1
32	GPIO28	Digital	Digital GPIO	Note 1
33	GPIO29	Digital	Digital GPIO	Note 1

34	GPIO30	Digital	Digital GPIO	Note 1
35	GPIO16	Digital	Digital GPIO	Note 1
36	GPIO17	Digital	Digital GPIO	Note 1
37	GPIO18	Digital	Digital GPIO	Note 1
38	GPIO22	Digital	Digital GPIO	Note 1
39	VDD_IO	Power	Digital IO power	
40	GPIO11	Digital	Digital GPIO	Note 1
41	GPIO12	Digital	Digital GPIO	Note 1
42	GPIO13	Digital	Digital GPIO	Note 1
43	RESETN	Digital	Reset signal	It must be connected to high, if not used
44	VBUS	Power	Connect to USB power	
45	VBAT_CHG	Power	Output to charger battery	
46	VDCDC_D	Power	Output of the DCDC converter 1.5V(typ)	
47	VDCDC_RF	Power	Connect to VDCDC_D on PCB 1.5V(typ)	
48	NC	NC	NC	

Table 1 HS6620D pin definition

Note 1: All digital peripheral pins can be programmed to any GPIO

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

HS6620D could be damaged by extra stress in excess of the absolute maximum ratings working conditions, please be sure the design is follow this rule.

Rating		Min	Max	Unit
Storage Temperature		-40	120	ºC
ESD	Human Body Mode	2000	-	V
	Machine Mode	200	-	V
	Charge Device Mode	500	-	V

Table 2 HS6620D absolute maximum ratings

3.2 Recommend Operating Conditions

Rating	Min	Typ	Max	Unit
Operation Temperature	-40	-	85	ºC
Digital Core supply voltage	0.95	1.05	1.2	V
RF supply voltage	1.4	1.5	1.6	V
I/O voltage (Vsupply>3.3)	3.1	3.3	3.5	V
I/O voltage (Vsupply<3.3)	Vsupply	Vsupply	Vsupply	V
Supply voltage	2.7	3.3	3.6	V

Table 3 HS6620D recommend operating conditions

3.3 Battery Charger

Charging Mode	Min	Typ	Max	Unit
Input Voltage (V_{IN}) Note: It needs more time to get battery fully charged when V_{IN}=4.5 4.5 5.0 7.0 (V)	4.5	5	6.5	V
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)	-	35	-	mA
Maximum Battery Fast Charge Current	-	100	-	mA
Trickle Charge Voltage Threshold	-	2.9	-	V
Float Voltage	-	-	-	
Battery Charge Termination Current, % of Fast Charge Current	-	10	-	%
Standby Mode	-	-	-	
Supply current to charger only	-	600	-	uA
Battery Current	-	600	-	uA

Table 4 HS6620D battery charger

3.4 Radio Characteristics

3.4.1 BLE Transmitter

[Core Supply Voltage = 1.25V @ 25℃]

Parameter		Min	Typ	Max	BLE Specification	Unit
Maximum RF transmit power		-	2	-	–	dBm
RF power control range		-18	-	2	-	dBm
RF power range control resolution		2.7	3	3.7	-	dB
ACP Note: Fo=2440MHz	F = Fo±2MHz	-	-		≤-20	dBm
	F = FO±>3MHz	-	-		≤-30	dBm
Δf_{1avg} maximum modulation		225	250	275		kHz
Δf_{2max} maximum modulation		100%			>99.9%	
$\Delta f_{2avg}/\Delta f_{1avg}$		0.84			>0.8	
Frequency Accuracy			4.03		-150~150	kHz
Frequency Offset			4.02		-150~150	KHz
Frequency Drift			-3.31		-50~50	KHz
Frequency Drift rate			-3.13		-20~20	KHz/50us
Initial Frequency Drift			-2.25		-20~20	KHz
2nd harmonic content				-50	<-40	dBm
3rd harmonic content		-		-50	<-40	dBm

Table 5 HS6620D BLE Transmitter

3.4.2 BLE Receiver

[Core Supply Voltage = 1.25V @ 25℃]

Parameter	Min	Typ	Max	BLE Specification	Unit

Sensitivity--PSR9 37byte package		-93[1]	-90	-81[2]	≤-70	dBm
Maximum received signal		-		10	0	dBm
I/C co-channel		-		9	-21	dB
Adjacent channel selectivity I/C Note: Fo=2440MHz	F = Fo+1MHz	-	-	1	-15	dB
	F = Fo -1MHz	-	-	-3	-15	dB
	F = Fo+2MHz	-	-	21	15	dB
	F = Fo-2MHz	-	-	23	15	dB
	F = Fo+3MHz	-	-	33	27	dB
	F = Fo-3MHz	-	-	34	27	dB

(1) Turn on soft decision of demodulation module

(2) @ 2424MHz 2448MHz 2472MHz（integral multiple of 24MHz channel）

Table 6 HS6620D BLE Receiver

3.5 Power Consumption

Operation Mode	Typical	DCDC on (VBAT=3.6V)	Ideal DCDC (Eff=100%)	Unit
Chip deep sleep	5			uA
Chip active	3.2	1.7	1.4	mA
Peak of Bluetooth transfer (2dBm)	20	11	8.5	mA
Peak of Bluetooth transfer (0dBm)	18	10	7.7	mA
Peak of Bluetooth receiver	18.5	10	7.9	mA

4 Chip Function Description

4.1 Radio Transceiver

The Radio Transceiver implements the RF part of the Bluetooth Low Energy protocol. Together with the Bluetooth 4.2 PHY layer, this provides a reliable wireless communication. All RF blocks are supplied by on-chip low-drop out-regulators (LDO's). The Bluetooth LE radio comprises the Receiver, Transmitter, Synthesizer, Rx/Tx combiner block, and Biasing LDO's.

4.1.1 Bluetooth Radio Receiver

The HS6620D receiver is a low IF down conversion architecture. The RF signal passes first through an integrated transformer, which is shared between receiver and transmitter. The transformer drives a differential variable-gain LNA, which amplifies the signal before it passes through a low-IF down conversion mixer stage. Following the mixer is a third-order complex BPF, which performs channel selection and image rejection. The IF signal is then digitized by two noise-shaping SAR ADCs before further signal processing in the digital domain.

4.1.2 Bluetooth Radio Transmitter

The HS6620D transmitter is a direct modulating architecture. The digital baseband signals directly modulate VCO and divider of PLL, which is called two-point modulation. After a 3-stage B-class power amplifier, the radio signal is output through antenna.

4.1.3 Frequency Synthesizer

The HS6620D Frequency synthesizer is fully integrated sigma delta fractional-N PLL to lock the VCO to a reference crystal oscillator. The synthesizer uses a number of integrated linear regulators for better isolation to the blocks respectively.

4.2 Bluetooth Baseband Unit

The BLE (Bluetooth Low Energy) core is a qualified Bluetooth 4.2 baseband controller compatible with

Bluetooth Smart specification and it is in charge of packet encoding/decoding and frame scheduling.

Features:

- All device classes support (Broadcaster, Central, Observer, Peripheral)
- All packet types (Advertising / Data / Control)
- Encryption (AES / CCM)
- Bit stream processing (CRC, Whitening)
- Frequency Hopping calculation
- Low power modes supporting 32.768kHz

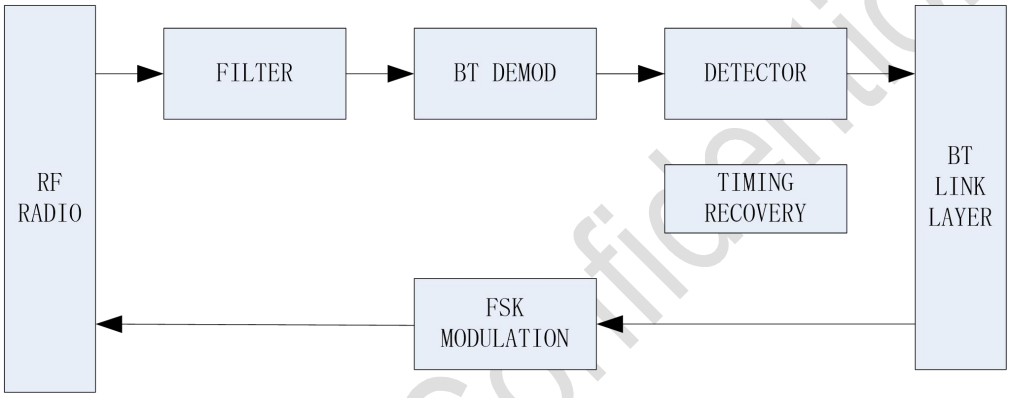

Figure 4 HS6620D BT Baseband

4.3 Peripherals

4.3.1 SPI

The Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. The HS6620D integrate 2 SPI interfaces, they can work in either master or slave mode and also support DMA or software mode to transfer data.

The master or slave controller only support point to point connection by hardware, that is, both the SPI interface has only one CS pin. The connection is shown below the figure:

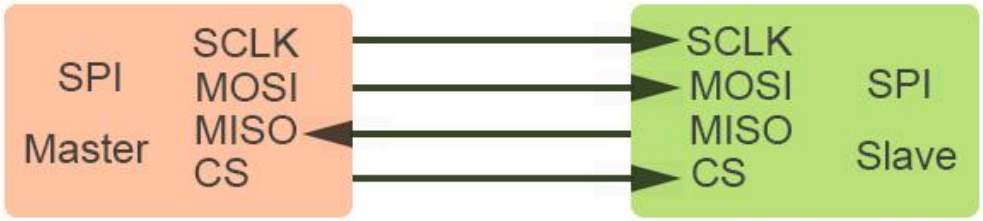

Figure 5 HS6620D SPI interconnection

The SPI Interface provides much flexibility that can fit most SPI slave devices. The polarity and phase of SCK can be both programmed and results in four combinations. The CS to SCK delay, the SCK to NCS delay, and SCK period are also programmed. The timing relationships of SPI Interface are illustrated below.

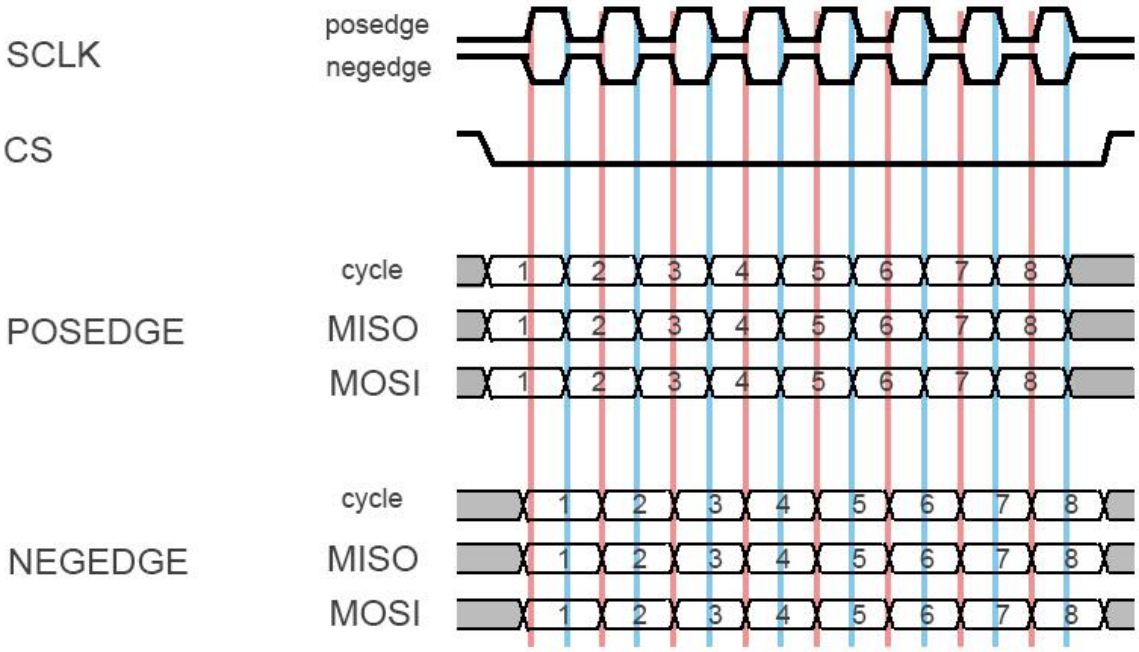

Figure 6 HS6620D SPI interface timing

4.3.2 UART

The UART is modeled after the industry-standard 16550. However, the register address space has been relocated to 32-bit data boundaries for APB bus implementation.

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and

interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled or disabled by the control registers.

HS6620D has 2 UART; the UART0 is a common 2 wire (transmitter and receiver) controller, and the UART1 support stream control (CTS/RTS). UART1 also supports ISO7816 protocols.

4.3.3 I2C

The I2C is a master or slave interface. It supports 100, 400 and 800 KHz clock rates for controlling EEPROM and etc. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs. The I2C support DMA operation for extra MCU free data transfer. The I2C work as ether master or slave, but cannot change the working mode after configuration.

The module is shown as below:

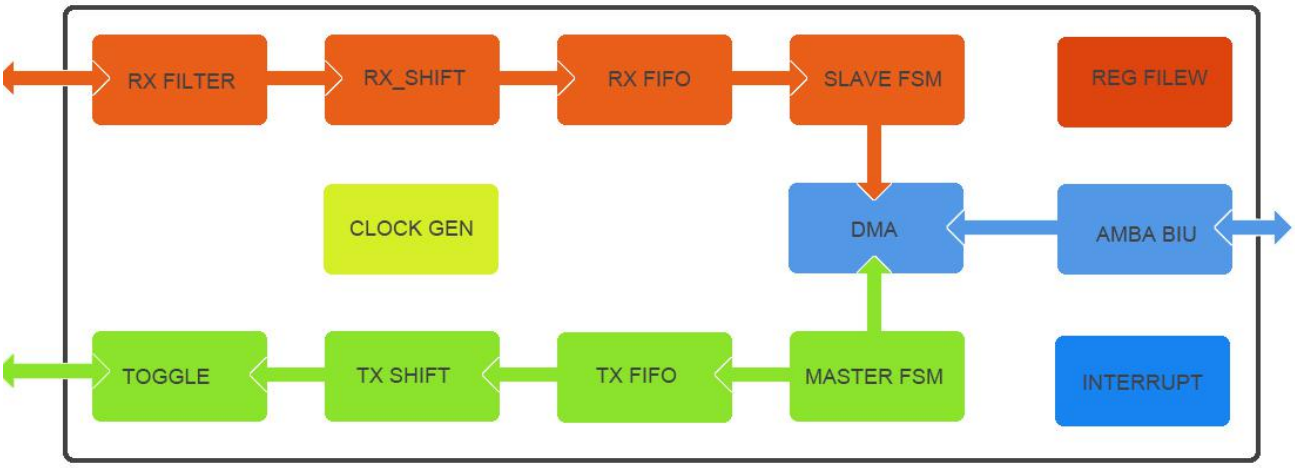

Figure 7 HS6620D I2C block digaram

4.3.4 Timer

The Timer includes three identical 32-bit Timer Counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

4.3.5 GPIO

The HS6620D has up to 31 software-configurable I/O pins.

Features:

- Fully programmable pin assignment

- Selectable pull-up, pull-down resistors per pin
- GPIO[7:0] ability to be configured as GP-ADC input
- Pins retain their last state when system enters the sleep mode
- Ability to wakeup chip by any GPIOs in sleep mode

4.3.6 I2S interface

The I2S have three wires: serial data, word select and serial clock and this interface is used for audio data transfer. The HS6620D I2S interface supports both master and slave mode and is used for transmit only. The I2S supports the standard I2S frame format for transmitting data.

4.3.7 Quadrature Decoders

This block decodes the pulse trains from a rotary encoder to provide the step and the direction of the movement of an external device. Three axes (X, Y, Z) are supported.

The integrated quadrature decoder can automatically decode the signals for the X, Y and Z axes of a HID input device, reporting step count and direction: the channels are expected to provide a pulse train with 90 degrees phase difference; depending on whether the reference channel is leading or lagging, the direction can be determined.

This block can be used for waking up the chip as soon as there is any kind of movement from the external device connected to it.

4.3.8 Keyboard Controller

The keyboard controller can be used for debouncing the incoming GPIO signals when implementing a keyboard scanning engine. It generates an interrupt to the CPU.

Features:

- Generates a keyboard interrupt on key press or key release
- Implements debouncing time up to 31 ms

4.3.9 General Purpose (GP) ADC

The HS6620D is equipped with a high-speed low power 12-bit general purpose Analog-to-Digital Converter (GPADC). It can operate in unipolar (single ended) mode as well as in bipolar (differential) mode.

The ADC has its own voltage regulator (LDO) of 1.2 V, which represents the full scale reference voltage.

Features:

- 12-bit dynamic ADC with 65 ns conversion time
- Maximum sampling rate 3.3M sample/s
- Ultra-low power (5 μA typical supply current at 100k sample/s)
- Single-ended as well as differential input with two input scales
- Eight single-ended or four differential external input channels
- Battery monitoring function
- Chopper function
- Offset and zero scale adjust
- Common-mode input level adjust

4.4 Power Management

HS6620D integrates a Power Management Unit (PMU), and a battery charger.

4.4.1 Power Management (PMU)

There are four different power modes in the HS6620D:

- *Active Mode: System is active and operates at full speed.*
- Sleep Mode: No power gating has been programmed; the CPU is idle, waiting for an interrupt. 24M crystal is on, 32K crystal is on. Peripherals is depending on the programmed enabled value.
- Extended Sleep Mode: All power domains are off except for the always on power domain, the programmed Bluetooth timer module, 24M crystal is off, 32K crystal is on. The data retention SRAM retains its data and other SRAM is power off. It is wake by timer or GPIOs.
- Deep Sleep Mode: All power domains are off except for the always on power domain, and all clocks are off. This mode dissipates the minimum leakage power. It is wake only by GOIOs in this mode.

4.4.2 Battery Charger

When Charger circuit is enabled, it will detect the battery voltage and enters the associated mode to charge the battery, i.e. Trickle, CC or CV mode. When the battery voltage reaches a high threshold, the charger will enter standby mode and keep monitoring the battery voltage. If the battery voltage drops to a lower threshold, charger circuit will re-charge the battery again.

5 Software

5.1 Protocol Stack

The HS6620D Software platform includes a qualified Bluetooth Smart single-mode stack on chip. Numerous Bluetooth Smart profiles for consumer wellness, sport, fitness, and security and proximity applications are supplied as standard, while additional customer profiles can be developed and added as needed.

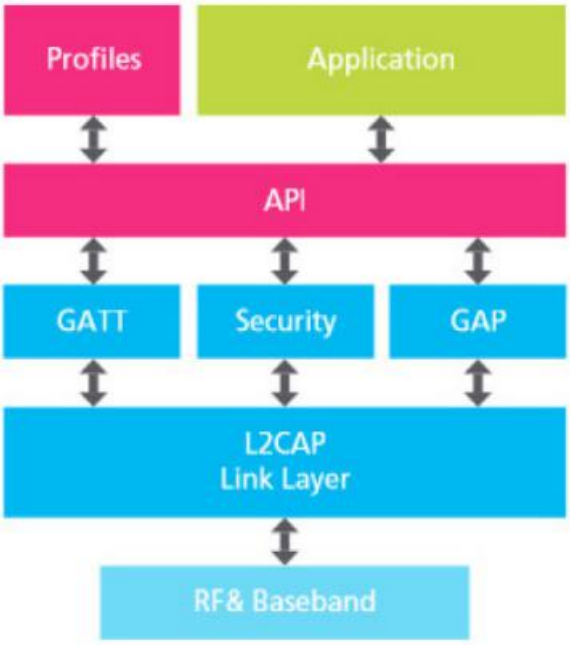

Figure 8 HS6620D software stack

Apart from the protocol stack, the Software platform supports a Hardware Abstraction Layer (HAL) which enables easy access to peripheral's features from a programmer's point of view as presented in the following figure.

Core drivers are provided for each interface of the HS6620D enabling optimized usage of the hardware's capabilities. These drivers are providing an easy to use interface towards the hardware engines without having to interfere with the register programming directly.

On top of the core drivers, a number of sample drivers *are also provided enabling communication with basic Bluetooth applications components: accelerometers, FLASH/EEPROM nonvolatile memories etc.*

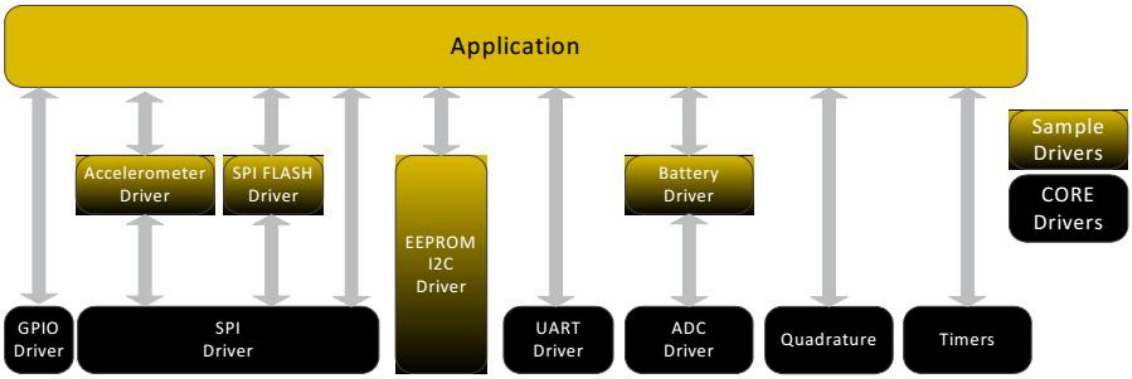

Figure 9 HS6620D Hardware Driver and Application

6 Package Information

6.1 Package Information

The HS6620D has QFN48 package, the information is as below:

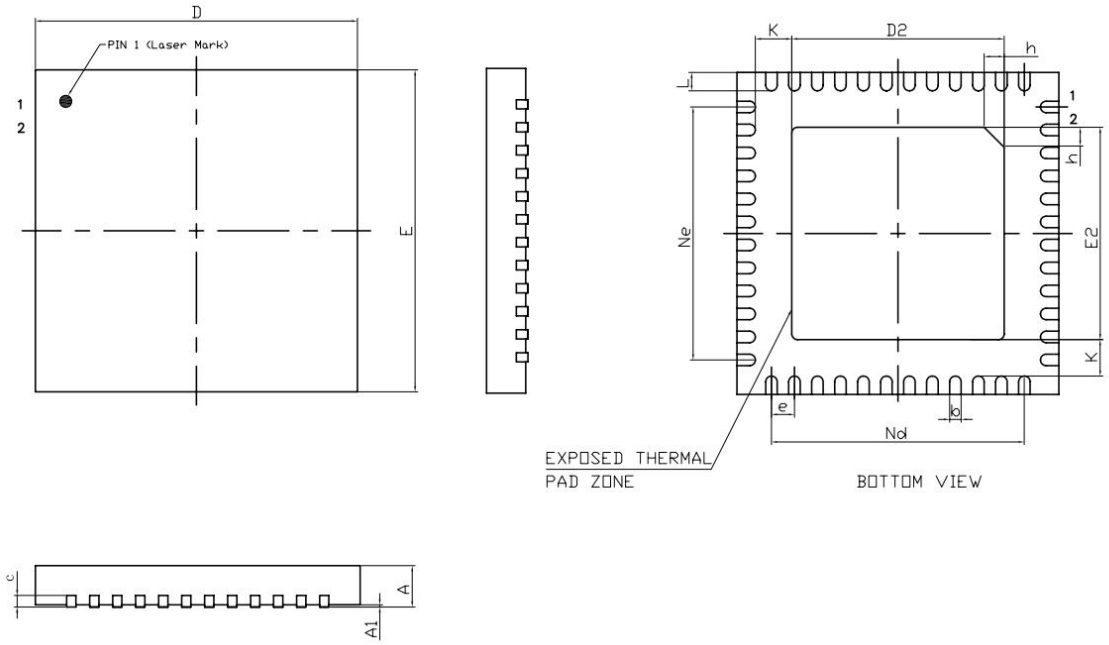

Figure 10 HS6620D QFN48 package

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.70	3.80	3.90
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	3.70	3.80	3.90
K	0.20	--	--
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	161*161		

Table 7 HS6620D QFN package

7 Application Circuit

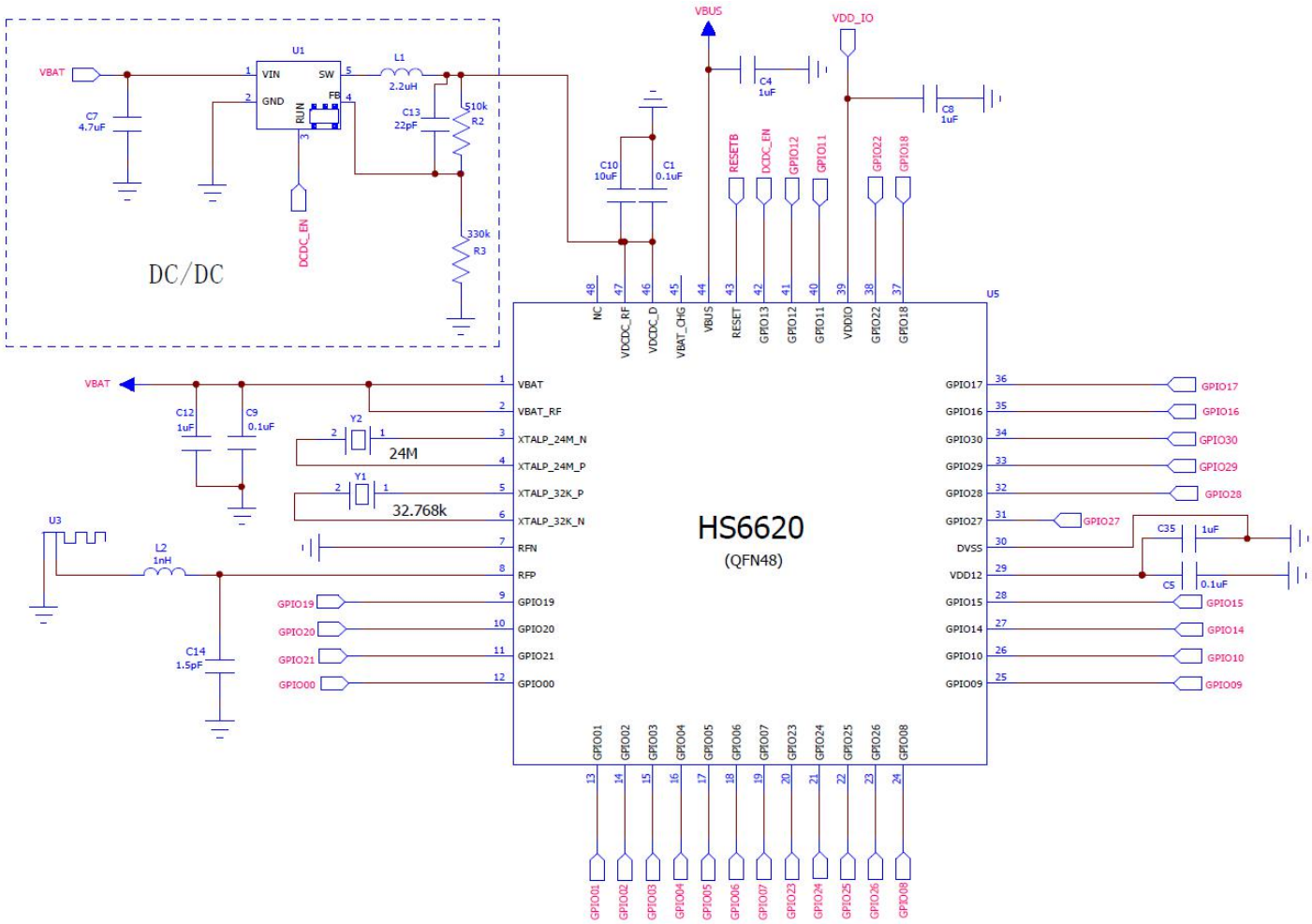

Figure 11 HS6620D application circuit