Sitronix

ST7586S

16-Level Gray Scale Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7586S is a driver & controller LSI for 16-level gray scale graphic dot-matrix liquid crystal display systems. It contains 384-segment and 160-common driver circuits. This chip can be connected directly to a microprocessor which accepts 8-bit parallel interface (8080-series or 6800-series type), 4-Line serial interface or 3-Line serial interface. Display data is stored into an on-chip Display Data RAM (DDRAM). It performs the Display Data RAM read/write operation without external operating clock, and the power consumption can be minimized. In addition, since all necessary power supply circuits for LCD system are built-in, ST7586S constructs a LCD display system with the fewest components.

FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

♦ 384 segment outputs / 160 common outputs

On-chip Display Data RAM

♦ Capacity: 384 x 160 x 4 = 245,760 bits

Various Partial Display Features

♦ Applicable partial duty

♦ Partial window moving & data scrolling

Microprocessor Interface

♦ 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU

♦ 4-Line serial interface

♦ 3-Line (9-bit) serial interface

On-chip Low Power Analog Circuit

♦ On-chip oscillator circuit

♦ Voltage booster with built-in boost-capacitors

♦ Extremely few external components: 4 capacitors

♦ Built-in voltage regulator with programmable contrast

♦ Built-in voltage follower supports LCD bias voltage Available bias: 1/9 ~ 1/14

Operating Voltage Range

♦ Digital Power (VDD1): 1.8V ~ 3.3V (TYP.)

♦ Analog Power (VDD2~VDD5, VDDX): 2.8V ~ 3.3V (TYP.)

♦ LCD operation voltage (Vop = V0-XV0) : 18V

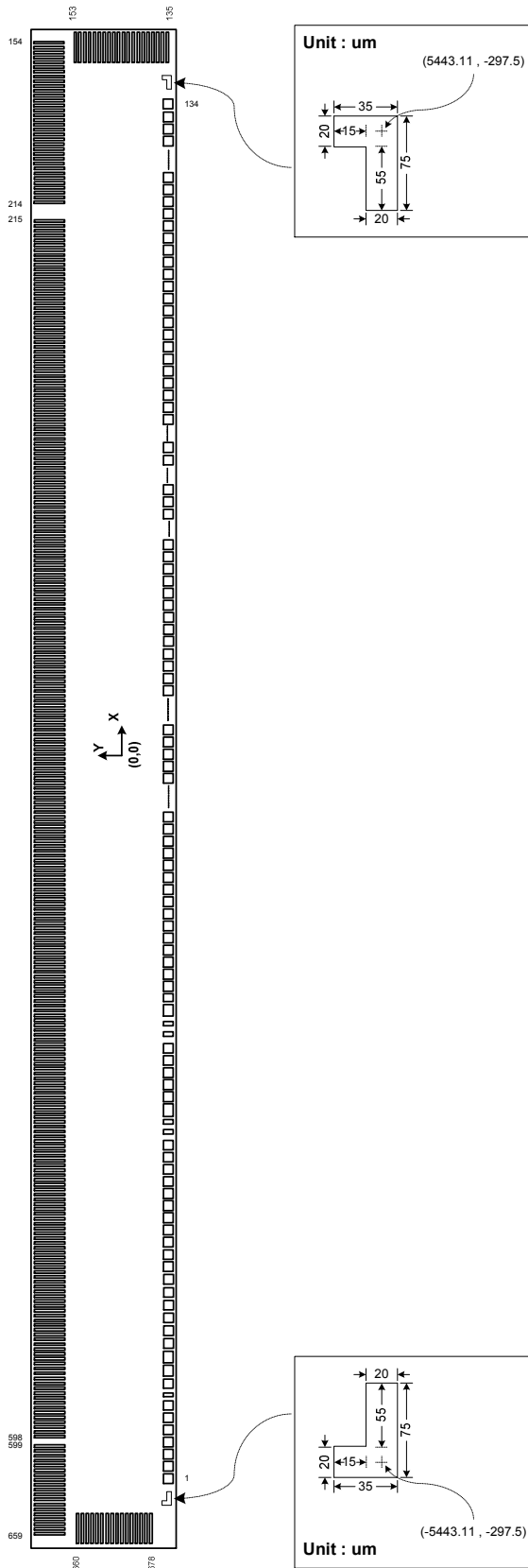**Built-in OTP–ROM for LCD Vop Optimization**

Package Type: COG

ST7586S	6800, 8080, 4-Line & 3-Line Interface	ST

ST7586S

PAD ARRANGEMENT

Unit: um

Part Number	ST7586S-G4	Chip Size	11434 x 701
Chip Thickness	300	Bump Height	15
Bump		**Bump Size**	
10, 11, 31, 39		105 x 63	
8, 29, 30, 37, 38		25 x 63	
1~7, 9, 12~28, 32~36, 40~134		65 x 63	
135~153, 660~678		149.4 x 10.5	
154~659		10.5 x 149.4	
* Refer to "PAD CENTER COORDINATES" for ITO layout			

PAD CENTER COORDINATES

PAD	NAME	X	Y		PAD	NAME	X	Y
1	VSS1	-5300	-283		47	VDD1	-1660	-283
2	VPP	-5220	-283		48	VDD1	-1580	-283
3	VPP	-5140	-283		49	VD1I	-1500	-283
4	VPP	-5060	-283		50	VD1I	-1420	-283
5	VPP	-4980	-283		51	VD1I	-1340	-283
6	CL	-4900	-283		52	VD1I	-1260	-283
7	CLS	-4820	-283		53	VD1O	-1180	-283
8	VDD1	-4760	-283		54	VD1O	-1100	-283
9	VD1S	-4700	-283		55	VSS1	-1020	-283
10	A0	-4600	-283		56	VSS1	-940	-283
11	RWR	-4480	-283		57	VSS1	-860	-283
12	D0	-4380	-283		58	VSS1	-780	-283
13	DUMMY	-4300	-283		59	VSS1	-700	-283
14	D1	-4220	-283		60	VSS1	-620	-283
15	D2	-4140	-283		61	VSSX	-540	-283
16	D3	-4060	-283		62	VSSX	-460	-283
17	D4	-3980	-283		63	VSS2	-380	-283
18	D5	-3900	-283		64	VSS2	-300	-283
19	D6	-3820	-283		65	VSS2	-220	-283
20	D7	-3740	-283		66	VSS2	-140	-283
21	Reserved	-3660	-283		67	VSS2	-60	-283
22	Reserved	-3580	-283		68	VSS2	20	-283
23	Reserved	-3500	-283		69	VSS2	100	-283
24	Reserved	-3420	-283		70	VSS2	180	-283
25	Reserved	-3340	-283		71	VSS2	260	-283
26	Reserved	-3260	-283		72	VSS2	340	-283
27	Reserved	-3180	-283		73	VSS2	420	-283
28	Reserved	-3100	-283		74	VSS2	500	-283
29	VSS1	-3040	-283		75	VSS4	580	-283
30	VDD1	-3000	-283		76	VSS4	660	-283
31	ERD	-2920	-283		77	VSS4	740	-283
32	RSTB	-2820	-283		78	VDDX	820	-283
33	DUMMY	-2740	-283		79	VDDX	900	-283
34	IF1	-2660	-283		80	VDD3	980	-283
35	IF2	-2580	-283		81	VDD3	1060	-283
36	IF3	-2500	-283		82	VDD4	1140	-283
37	VSS1	-2440	-283		83	VDD4	1220	-283
38	VDD1	-2400	-283		84	VDD4	1300	-283
39	CSB	-2320	-283		85	VDD5	1380	-283
40	EXTB	-2220	-283		86	VDD5	1460	-283
41	TE	-2140	-283		87	VDD5	1540	-283
42	TCAP	-2060	-283		88	VDD5	1620	-283
43	VDD1	-1980	-283		89	VDD5	1700	-283
44	VDD1	-1900	-283		90	VDD5	1780	-283
45	VDD1	-1820	-283		91	VDD5	1860	-283
46	VDD1	-1740	-283		92	VDD5	1940	-283

PAD	NAME	X	Y		PAD	NAME	X	Y
93	VDD2	2020	-283		141	COM13	5606.5	-152.5
94	VDD2	2100	-283		142	COM15	5606.5	-130.5
95	VDD2	2180	-283		143	COM17	5606.5	-108.5
96	VDD2	2260	-283		144	COM19	5606.5	-86.5
97	VDD2	2340	-283		145	COM21	5606.5	-64.5
98	VDD2	2420	-283		146	COM23	5606.5	-42.5
99	VDD2	2500	-283		147	COM25	5606.5	-20.5
100	VDD2	2580	-283		148	COM27	5606.5	1.5
101	VDD2	2660	-283		149	COM29	5606.5	23.5
102	VDD2	2740	-283		150	COM31	5606.5	45.5
103	VM	2820	-283		151	COM33	5606.5	67.5
104	VM	2900	-283		152	COM35	5606.5	89.5
105	VM	2980	-283		153	COM37	5606.5	111.5
106	VM	3060	-283		154	COM39	5649.33	240
107	VM	3140	-283		155	COM41	5627.33	240
108	VM	3220	-283		156	COM43	5605.33	240
109	VM	3300	-283		157	COM45	5583.33	240
110	VREF	3380	-283		158	COM47	5561.33	240
111	V0I	3460	-283		159	COM49	5539.33	240
112	V0I	3540	-283		160	COM51	5517.33	240
113	V0I	3620	-283		161	COM53	5495.33	240
114	V0I	3700	-283		162	COM55	5473.33	240
115	V0S	3780	-283		163	COM57	5451.33	240
116	V0O	3860	-283		164	COM59	5429.33	240
117	V0O	3940	-283		165	COM61	5407.33	240
118	XV0O	4020	-283		166	COM63	5385.33	240
119	XV0O	4100	-283		167	COM65	5363.33	240
120	XV0S	4180	-283		168	COM67	5341.33	240
121	XV0I	4260	-283		169	COM69	5319.33	240
122	XV0I	4340	-283		170	COM71	5297.33	240
123	XV0I	4420	-283		171	COM73	5275.33	240
124	XV0I	4500	-283		172	COM75	5253.33	240
125	VGO	4580	-283		173	COM77	5231.33	240
126	VGO	4660	-283		174	COM79	5209.33	240
127	VGS	4740	-283		175	COM81	5187.33	240
128	VGI	4820	-283		176	COM83	5165.33	240
129	VGI	4900	-283		177	COM85	5143.33	240
130	VGI	4980	-283		178	COM87	5121.33	240
131	VGI	5060	-283		179	COM89	5099.33	240
132	VGI	5140	-283		180	COM91	5077.33	240
133	VGI	5220	-283		181	COM93	5055.33	240
134	VSS1	5300	-283		182	COM95	5033.33	240
135	COM1	5606.5	-284.5		183	COM97	5011.33	240
136	COM3	5606.5	-262.5		184	COM99	4989.33	240
137	COM5	5606.5	-240.5		185	COM101	4967.33	240
138	COM7	5606.5	-218.5		186	COM103	4945.33	240
139	COM9	5606.5	-196.5		187	COM105	4923.33	240
140	COM11	5606.5	-174.5		188	COM107	4901.33	240

PAD	NAME	X	Y		PAD	NAME	X	Y
189	COM109	4879.33	240		237	SEG22	3729	240
190	COM111	4857.33	240		238	SEG23	3707	240
191	COM113	4835.33	240		239	SEG24	3685	240
192	COM115	4813.33	240		240	SEG25	3663	240
193	COM117	4791.33	240		241	SEG26	3641	240
194	COM119	4769.33	240		242	SEG27	3619	240
195	COM121	4747.33	240		243	SEG28	3597	240
196	COM123	4725.33	240		244	SEG29	3575	240
197	COM125	4703.33	240		245	SEG30	3553	240
198	COM127	4681.33	240		246	SEG31	3531	240
199	COM129	4659.33	240		247	SEG32	3509	240
200	COM131	4637.33	240		248	SEG33	3487	240
201	COM133	4615.33	240		249	SEG34	3465	240
202	COM135	4593.33	240		250	SEG35	3443	240
203	COM137	4571.33	240		251	SEG36	3421	240
204	COM139	4549.33	240		252	SEG37	3399	240
205	COM141	4527.33	240		253	SEG38	3377	240
206	COM143	4505.33	240		254	SEG39	3355	240
207	COM145	4483.33	240		255	SEG40	3333	240
208	COM147	4461.33	240		256	SEG41	3311	240
209	COM149	4439.33	240		257	SEG42	3289	240
210	COM151	4417.33	240		258	SEG43	3267	240
211	COM153	4395.33	240		259	SEG44	3245	240
212	COM155	4373.33	240		260	SEG45	3223	240
213	COM157	4351.33	240		261	SEG46	3201	240
214	COM159	4329.33	240		262	SEG47	3179	240
215	SEG0	4213	240		263	SEG48	3157	240
216	SEG1	4191	240		264	SEG49	3135	240
217	SEG2	4169	240		265	SEG50	3113	240
218	SEG3	4147	240		266	SEG51	3091	240
219	SEG4	4125	240		267	SEG52	3069	240
220	SEG5	4103	240		268	SEG53	3047	240
221	SEG6	4081	240		269	SEG54	3025	240
222	SEG7	4059	240		270	SEG55	3003	240
223	SEG8	4037	240		271	SEG56	2981	240
224	SEG9	4015	240		272	SEG57	2959	240
225	SEG10	3993	240		273	SEG58	2937	240
226	SEG11	3971	240		274	SEG59	2915	240
227	SEG12	3949	240		275	SEG60	2893	240
228	SEG13	3927	240		276	SEG61	2871	240
229	SEG14	3905	240		277	SEG62	2849	240
230	SEG15	3883	240		278	SEG63	2827	240
231	SEG16	3861	240		279	SEG64	2805	240
232	SEG17	3839	240		280	SEG65	2783	240
233	SEG18	3817	240		281	SEG66	2761	240
234	SEG19	3795	240		282	SEG67	2739	240
235	SEG20	3773	240		283	SEG68	2717	240
236	SEG21	3751	240		284	SEG69	2695	240

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PAD	NAME	X	Y		PAD	NAME	X	Y
285	SEG70	2673	240		333	SEG118	1617	240
286	SEG71	2651	240		334	SEG119	1595	240
287	SEG72	2629	240		335	SEG120	1573	240
288	SEG73	2607	240		336	SEG121	1551	240
289	SEG74	2585	240		337	SEG122	1529	240
290	SEG75	2563	240		338	SEG123	1507	240
291	SEG76	2541	240		339	SEG124	1485	240
292	SEG77	2519	240		340	SEG125	1463	240
293	SEG78	2497	240		341	SEG126	1441	240
294	SEG79	2475	240		342	SEG127	1419	240
295	SEG80	2453	240		343	SEG128	1397	240
296	SEG81	2431	240		344	SEG129	1375	240
297	SEG82	2409	240		345	SEG130	1353	240
298	SEG83	2387	240		346	SEG131	1331	240
299	SEG84	2365	240		347	SEG132	1309	240
300	SEG85	2343	240		348	SEG133	1287	240
301	SEG86	2321	240		349	SEG134	1265	240
302	SEG87	2299	240		350	SEG135	1243	240
303	SEG88	2277	240		351	SEG136	1221	240
304	SEG89	2255	240		352	SEG137	1199	240
305	SEG90	2233	240		353	SEG138	1177	240
306	SEG91	2211	240		354	SEG139	1155	240
307	SEG92	2189	240		355	SEG140	1133	240
308	SEG93	2167	240		356	SEG141	1111	240
309	SEG94	2145	240		357	SEG142	1089	240
310	SEG95	2123	240		358	SEG143	1067	240
311	SEG96	2101	240		359	SEG144	1045	240
312	SEG97	2079	240		360	SEG145	1023	240
313	SEG98	2057	240		361	SEG146	1001	240
314	SEG99	2035	240		362	SEG147	979	240
315	SEG100	2013	240		363	SEG148	957	240
316	SEG101	1991	240		364	SEG149	935	240
317	SEG102	1969	240		365	SEG150	913	240
318	SEG103	1947	240		366	SEG151	891	240
319	SEG104	1925	240		367	SEG152	869	240
320	SEG105	1903	240		368	SEG153	847	240
321	SEG106	1881	240		369	SEG154	825	240
322	SEG107	1859	240		370	SEG155	803	240
323	SEG108	1837	240		371	SEG156	781	240
324	SEG109	1815	240		372	SEG157	759	240
325	SEG110	1793	240		373	SEG158	737	240
326	SEG111	1771	240		374	SEG159	715	240
327	SEG112	1749	240		375	SEG160	693	240
328	SEG113	1727	240		376	SEG161	671	240
329	SEG114	1705	240		377	SEG162	649	240
330	SEG115	1683	240		378	SEG163	627	240
331	SEG116	1661	240		379	SEG164	605	240
332	SEG117	1639	240		380	SEG165	583	240

PAD	NAME	X	Y		PAD	NAME	X	Y
381	SEG166	561	240		429	SEG214	-495	240
382	SEG167	539	240		430	SEG215	-517	240
383	SEG168	517	240		431	SEG216	-539	240
384	SEG169	495	240		432	SEG217	-561	240
385	SEG170	473	240		433	SEG218	-583	240
386	SEG171	451	240		434	SEG219	-605	240
387	SEG172	429	240		435	SEG220	-627	240
388	SEG173	407	240		436	SEG221	-649	240
389	SEG174	385	240		437	SEG222	-671	240
390	SEG175	363	240		438	SEG223	-693	240
391	SEG176	341	240		439	SEG224	-715	240
392	SEG177	319	240		440	SEG225	-737	240
393	SEG178	297	240		441	SEG226	-759	240
394	SEG179	275	240		442	SEG227	-781	240
395	SEG180	253	240		443	SEG228	-803	240
396	SEG181	231	240		444	SEG229	-825	240
397	SEG182	209	240		445	SEG230	-847	240
398	SEG183	187	240		446	SEG231	-869	240
399	SEG184	165	240		447	SEG232	-891	240
400	SEG185	143	240		448	SEG233	-913	240
401	SEG186	121	240		449	SEG234	-935	240
402	SEG187	99	240		450	SEG235	-957	240
403	SEG188	77	240		451	SEG236	-979	240
404	SEG189	55	240		452	SEG237	-1001	240
405	SEG190	33	240		453	SEG238	-1023	240
406	SEG191	11	240		454	SEG239	-1045	240
407	SEG192	-11	240		455	SEG240	-1067	240
408	SEG193	-33	240		456	SEG241	-1089	240
409	SEG194	-55	240		457	SEG242	-1111	240
410	SEG195	-77	240		458	SEG243	-1133	240
411	SEG196	-99	240		459	SEG244	-1155	240
412	SEG197	-121	240		460	SEG245	-1177	240
413	SEG198	-143	240		461	SEG246	-1199	240
414	SEG199	-165	240		462	SEG247	-1221	240
415	SEG200	-187	240		463	SEG248	-1243	240
416	SEG201	-209	240		464	SEG249	-1265	240
417	SEG202	-231	240		465	SEG250	-1287	240
418	SEG203	-253	240		466	SEG251	-1309	240
419	SEG204	-275	240		467	SEG252	-1331	240
420	SEG205	-297	240		468	SEG253	-1353	240
421	SEG206	-319	240		469	SEG254	-1375	240
422	SEG207	-341	240		470	SEG255	-1397	240
423	SEG208	-363	240		471	SEG256	-1419	240
424	SEG209	-385	240		472	SEG257	-1441	240
425	SEG210	-407	240		473	SEG258	-1463	240
426	SEG211	-429	240		474	SEG259	-1485	240
427	SEG212	-451	240		475	SEG260	-1507	240
428	SEG213	-473	240		476	SEG261	-1529	240

PAD	NAME	X	Y		PAD	NAME	X	Y
477	SEG262	-1551	240		525	SEG310	-2607	240
478	SEG263	-1573	240		526	SEG311	-2629	240
479	SEG264	-1595	240		527	SEG312	-2651	240
480	SEG265	-1617	240		528	SEG313	-2673	240
481	SEG266	-1639	240		529	SEG314	-2695	240
482	SEG267	-1661	240		530	SEG315	-2717	240
483	SEG268	-1683	240		531	SEG316	-2739	240
484	SEG269	-1705	240		532	SEG317	-2761	240
485	SEG270	-1727	240		533	SEG318	-2783	240
486	SEG271	-1749	240		534	SEG319	-2805	240
487	SEG272	-1771	240		535	SEG320	-2827	240
488	SEG273	-1793	240		536	SEG321	-2849	240
489	SEG274	-1815	240		537	SEG322	-2871	240
490	SEG275	-1837	240		538	SEG323	-2893	240
491	SEG276	-1859	240		539	SEG324	-2915	240
492	SEG277	-1881	240		540	SEG325	-2937	240
493	SEG278	-1903	240		541	SEG326	-2959	240
494	SEG279	-1925	240		542	SEG327	-2981	240
495	SEG280	-1947	240		543	SEG328	-3003	240
496	SEG281	-1969	240		544	SEG329	-3025	240
497	SEG282	-1991	240		545	SEG330	-3047	240
498	SEG283	-2013	240		546	SEG331	-3069	240
499	SEG284	-2035	240		547	SEG332	-3091	240
500	SEG285	-2057	240		548	SEG333	-3113	240
501	SEG286	-2079	240		549	SEG334	-3135	240
502	SEG287	-2101	240		550	SEG335	-3157	240
503	SEG288	-2123	240		551	SEG336	-3179	240
504	SEG289	-2145	240		552	SEG337	-3201	240
505	SEG290	-2167	240		553	SEG338	-3223	240
506	SEG291	-2189	240		554	SEG339	-3245	240
507	SEG292	-2211	240		555	SEG340	-3267	240
508	SEG293	-2233	240		556	SEG341	-3289	240
509	SEG294	-2255	240		557	SEG342	-3311	240
510	SEG295	-2277	240		558	SEG343	-3333	240
511	SEG296	-2299	240		559	SEG344	-3355	240
512	SEG297	-2321	240		560	SEG345	-3377	240
513	SEG298	-2343	240		561	SEG346	-3399	240
514	SEG299	-2365	240		562	SEG347	-3421	240
515	SEG300	-2387	240		563	SEG348	-3443	240
516	SEG301	-2409	240		564	SEG349	-3465	240
517	SEG302	-2431	240		565	SEG350	-3487	240
518	SEG303	-2453	240		566	SEG351	-3509	240
519	SEG304	-2475	240		567	SEG352	-3531	240
520	SEG305	-2497	240		568	SEG353	-3553	240
521	SEG306	-2519	240		569	SEG354	-3575	240
522	SEG307	-2541	240		570	SEG355	-3597	240
523	SEG308	-2563	240		571	SEG356	-3619	240
524	SEG309	-2585	240		572	SEG357	-3641	240

PAD	NAME	X	Y		PAD	NAME	X	Y
573	SEG358	-3663	240		621	COM114	-4813.33	240
574	SEG359	-3685	240		622	COM112	-4835.33	240
575	SEG360	-3707	240		623	COM110	-4857.33	240
576	SEG361	-3729	240		624	COM108	-4879.33	240
577	SEG362	-3751	240		625	COM106	-4901.33	240
578	SEG363	-3773	240		626	COM104	-4923.33	240
579	SEG364	-3795	240		627	COM102	-4945.33	240
580	SEG365	-3817	240		628	COM100	-4967.33	240
581	SEG366	-3839	240		629	COM98	-4989.33	240
582	SEG367	-3861	240		630	COM96	-5011.33	240
583	SEG368	-3883	240		631	COM94	-5033.33	240
584	SEG369	-3905	240		632	COM92	-5055.33	240
585	SEG370	-3927	240		633	COM90	-5077.33	240
586	SEG371	-3949	240		634	COM88	-5099.33	240
587	SEG372	-3971	240		635	COM86	-5121.33	240
588	SEG373	-3993	240		636	COM84	-5143.33	240
589	SEG374	-4015	240		637	COM82	-5165.33	240
590	SEG375	-4037	240		638	COM80	-5187.33	240
591	SEG376	-4059	240		639	COM78	-5209.33	240
592	SEG377	-4081	240		640	COM76	-5231.33	240
593	SEG378	-4103	240		641	COM74	-5253.33	240
594	SEG379	-4125	240		642	COM72	-5275.33	240
595	SEG380	-4147	240		643	COM70	-5297.33	240
596	SEG381	-4169	240		644	COM68	-5319.33	240
597	SEG382	-4191	240		645	COM66	-5341.33	240
598	SEG383	-4213	240		646	COM64	-5363.33	240
599	COM158	-4329.33	240		647	COM62	-5385.33	240
600	COM156	-4351.33	240		648	COM60	-5407.33	240
601	COM154	-4373.33	240		649	COM58	-5429.33	240
602	COM152	-4395.33	240		650	COM56	-5451.33	240
603	COM150	-4417.33	240		651	COM54	-5473.33	240
604	COM148	-4439.33	240		652	COM52	-5495.33	240
605	COM146	-4461.33	240		653	COM50	-5517.33	240
606	COM144	-4483.33	240		654	COM48	-5539.33	240
607	COM142	-4505.33	240		655	COM46	-5561.33	240
608	COM140	-4527.33	240		656	COM44	-5583.33	240
609	COM138	-4549.33	240		657	COM42	-5605.33	240
610	COM136	-4571.33	240		658	COM40	-5627.33	240
611	COM134	-4593.33	240		659	COM38	-5649.33	240
612	COM132	-4615.33	240		660	COM36	-5606.5	111.5
613	COM130	-4637.33	240		661	COM34	-5606.5	89.5
614	COM128	-4659.33	240		662	COM32	-5606.5	67.5
615	COM126	-4681.33	240		663	COM30	-5606.5	45.5
616	COM124	-4703.33	240		664	COM28	-5606.5	23.5
617	COM122	-4725.33	240		665	COM26	-5606.5	1.5
618	COM120	-4747.33	240		666	COM24	-5606.5	-20.5
619	COM118	-4769.33	240		667	COM22	-5606.5	-42.5
620	COM116	-4791.33	240		668	COM20	-5606.5	-64.5

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PAD	NAME	X	Y
669	COM18	-5606.5	-86.5
670	COM16	-5606.5	-108.5
671	COM14	-5606.5	-130.5
672	COM12	-5606.5	-152.5
673	COM10	-5606.5	-174.5
674	COM8	-5606.5	-196.5
675	COM6	-5606.5	-218.5
676	COM4	-5606.5	-240.5
677	COM2	-5606.5	-262.5
678	COM0	-5606.5	-284.5

Unit : um

BLOCK DIAGRAM
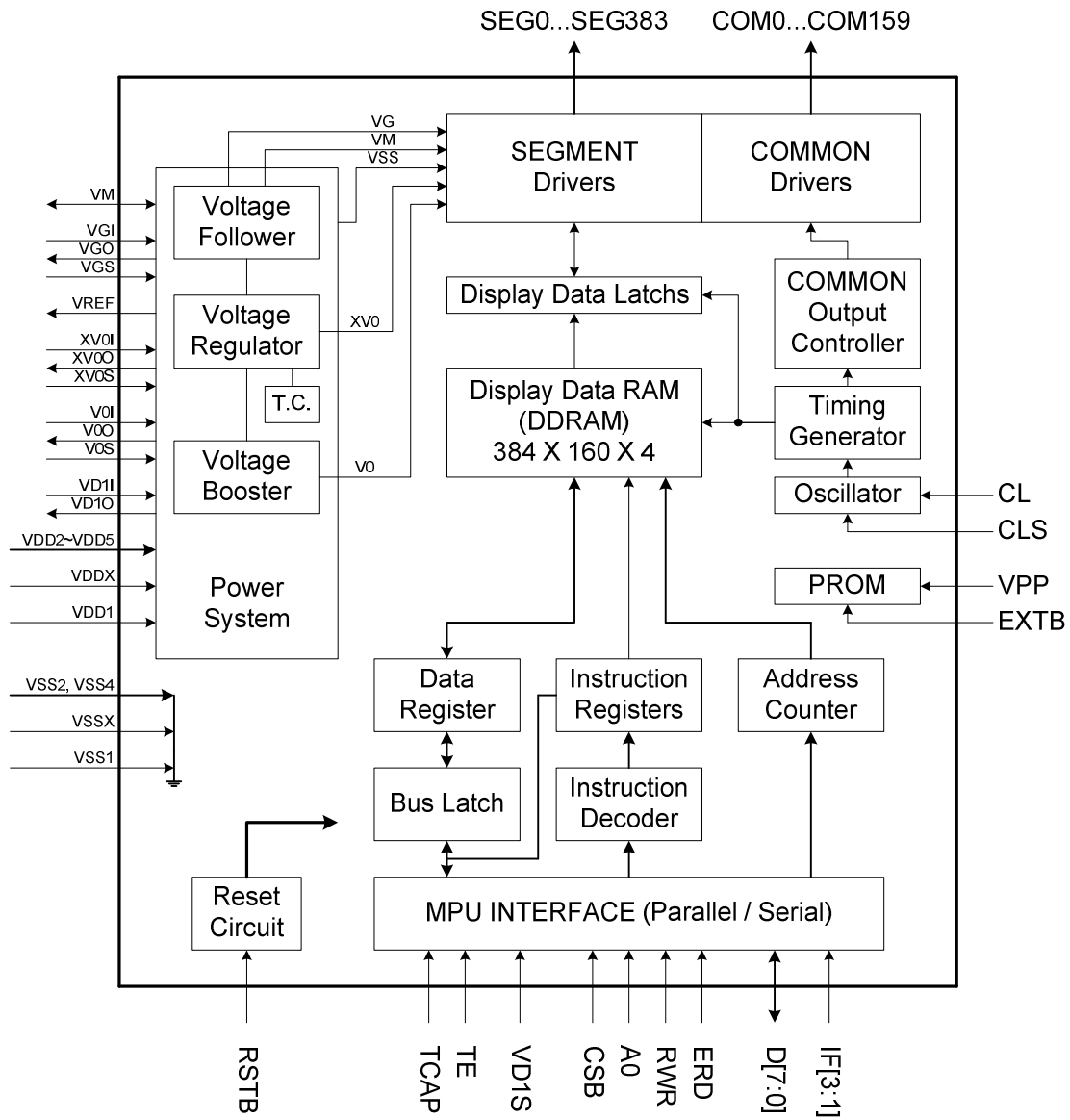
PIN DESCRIPTION

Power System

Name	Type	Description
VDD1	Power	VDD1 is the power of interface I/O circuit.
VDD2~5	Power	VDD2 is the analog power for internal booster. VDD3~5 are the analog power for LCD driver. VDD2~5 and VDDX are separated in ITO and connected together by FPC or PCB.
VDDX	Power	Digital power for OSC circuit. VDD2~5 and VDDX are separated in ITO and connected together by FPC or PCB.
VSS1	Power	Ground of interface, logic (VSS1) and OSC (VSSX) circuits. Ground system should be connected together by FPC or PCB.
VSS2 VSS4	Power	Ground of booster (VSS2) and LCD (VSS4) driver. Ground system should be connected together by FPC or PCB.
VSSX	Power	Ground of OSC circuit. Ground system should be connected together by FPC or PCB.
VD1S	Input	Digital power source selection. VD1S = "L": the power source of digital circuit is VDD1. VD1S = "H": the power source of digital circuit is internal regulator. <table><tr><th>VDD1 (TYP.)</th><th>Cap. of VD1 and VSS</th><th>Level of VD1S</th></tr><tr><td>1.8</td><td>Unnecessary</td><td>VSS1</td></tr><tr><td>2.8</td><td>Necessary</td><td>VDD1</td></tr><tr><td>3.0</td><td>Necessary</td><td>VDD1</td></tr><tr><td>3.3</td><td>Necessary</td><td>VDD1</td></tr></table>
VD1I VD1O	Power	VD1I is the power source of digital circuits. VD1O is the VD1 output. VD1I and VD1O should be connected together by FPC or PCB.
V0O V0I V0S	Power Power Input	Positive operating voltage of COM-drivers. V0O is the output of the positive Vop generator. V0I is the positive Vop supply of LCD drivers. V0S is the sensor of the positive Vop generator. V0O, V0I & V0S should be separated on ITO and be connected together by FPC.
XV0O XV0I XV0S	Power Power Input	Negative operating voltage of COM-drivers. XV0O is the output of the negative Vop generator. XV0I is the negative Vop supply of LCD drivers. XV0S is the sensor of the negative Vop generator. XV0O, XV0I & XV0S should be separated on ITO and be connected together by FPC.
VGO VGI VGS VM	Power Power Input Power	VG is the power of SEG-drivers. VM is the non-select voltage level of COM-drivers. VGO is the output of the VG regulator. VGI is the supply of SEG-drivers. VGS is the sensor of the VG regulator. VGO, VGI & VGS should be separated on ITO and be connected together by FPC. Be sure the relationships (as shown below) among the LCD driving voltages: $V0 \geq VG \geq VM \geq VSS \geq XV0$; $VDDA-0.7 \geq VM \geq 0.9V$; and $2*VDDA-0.7 \geq VG \geq 1.8V$ When this IC is operating, VG and VM are generated according to the bias setting shown below: <table><tr><th>LCD Bias</th><th>VG</th><th>VM</th><th></th></tr><tr><td>1/N Bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td><td>Note: N = 9~14</td></tr></table>

ST7586S

LCD Driver Outputs

Name	Type	Description
SEG0 to SEG383	Output	LCD SEG-driver outputs. The display data and the polar-signal (M) control the output voltage of SEG-driver. | Display Data	M	Segment Driver Output Voltage	
		Normal Display	Reverse Display
H	H	VG	VSS
H	L	VSS	VG
L	H	VSS	VG
L	L	VG	VSS
Display OFF, Sleep-In mode		VSS	VSS	
COM0 to COM159	Output	LCD COM-driver outputs. The internal scanning data and the polar-signal (M) control the output voltage of COM-driver. 	Scan data	M	Common Driver Output Voltage
H	H	XV0
H	L	V0
L	H	VM
L	L	VM
Display OFF, Sleep-In mode		VSS	

Microprocessor Interface

Name	Type	Description
RSTB	Input	Reset input pin. When RSTB is "L", internal initialization procedure is executed.
IF[3:1]	Input	These pins select interface operation mode. | IF3	IF2	IF1	MPU interface type
H	H	L	80 series 8-bit parallel
H	L	L	68 series 8-bit parallel
L	H	H	8-bit serial (4-Line)
L	H	L	9-bit serial (3-Line)	 Note: Refer to "Interface Selection" for detailed information.
CSB	Input	Chip select input pin. CSB="L": This chip is selected and the MPU interface is active. CSB="H": This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).

A0	Input	The function of this pin is different in parallel and serial interface.
		● In parallel interface: A0 is register selection input.
		  A0 = "H": inputs on data bus are display data;
		  A0 = "L": inputs on data bus are command.
		● In serial interface: this pad will be used as SCL (serial-clock) input

RWR	Input	Read / Write execution control pin. (This pin is only used in parallel interface) 	MPU Type	RWR	Description
6800-series	R/W	Read / Write control input pin R/W = "H" : read R/W = "L" : write
8080-series	/WR	Write enable clock input pin. The data are latched at the rising edge of the /WR signal. | This pin is not used in serial interfaces and should be connected to VDD1.

Name	Type	Description
ERD	Input	Read / Write execution control pin. (This pin is only used in parallel interface) _table below_ This pin is not used in serial interfaces and should be connected to VDD1.

D[7:0]	I/O	The bi-directional data bus of the MPU interface. When CSB is "H", they are high impedance.
		● If using serial interface:
		   D0 is the SDA signal in 4-Line & 3-Line interface.
		   D1 is the A0 signal in 4-Line interface.

MPU Type	ERD	Description
6800-series	E	Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.
8080-series	/RD	Read enable input pin. When /RD is "L", data bus is in output status.

Note:

1. After VDD1 is turned ON, all MPU interface pins should not be left OPEN.
2. The un-used pins should be connected to VDD1.

OTP Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in OTP. Apply external power (6.5~6.75V) here when programming (> 8mA for successful programming).
EXTB	Input	EXTB="L": Enable the extension operation mode. When programming OTP, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

Test Pins

Name	Type	Description
CLS	Test	Reserved for testing only. Please fix this pin to VDD1.
CL	Test	Reserved for testing only. Leave this pin open.
TCAP	Test	Reserved for testing only. Leave this pin open.
VREF	Test	Reserved for testing only. Leave this pin open.
TE	Test	Reserved for testing only. Leave this pin open.

ST7586S

ITO Resistance Limitation

Pin Name	ITO Resister
VDDX, VDD1~VDD5, VSSX, VSS1, VSS2, VSS4, V0I, V0O, V0S, XV0I, XV0O, XV0S, VM	<100Ω
VPP, VGI, VGO, VGS	<50Ω
A0, ERD, RWR, CSB, D[7:0], (SDA), (SCL), TE	<700Ω
RSTB	<10KΩ
IF[3:1], CLS, EXTB	<1KΩ
TCAP, CL, VREF	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM159 is equal, and so is it of SEG0 ~ SEG383.

2. These Limitations include the bottleneck of ITO layout.

3. Refer to the application note for ITO layout guideline.

FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7586S can interface with an MPU when CSB is "L". If CSB is "H", the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is "H".

Interface Selection

The interface selection is controlled by IF[3..1] pins. Please refer to the table below:

Table 1

Setting			MPU Type	Interface Pin Function				
IF3	IF2	IF1		CSB	A0	RWR	ERD	D[7:0]
H	H	L	Parallel 8080 series MPU	CSB	A0	/WR	/RD	D[7:0]
H	L	L	Parallel 6800 series MPU			R/W	E	
L	H	H	Serial 4-Line series MPU		SCL	--	--	D1=A0; D0=SDA. D[7:2] are not used.
L	H	L	Serial 3-Line series MPU			--	--	D0=SDA. D[7:1] are not used.

Note: The un-used pins are marked as "--" and should be fixed to "H" by "VDD1".

Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MPU		6800 series MPU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note: Reading Display Data or Parameter is specified by the instruction before the read operation.

Serial Interface

In serial interface mode (4-Line or 3-Line), IC is active when CSB is "L". Control signals (SDA, SCL and A0 for 4-Line) are enabled when CSB is "L". When CSB is "H", the MPU interface is not active and the internal shift register and counter are reset. It is recommended to set CSB to "H" after each byte transmission.

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to Fig. 1).
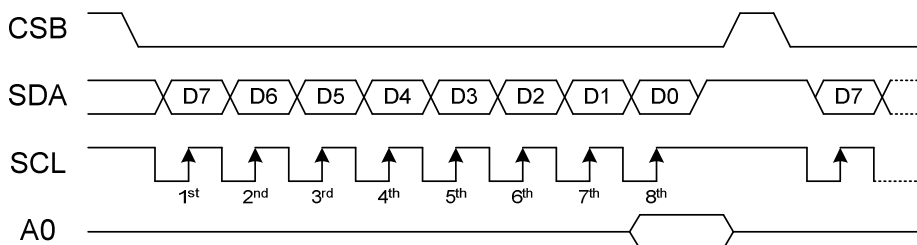

Fig. 1   Write-Operation of 4-Line Serial Interface

In 3-Line interface, A0 signal is not available and the 1st output of SDA will be treated as A0 flag (refer to Fig. 2).
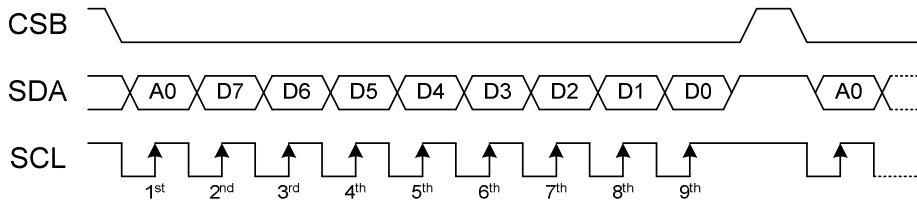
Fig. 2   Write-Operation of 4-Line Serial Interface

Display Data RAM (DDRAM)

ST7586S containing a 384x160x4 bit static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 384 columns by 160 rows. ST7586S provides two kinds of display modes (monochrome mode and gray scale mode) and a fast-addressing mode for fast updating display data. Each column address represents 3 sub-columns. For example, setting the column address to "01h" means that upcoming 8 bits data is addressing to column 3; column 4 and column 5 respectively (refer to Fig. 3, Fig. 4 and Fig. 5). The display data which is written by MCU will be stored in DDRAM with the format of D7 at the left and D0 at the right when MX[1:0]=(0,0) (refer to Fig. 3, Fig. 4 and Fig. 5). The row address is directly related to the row output number. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.
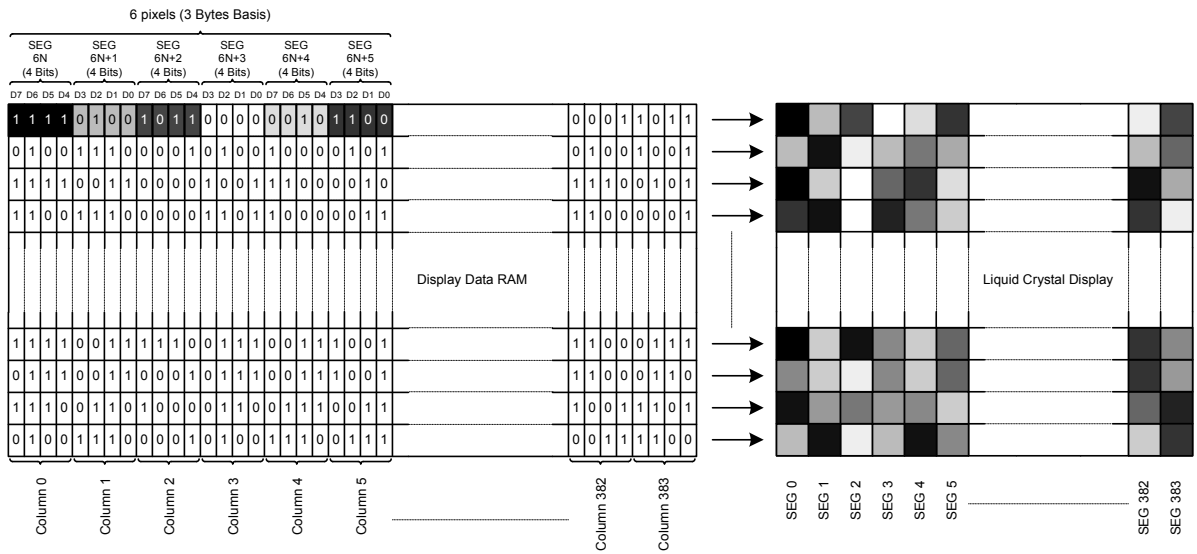
Pixel Data				LCD
D7 (D3)	D6 (D2)	D5 (D1)	D4 (D0)	
1	1	1	1	
1	1	1	0	
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	

Fig. 3   DDRAM Mapping (16-Level Gray Scale Mode)

Fig. 4   DDRAM Mapping (4-Level Gray Scale Mode)
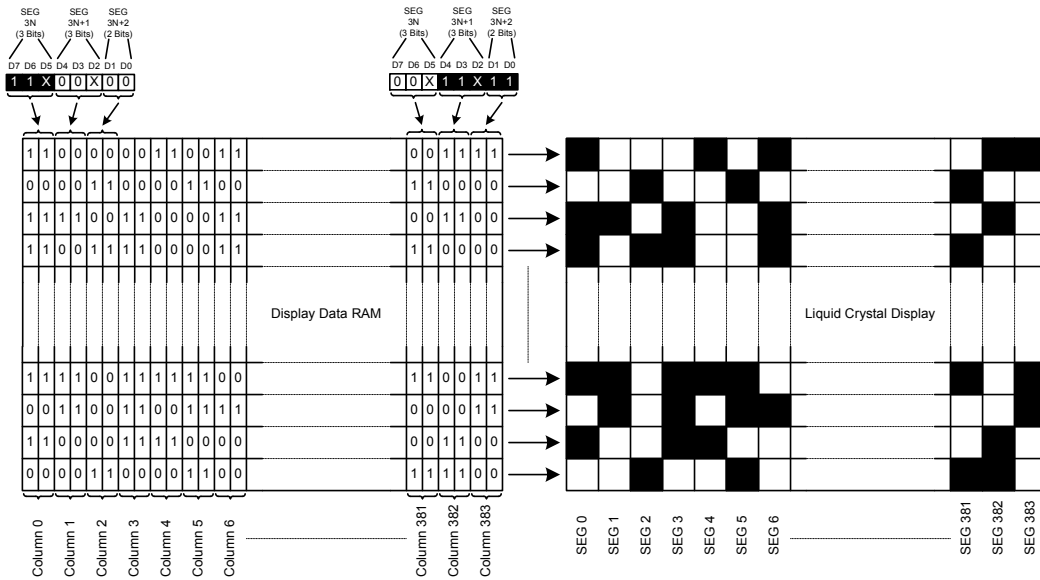
Fig. 5   DDRAM Mapping (Monochrome Mode)

Addressing

In order to allow MCU accessing display data continuously, the address counter is automatically increasing by one (+1) after accessing each byte of display data (i.e. "White Display Data" in all interface or "Read Display Data" in parallel interface). The locations of RAM are addressed by the address pointers (XS, XE, YS and YE). The address ranges are X=0~127 (column address) and Y=0~159 (row address). Addresses outside these range is not allowed.

Before writing to DDRAM, a "window" must be defined for the incoming display data. By specifying the address pointers XS, XE, YS and YE, a "window" is established. The instruction registers XS and YS identify the start addresses while XE and YE identifying the end addresses. For example, the whole display range will be written via the following values to define 384x160: XS=0 (00h), YS=0 (00h) and XE=127 (7Fh), YE=159 (9Fh).

Column Address Circuit

The column address of DDRAM is specified by the "Set Column Address" instruction. Each column address includes three sub-columns Column N, Column N+1 and Column N+2 respectively ("N" is the column address value). The column address counter is increased by one (+1) after each byte of display data accessed (write/read). The starting column address is defined by XS and the ending column address is defined by XE. The column address counter will be returned to the starting column address (XS) immediately if the increment of the column address exceeds the boundary column address (XE).

Row Address Circuit

The circuit provides the row address of DDRAM. The row address is increased by one (+1) after the column address counter is over XE. The row address will be returned to starting row address (YS) immediately when the row address is increased by one over the ending row address (YE).

LCD Display Function
DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or MY setting is illustrated below.

Fig. 6 DDRAM Display Direction
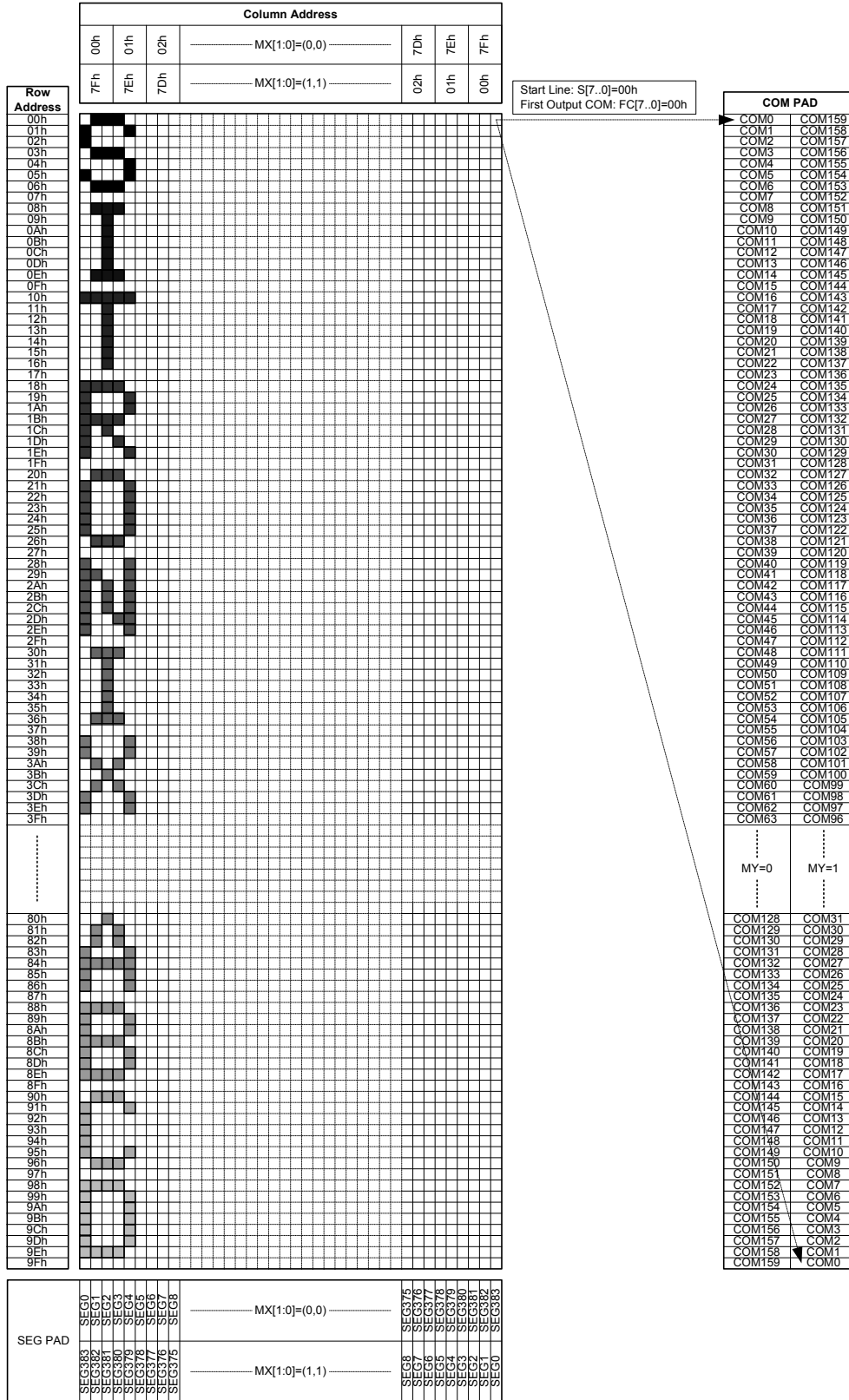
ST7586S

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (setting by instruction of First Output COM) of display. Therefore, by setting Line Address repeatedly, ST7586S is possible to realize the screen scrolling without changing the content of DDRAM as shown in Fig. 7.
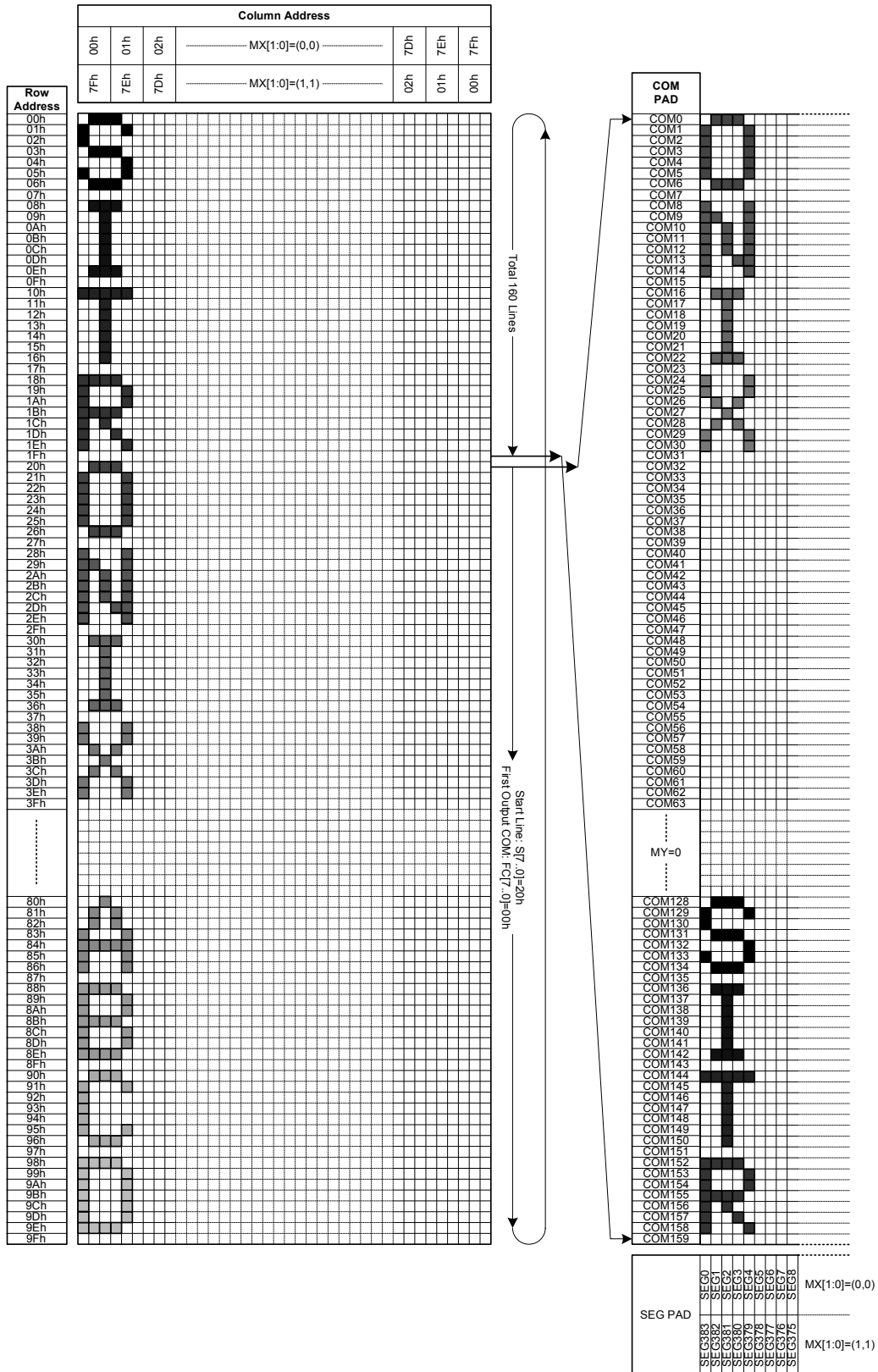
Fig. 7   Display Data RAM Map (1/160 Duty)

Partial Display

This function is defining the visible display area as illustrated in Fig. 8. The different partial display area setting will be changing frame rate or Vop to avoid abnormal display. The recommended range of partial display area setting is defined from 64 duty to 160 duty. The partial display setting is combining the instructions of Partial Display and Partial Display Area.

Original Display

Partial Area Display (PTS<PTE)

Partial Area Display (PTE<PTS)
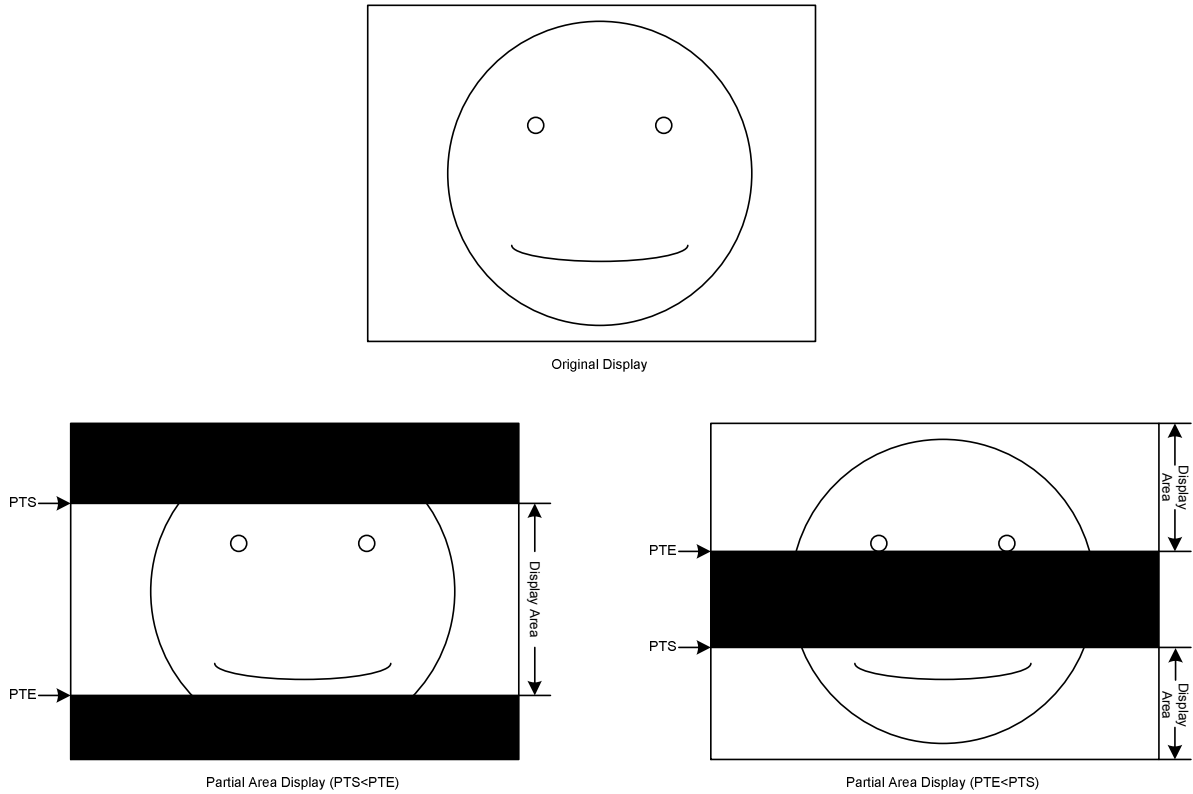
Fig. 8   Partial Display Definition

Rolling Scroll

This function is determined by the instructions of Scroll Area and Start Line. TA, SA and BA meaning Top Area, Scrolling Area and Bottom Area respectively. The instruction of Scroll Area setting must correspond to TA+SA+BA=160. Depending on the Scroll Area setting, the setting range of Start Line must correspond to $TA \leqq S[7..0] < (TA+SA)$.

Original Display

Rolling Scroll Display
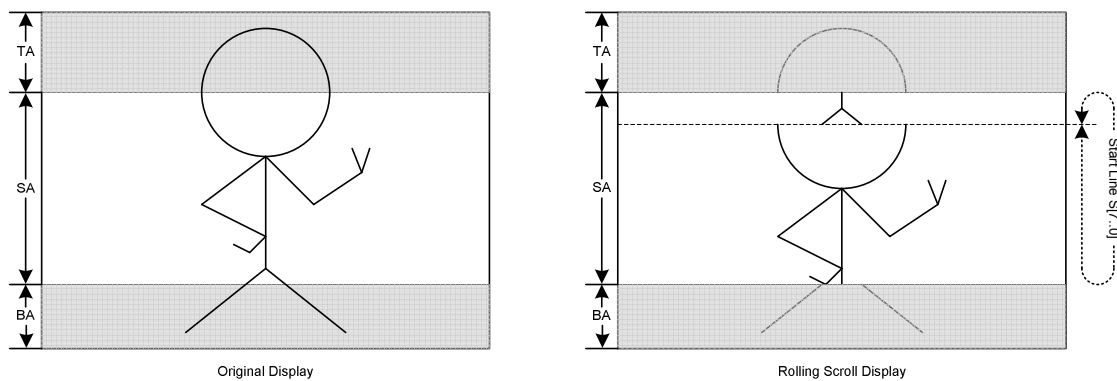
Fig. 9   Scroll Definition

Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external component. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7586S is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW section.

External Component of Power Circuit

The recommended external power components need only three capacitors. The detailed values of these three capacitors are determined by panel size and loading.
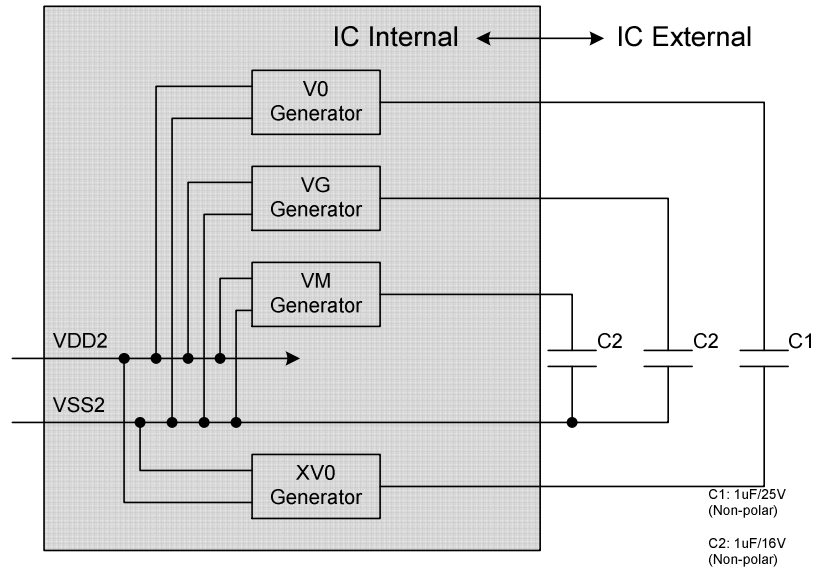
Fig. 10   Power Circuit

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Temperature Gradient Selection Circuit
SET V0 with temperature compensation (Temperature ≠ 24℃)

There are 16-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8℃. Please see Fig. 11 as below.
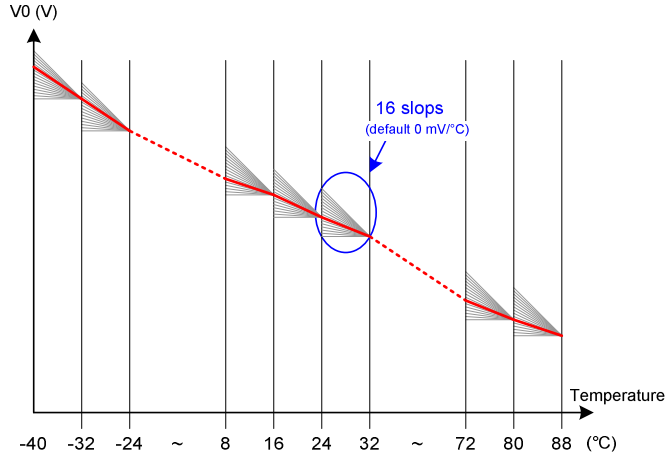
Fig. 11   Temperature Compensation Coefficient Selection

In instruction Temperature Gradient Compensation each parameter MTx, where x=0, 1, 2,…, E, F has a setting value between 0 and 15. MTx=0 results in Mx=0V increment on V0, MTx=1 results in Mx=5mV increment,…, MTx=15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V0 quantity due to temperature V0(T) are described in the equation shown in Table 3.

Temerature Range	Equation V0(T) at temperature=T℃
-40℃ $\leq$ T < -32℃	V0(T) = V0(T24) + (-32 - T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) x 8
-32℃ $\leq$ T < -24℃	V0(T) = V0(T24) + (-24 - T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24℃ $\leq$ T < -16℃	V0(T) = V0(T24) + (-16 - T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16℃ $\leq$ T < -8℃	V0(T) = V0(T24) + (-8 - T) x M3 + (M4 + M5 + M6 + M7) x 8
-8℃ $\leq$ T < 0℃	V0(T) = V0(T24) + (0 - T) x M4 + (M5 + M6 + M7) x 8
0℃ $\leq$ T < 8℃	V0(T) = V0(T24) + (8 - T) x M5 + (M6 + M7) x 8
8℃ $\leq$ T < 16℃	V0(T) = V0(T24) + (16 - T) x M6 + M7 x 8
16℃ $\leq$ T < 24℃	V0(T) = V0(T24) + (24 - T) x M7
24℃ $\leq$ T < 32℃	V0(T) = V0(T24) - (T - 24) x M8
32℃ $\leq$ T < 40℃	V0(T) = V0(T24) - (T - 32) x M9 – M8 x 8
40℃ $\leq$ T < 48℃	V0(T) = V0(T24) - (T - 40) x M10 – (M9 + M8) x 8
48℃ $\leq$ T < 56℃	V0(T) = V0(T24) - (T - 48) x M11 – (M10 + M9 + M8) x 8
56℃ $\leq$ T < 64℃	V0(T) = V0(T24) - (T - 56) x M12 – (M11 + M10 + M9 + M8) x 8
64℃ $\leq$ T < 72℃	V0(T) = V0(T24) - (T - 64) x M13 – (M12 + M11 + M10 + M9 + M8) x 8
72℃ $\leq$ T < 80℃	V0(T) = V0(T24) - (T - 72) x M14 – (M13 + M12 + M11 + M10 + M9 + M8) x 8
80℃ $\leq$ T < 88℃	V0(T) = V0(T24) - (T - 80) x M15 – (M14 + M13 + M12 + M11 + M10 + M9 + M8) x 8

Table 3

Fig. 12   Temperature Gradient Compensation

Note:

● Please make sure to avoid any kind of heating source near ST7586S such as back light, to prevent Vop is not anticipative because of temperature compensation circuit is working.

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Frequency Temperature Gradient Compensation Coefficient
Register Loading Detection

ST7586S will auto-switch frame rate in different temperature such as Fig. 13. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Frame Rate. The frame rate range is from 18.75Hz to 170Hz.
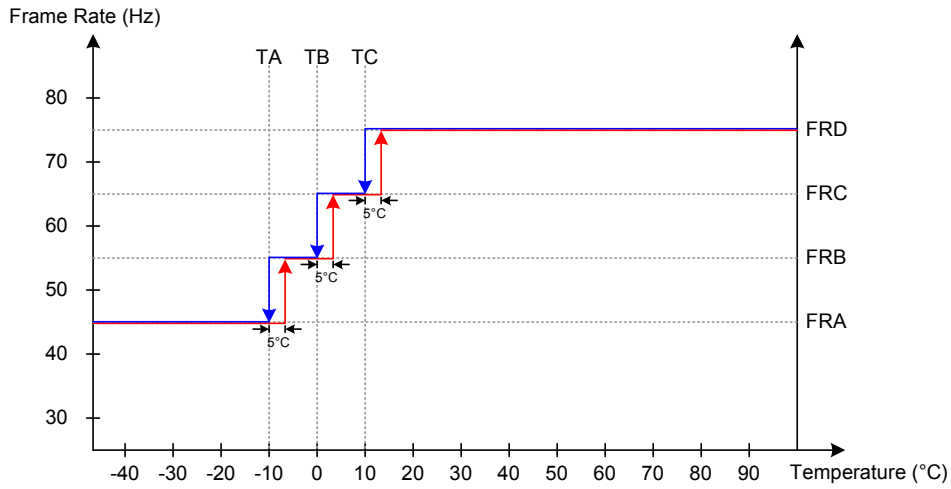
Fig. 13   Frame Rate

RESET CIRCUIT

Setting RSTB pin to "L" (hardware reset) or instruction RESET (software reset) can initialize internal function. Please note the hardware reset is not same as the software reset. Generally, VDD1 is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDD1 is stable. Initialization by RSTB pin is essential before operating. The default values of registers are listed below:

Procedure		After Hardware Reset	After Software Reset
DDRAM Content		No Change	No Change
Column Address	Start Address	00h	00h
	End Address	7Fh	7Fh
Row Address	Start Address	00h	00h
	End Address	9Fh	9Fh
Power Save Mode		Sleep IN Mode	Sleep IN Mode
Partial Mode		Partial Mode OFF	Partial Mode OFF
Partial Display Area	Start Address	00h	00h
	End Address	9Fh	9Fh
Inverse Display		Inverse Display OFF	Inverse Display OFF
All Pixel ON		All Pixel ON Mode OFF	All Pixel ON Mode OFF
Display ON/OFF		Display OFF	Display OFF
Display Control	SEG Direction	SEG0 → SEG383	No Change
	COM Direction	COM0 → COM159	No Change
Start Line		00h	00h
Display Duty		9Fh	9Fh
First Output COM		00h	00h
N-Line Inversion		8Ch	8Ch
Read Modify Write		Disable	Disable
Vop[8:0]		142h	142h
BIAS		1/10	1/10
Booster Level		x8	x8
Frame Rate (Gray Scale Mode & Monochrome Mode)		FA[4:0]=06h, FB[4:0]=0Bh, FC[4:0]=0Dh, FD[4:0]=12h	FA[4:0]=06h, FB[4:0]=0Bh, FC[4:0]=0Dh, FD[4:0]=12h
Temperature Range		TA[6:0]=1Eh, TB[6:0]=28h, TC[6:0]=32h	TA[6:0]=1Eh, TB[6:0]=28h, TC[6:0]=32h
Temperature Gradient Compensation		MT0[3:0]=0Fh, MT1[3:0]=07h, MT2[3:0]=02h, MT3[3:0]=02h, MT4[3:0]=01h, MT5[3:0]=01h, MT6[3:0]=02h, MT7[3:0]=00h, MT8[3:0]=00h, MT9[3:0]=00h, MTA[3:0]=02h, MTB[3:0]=03h, MTC[3:0]=02h, MTD[3:0]=08h, MTE[3:0]=06h, MTF[3:0]=0Bh	MT0[3:0]=0Fh, MT1[3:0]=07h, MT2[3:0]=02h, MT3[3:0]=02h, MT4[3:0]=01h, MT5[3:0]=01h, MT6[3:0]=02h, MT7[3:0]=00h, MT8[3:0]=00h, MT9[3:0]=00h, MTA[3:0]=02h, MTB[3:0]=03h, MTC[3:0]=02h, MTD[3:0]=08h, MTE[3:0]=06h, MTF[3:0]=0Bh

Table 4

INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
NOP	0	0	0	0	0	0	0	0	0	0	No operation
RESET	0	0	0	0	0	0	0	0	0	1	Software reset
Power Save	0	0	0	0	0	1	0	0	0	SLP	Set power save mode SLP=0: Sleep in mode SLP=1: Sleep out mode
Partial Mode	0	0	0	0	0	1	0	0	1	PTL	Set partial mode PTL=0: Partial mode on PTL=1: Partial mode off
Inverse Display	0	0	0	0	1	0	0	0	0	INV	Set inverse display mode INV=0: Normal display INV=1: Inverse display
All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
Display ON/OFF	0	0	0	0	1	0	1	0	0	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
Set Column Address	0	0	0	0	1	0	1	0	1	0	Set column address Starting column address: 00h≤XS≤7Fh Ending column address: XS≤XE≤7Fh
	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
Set Row Address	0	0	0	0	1	0	1	0	1	1	Set row address Starting row address: 00h≤YS≤9Fh Ending row address: YS≤YE≤9Fh
	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Write Display Data	0	0	0	0	1	0	1	1	0	0	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Read Display Data	0	0	0	0	1	0	1	1	1	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Display Area	0	0	0	0	1	1	0	0	0	0	Set partial area Partial display address start: 00h≤PTS≤9Fh Partial display address end: 00h≤PTE≤9Fh Display Area: 64≤Duty≤160
	1	0	PTS15	PTS14	PTS13	PTS12	PTS11	PTS10	PTS9	PTS8	
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE15	PTE14	PTE13	PTE12	PTE11	PTE10	PTE9	PTE8	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	
Scroll Area	0	0	0	0	1	1	0	0	1	1	Set scroll area Top Area: TA=00h~A0h Scrolling Area: SA=00h~A0h Bottom Area: BA=00h~A0h TA+SA+BA=160
	1	0	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	1	0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
Display Control	0	0	0	0	1	1	0	1	1	0	Set scan direction of COM and SEG MY=0: COM0→COM159 MY=1: COM159→COOM0 MX[1:0]=(0,0): SEG0→SEG383 MX[1:0]=(1,1): SEG383→SEG0
	1	0	MY	MX1	0	0	MX0	0	0	0	
Start Line	0	0	0	0	1	1	0	1	1	1	Set display start line S=00h~9Fh
	1	0	S7	S6	S5	S4	S3	S2	S1	S0	

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INSTRUCTION	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
Display Mode	0	0	0	0	1	1	1	0	0	M	Set display mode M=0: Gray mode M=1 : Monochrome mode
Enable DDRAM Interface	0	0	0	0	1	1	1	0	1	0	Enable DDRAM interface RIF=0: Monochrome mode & 4-level gray scale mode RIF=1: 16-level gray scale mode
	1	0	0	0	0	0	0	0	1	RIF	
Display Duty	0	0	1	0	1	1	0	0	0	0	Set display duty DT=03h~9Fh
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
First Output COM	0	0	1	0	1	1	0	0	0	1	Set first output COM FC=00h~9Fh
	1	0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	
FOSC Divider	0	0	1	0	1	1	0	0	1	1	Set FOSC dividing ratio
	1	0	0	0	0	0	0	0	FOD1	FOD0	
Partial Display	0	0	1	0	1	1	0	1	0	0	Set partial display mode
	1	0	1	0	1	0	0	0	0	0	
N-Line Inversion	0	0	1	0	1	1	0	1	0	1	Set N-Line inversion
	1	0	M	0	0	NL4	NL3	NL2	NL1	NL0	
Read Modify Write	0	0	1	0	1	1	1	0	0	RMW	Read modify write control RMW=0: Enable read modify write RMW=1: Disable read modify write
Set Vop	0	0	1	1	0	0	0	0	0	0	Set Vop
	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	-	-	-	-	-	-	-	Vop8	
Vop Increase	0	0	1	1	0	0	0	0	0	1	Vop increase one step
Vop Decrease	0	0	1	1	0	0	0	0	1	0	Vop decrease one step
BIAS System	0	0	1	1	0	0	0	0	1	1	Set BIAS system
	1	0	-	-	-	-	-	BS2	BS1	BS0	
Booster Level	0	0	1	1	0	0	0	1	0	0	Set booster level
	1	0	-	-	-	-	-	BST2	BST1	BST0	
Analog Control	0	0	1	1	0	1	0	0	0	0	Enable analog circuit
	1	0	0	0	0	1	1	1	0	1	
Auto Read Control	0	0	1	1	0	1	0	1	1	1	Auto read control XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR /RD	0	0	0	0	0	
OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
OTP Write	0	0	1	1	1	0	0	0	1	0	OTP programming procedure
OTP Read	0	0	1	1	1	0	0	0	1	1	OTP up-load procedure
OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=0: Disable OTP Ctrl=1: Enable OTP
	1	0	0	Ctrl	0	1	1	0	0	1	
OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	1	1	1	1	

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INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Frame Rate (Gray Scale Mode)	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range (Gray scale mode)
	1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	
Frame Rate (Monochrome Mode)	0	0	1	1	1	1	0	0	0	1	Frame rate setting in different temperature range (Monochrome mode)
	1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	
Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	

INSTRUCTION DESCRIPTION

NOP

"No Operation" instruction. ST7586S will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	0	0	No operation

RESET

When this instruction is issued, the software reset procedure is started. This instruction resets the software reset default value and keeps the DDRAM content.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	0	1	Software reset

Power Save

When ST7586S enters the sleep in mode, the mode causes the LCD module entering the minimum power consumption mode. All of operations (e.g. the DC/DC converter, internal oscillator and panel scanning) are stopped.

When ST7586S enters sleep out mode (exit sleep in mode), the DC/DC converter and internal oscillator are started.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	0	SLP	SLP=0: Sleep in mode SLP=1: Sleep out mode

Partial Mode

When ST7586S enters the partial display mode, the partial area is described by Partial Display Area instruction. The different partial display area setting will be changing frame rate or Vop to avoid abnormal display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	1	PTL	PTL=0: Partial mode on PTL=1: Partial mode off

Inverse Display

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	INV	INV=0: Normal display INV=1: Inverse display

All Pixel ON/OFF

When ST7586S enters all pixels on or off mode, all display pixels are turned on or off regardless of the content of DDRAM. The content of DDRAM is not changed by setting All Pixel ON/OFF. After execute the instruction of Partial Mode, the display mode will exit all pixel on/off mode then enter normal mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	1	AP	AP=0: All pixel off mode AP=1: All pixel on mode

Display ON/OFF

This instruction turns the display ON or OFF. When ST7586S enters display off, the display output is blank regardless of the content of DDRAM. When ST7586S enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	0	DSP	DSP=0: Display off DSP=1: Display on

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Set Column Address

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one (+1) after each DDRAM access. After the ending column address XE[15..0], column address returns to starting column address XS[15..0]. The XS[15..0] setting that must be equal to or less than XE[15..0]. When XS[15..0] or XE[15..0] is great than 7Fh, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	0	XS: Starting column address XE: Ending column address
1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

Set Row Address

This instruction is used to define area of DDRAM where MCU can access. The row address is automatically increased by one (+1) after column address counter is over XE[15..0]. The row address will return to starting row address YS[15..0] immediately when the row address increases one over the ending row address YE[15..0]. The YS[15..0] setting must be equal to or less than YE[15..0]. When YS[15..0] or YE[15..0] is great than 9Fh, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	1	YS: Starting row address YE: Ending row address
1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

Write Display Data

This instruction is used to transfer data from MCU to DDRAM without changing status of ST7586S. The column address and row address will be reset to starting column address (XS) and starting row address (YS) when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Write Display Data would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	1	0	0	Write display data to DDRAM
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

Read Display Data

The instruction is used to transfer data from DDRAM to MCU without changing status of ST7586S. The column address and row address will be reset to staring column address (XS) and starting row address (YS) when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Read Display Data would be stopped when any other instruction is accepted. Read Display Data is only available via the parallel interface.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	1	1	0	Read display data from DDRAM
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

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Partial Display Area

This instruction defines the display area of partial mode. There are four parameters associated with this instruction, the Partial Display Address Start PTS[15..0] and the Partial Display Address End as illustrated in Fig. 8. The instruction of Partial Display must be executed before setting the instruction of Partial Display Area

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	0	0	0	Partial display address start: 00h≦PTS≦9Fh
1	0	PTS15	PTS14	PTS13	PTS12	PTS11	PTS10	PTS9	PTS8	
1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	Partial display address end: 00h≦PTE≦9Fh
1	0	PTE15	PTE14	PTE13	PTE12	PTE11	PTE10	PTE9	PTE8	
1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	Display Area: 64≦Duty≦160

Scroll Area

This instruction defines the scrolling area of display. The first parameter TA[7..0] describes the fixed Top Area. The second parameter SA[7..0] describes the Scrolling Area. The third parameter BA[7..0]describes the Bottom Area. This instruction setting must correspond to TA+SA+BA=160.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	0	1	1	Top Area: TA=00h~A0h
1	0	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Scrolling Area: SA=00h~A0h
1	0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	Bottom Area: BA=00h~A0h
1	0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	TA+SA+BA=160

Display Control

This instruction defines the write/read scanning direction of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	0	MY=0: COM0→COM159 MY=1: COM159→COM0
1	0	MY	MX1	0	0	MX0	0	0	0	MX[1:0]=(0,0): SEG0→SEG383 MX[1:0]=(1,1): SEG383→SEG0

Start Line

This instruction sets row address of DDRAM to determine the initial display line. The display data of specified row address is displayed at the First Output COM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	1	S=00h~9Fh
1	0	S7	S6	S5	S4	S3	S2	S1	S0	

S7	S6	S5	S4	S3	S2	S1	S0	Line Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	127
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

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Display Mode

This instruction defines the display mode is gray scale mode or monochrome mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	0	M	M=0 : Gray mode M=1 : Monochrome mode

Enable DDRAM Interface

This instruction is used to initial DDRAM interface for write data to DDRAM or read data from DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	1	0	Enable DDRAM interface
1	0	0	0	0	0	0	0	1	RIF	RIF=0: Monochrome mode & 4-level gray scale mode RIF=1: 16-level gray scale mode

Display Duty

This instruction defines display duty. The parameter setting of Display Duty is the number of physical display duty decreasing by one (-1). For example, the parameter must set 9Fh when the LCD display duty is 160.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	0	DT=03h~9Fh
1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	

First Output COM

This instruction defines the first output COM number that mapping to the Start Line of DDRAM. For example, the parameter of First Output COM setting is 08h and the parameter of Start Line setting is 02h means that the COM8 would output the DDRAM data at row address 2.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	1	FC=00h~9Fh
1	0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	

FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	COM Number
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	127
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

ST7586S

FOSC Divider

This instruction is used to specify the FOSC dividing

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	1	1	Set FOSC dividing ratio
1	0	0	0	0	0	0	0	FOD1	FOD0	

FOD1	FOD0	FOSC Dividing Ratio
0	0	Not Divide
0	1	2 Divisions
1	0	4 Divisions
1	1	8 Divisions

Partial Display

This instruction is used to set the partial display. The instruction of Partial Display must be executed before setting the instruction of Partial Display Area.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	1	0	0	Set partial display mode
1	0	1	0	1	0	0	0	0	0	

N-Line Inversion

This instruction is used to set the frame inverted number with range of 2 to 31.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	1	0	1	Set N-Line inversion
1	0	M	0	0	NL4	NL3	NL2	NL1	NL0	

M	N-Line Inversion Mode
0	Inversion occurs in every frame
1	Inversion is independent from frame

NL4	NL3	NL2	NL1	NL0	Line Inversion
0	0	0	0	0	Frame inversion
0	0	0	1	0	3 line inversion
0	0	0	1	1	4 line inversion
:	:	:	:	:	:
1	1	1	0	1	30 line inversion
1	1	1	1	0	31 line inversion
1	1	1	1	1	32 line inversion

Read Modify Write

This instruction is used to enter/exit read modify write mode. When entering read modify write, the display data read will not increase column address. Only the display data write operation will increase the column address. This mode is maintained until Disable Read Modify Write (B9h) is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	1	0	0	RMW	RMW=0: Enable read modify write RMW=1: Disable read modify write

```
         ( Set Row/Column Address )
                    │
                    ▼
         [ Enable Read Modify Write ]
                    │
                    ▼
      ( Read-Modify-Write Cycle )◄──┐
                    │               │
                    ▼               │
           [ Dummy Read ]           │
                    │               │
                    ▼               │
           [ Data Read ]            │
                    │               │
                    ▼             No│
           [ Modify Data ]          │
                    │               │
                    ▼               │
           [ Data Write      ]      │
           [ (at same Column Addr.) ]
                    │               │
                    ▼ Column Address increase
              < Finished? >─────────┘
                    │
                    ▼ Yes
             ( Done )
```
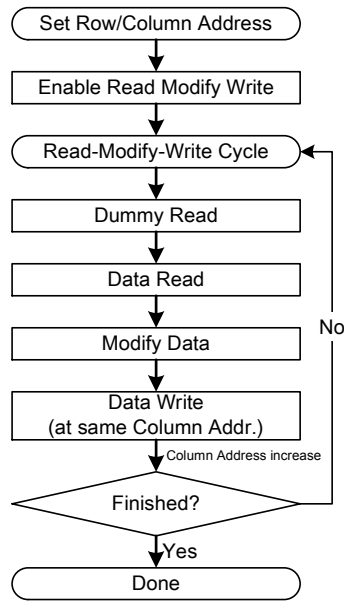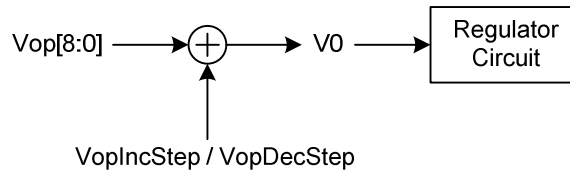
Set Vop

This instruction is used to adjust the optimum LCD supply voltage Vop.

The calculation of Vop is as shown blow: V0 = 3.6 + (Vop[8:0] + VopIncStep – VopDecStep) x 0.04

VopIncStep = Total Vop Increase Steps

VopDecStep = Total Vop Decrease Steps

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	0	0	0	
1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	Set Vop
1	0	-	-	-	-	-	-	-	Vop8	

The suggestion of usable V0 voltage is shown below (assume, VopIncStep / VopDecStep=0):

Vop8	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	V0 (V)
0	0	1	1	0	0	0	0	0	7.44
0	0	1	1	0	0	0	0	1	7.48
0	0	1	1	0	0	0	1	0	7.52
:	:	:	:	:	:	:	:	:	:
1	0	1	1	0	0	1	1	0	17.92
1	0	1	1	0	0	1	1	1	17.96
1	0	1	1	0	1	0	0	0	18.00

Vop Increase

This instruction is used to increase Vop step by one

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	0	0	1	Vop increase one step

Vop Decrease

This instruction is used to decrease Vop step by one

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	0	1	0	Vop decrease one step

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BIAS System

This instruction is used to select LCD bias ratio of the voltage to meet the requirement of driving the LCD.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	0	1	1	Set BIAS system
1	0	-	-	-	-	-	BS2	BS1	BS0	

BS2	BS1	BS0	BIAS Ratio
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9

Booster Level

This instruction is used to control the built-in booster circuit to provide the power source of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	1	0	0	Set booster level
1	0	-	-	-	-	-	BST2	BST1	BST0	

BST2	BST1	BST0	Booster Level
0	0	0	x1 Booster
0	0	1	x2 Booster
0	1	0	x3 Booster
0	1	1	x4 Booster
1	0	0	x5 Booster
1	0	1	x6 Booster
1	1	0	x7 Booster
1	1	1	x8 Booster

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Analog Control

This instruction is used to set status of analog circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	0	0	Enable analog circuit
1	0	0	0	0	1	1	1	0	1	

Auto Read Control

This instruction is used to set status of OTP auto read to enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	XARD=0: Enable auto read
1	0	1	0	0	XARD	1	1	1	1	XARD=1: Disable auto read

OTP WR/RD Control

This instruction is used to set status of OTP that write to OTP or read from OTP.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	WR/RD=0: Enable OTP read
1	0	0	0	WR/RD	0	0	0	0	0	WR/RD=1: Enable OTP write

OTP Control Out

This instruction is used to cancel the OTP control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	1	OTP control out

OTP Write

This instruction is used to trigger OTP programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	0	OTP programming procedure

OTP Read

This instruction is used to trigger OTP up-load procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	OTP up-load procedure

OTP Selection Control

This instruction is used to define OTP selection control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	0	Ctrl=0: Disable OTP
1	0	0	Ctrl	0	1	1	0	0	1	Ctrl=1: Enable OTP

OTP Programming Setting

This instruction is used to set OTP write timing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	1	OTP programming setting
1	0	0	0	0	0	1	1	1	1	

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Frame Rate (Gray Scale Mode)

When enter gray scale mode (4-level gray scale or 16-level gray scale), this instruction is used to define frequency of frame rate in different temperature range as shown in Fig. 13

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	0	FRA: FR in temp. -30℃ to TA
1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	FRB: FR in temp TA to TB
1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	FRC: FR in temp. TB to TC
1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	FRD: FR in temp TC to 90℃

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
0	0	0	0	0	38.5
0	0	0	0	1	38.5
0	0	0	1	0	38.5
0	0	0	1	1	40.0
0	0	1	0	0	41.5
0	0	1	0	1	46.0
0	0	1	1	0	46.0
0	0	1	1	1	49.0
0	1	0	0	0	51.0
0	1	0	0	1	53.0
0	1	0	1	0	55.0
0	1	0	1	1	55.0
0	1	1	0	0	69.0
0	1	1	0	1	73.0
0	1	1	1	0	76.5
0	1	1	1	1	76.5

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
1	0	0	0	0	77.0
1	0	0	0	1	77.0
1	0	0	1	0	77.0
1	0	0	1	1	80.0
1	0	1	0	0	83.0
1	0	1	0	1	92.0
1	0	1	1	0	92.0
1	0	1	1	1	98.0
1	1	0	0	0	102.0
1	1	0	0	1	106.0
1	1	0	1	0	110.0
1	1	0	1	1	110.0
1	1	1	0	0	138.0
1	1	1	0	1	146.0
1	1	1	1	0	153.0
1	1	1	1	1	153.0

Frame Rate (Monochrome Mode)

When enter monochrome mode, this instruction is used to define frequency of frame rate in different temperature range as shown in Fig. 13

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	1	FRA: FR in temp. -30℃ to TA
1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	FRB: FR in temp TA to TB
1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	FRC: FR in temp. TB to TC
1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	FRD: FR in temp TC to 90℃

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)		FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
0	0	0	0	0	38.5		1	0	0	0	0	77.0
0	0	0	0	1	38.5		1	0	0	0	1	77.0
0	0	0	1	0	38.5		1	0	0	1	0	77.0
0	0	0	1	1	40.0		1	0	0	1	1	80.0
0	0	1	0	0	41.5		1	0	1	0	0	83.0
0	0	1	0	1	46.0		1	0	1	0	1	92.0
0	0	1	1	0	46.0		1	0	1	1	0	92.0
0	0	1	1	1	49.0		1	0	1	1	1	98.0
0	1	0	0	0	51.0		1	1	0	0	0	102.0
0	1	0	0	1	53.0		1	1	0	0	1	106.0
0	1	0	1	0	55.0		1	1	0	1	0	110.0
0	1	0	1	1	55.0		1	1	0	1	1	110.0
0	1	1	0	0	69.0		1	1	1	0	0	138.0
0	1	1	0	1	73.0		1	1	1	0	1	146.0
0	1	1	1	0	76.5		1	1	1	1	0	153.0
0	1	1	1	1	76.5		1	1	1	1	1	153.0

Temperature Range

This instruction is used to define the temperature range for automatic frame rate adjustment according to current temperature as shown in Fig. 13.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	1	0	TA[6 :0]=TA Temp.(℃)+40
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	TB[6:0]=TB Temp.(℃)+40
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	TC[6 :0]=TC Temp.(℃)+40

Temp. Range Value	Temp. Rising State (℃)	Temp. Falling State (℃)
Freq. changing point A	(TA[6:0]-40)+5	TA[6:0]-40
Freq. changing point B	(TB[6:0]-40)+5	TB[6:0]-40
Freq. changing point C	(TC[6:0]-40)+5	TC[6:0]-40

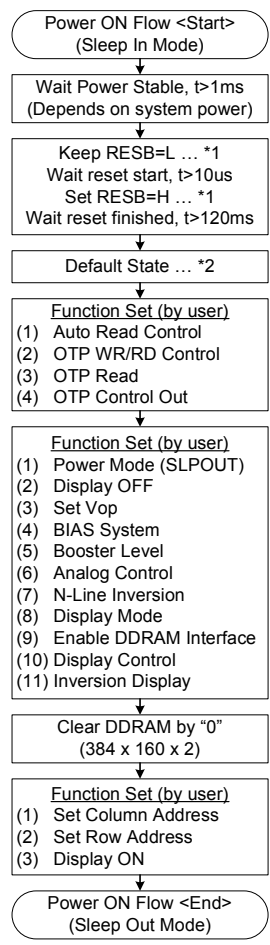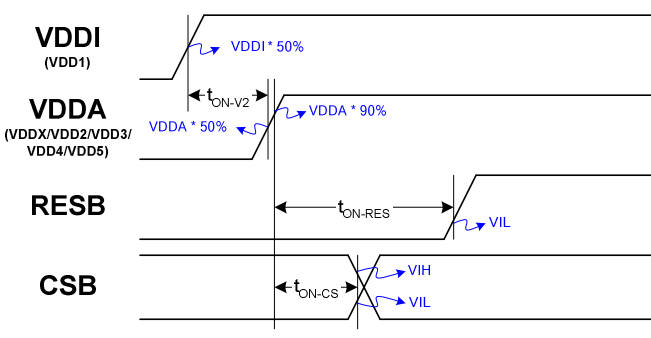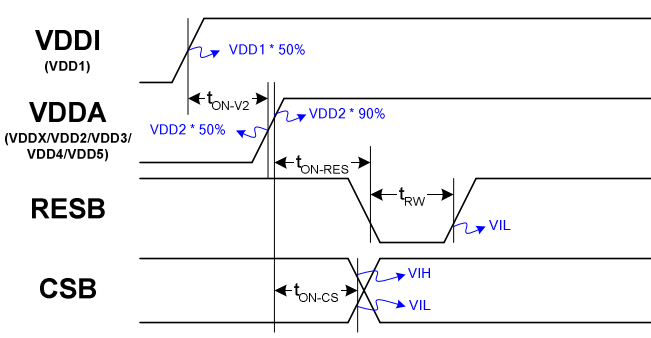## Temperature Gradient Compensation

This instruction is used to define the temperature gradient compensation coefficient. The temperature gradient compensation coefficient setting is shown as below table.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	1	0	0	
1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	Set temperature gradient
1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	compensation coefficient
1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	

MTx3	MTx2	MTx1	MTx0	Mx (mV/℃)
0	0	0	0	0
0	0	0	1	-5
0	0	1	0	-10
:	:	:	:	:
1	1	0	1	-65
1	1	1	0	-70
1	1	1	1	-75

OPERATION FLOW

Power ON

Referential Operation Flow	Operation Sequence
Power ON Flow \<Start\> (Sleep In Mode) Wait Power Stable, t>1ms (Depends on system power) Keep RESB=L … *1 Wait reset start, t>10us Set RESB=H … *1 Wait reset finished, t>120ms Default State … *2 Function Set (by user) (1) Auto Read Control (2) OTP WR/RD Control (3) OTP Read (4) OTP Control Out Function Set (by user) (1) Power Mode (SLPOUT) (2) Display OFF (3) Set Vop (4) BIAS System (5) Booster Level (6) Analog Control (7) N-Line Inversion (8) Display Mode (9) Enable DDRAM Interface (10) Display Control (11) Inversion Display Clear DDRAM by "0" (384 x 160 x 2) Function Set (by user) (1) Set Column Address (2) Set Row Address (3) Display ON Power ON Flow \<End\> (Sleep Out Mode)	**Case-1: RSTB=L while Power ON** **Case-2: RSTB=H while Power ON**

Note

1. Please refer to the specification of tRW and tR.
2. Refer to the section of RESET CIRCUIT.
3. The detail instruction functionality is described in section of INSTRUCTION DESCRIPTION.
4. The power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% od its rated voltage.

Item	Symbol	Requirement	Description
VDD2 power ON delay	t_{ON-V2}	No Limitation	• VDDI and VDDA can be applied in any order. IC will NOT be damaged when one of VDD1 and VDD2 is ON but another is OFF. • Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. • Recommend Setting: $-50ms \leq t_{ON-V2} \leq$ No Limitation.
RESB input time	t_{ON-RES}	Case-1 $t_{RW} \leq t_{ON-RES}$ Case-2 No Limitation	• RESB=L can be input at any time after power is stable. • t_{RW} & t_R should match the timing specification of RESB. • RESB has priority over CSB. • Recommend Setting: $0 \leq t_{ON-RES} \leq 50$ ms.
CSB input time	t_{ON-CS}	No Limitation	• CSB can be input at any time after power is stable.

Note:

1. If the contents of internal registers are the same as default, the related commands can be ignored.

2. If RESB is held high or unstable during power ON, a successful hardware reset by RSTB is required after VDDI and VDDA are both stable (as illustrated in Case-2). Otherwise, correct functionality can NOT be guaranteed.
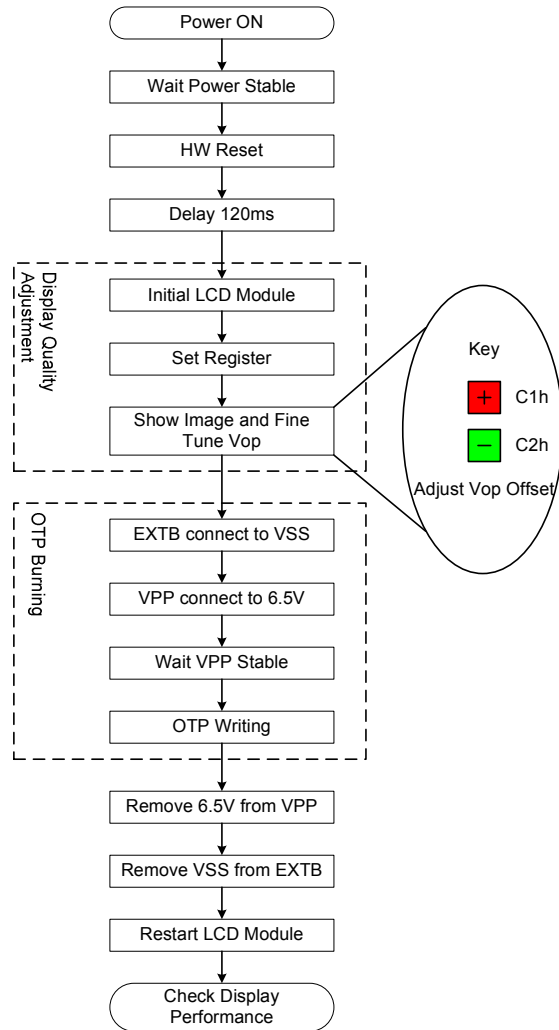
ST7586S

Power OFF

Referential Operation Flow	Operation Sequence

Referential Operation Flow:

Power OFF Flow <Start>
(Sleep Out Mode)
↓
Function Set (by user)
(1) Display OFF
(2) Power Mode (SLPIN)
↓
Wait 120ms
↓
Keep RESB=L
↓
Wait 200ms
↓
Power OFF
↓
Power OFF Flow <End>
(Sleep In Mode)

Operation Sequence:

Case-1: Use RSTB

Case-2: Power OFF at Sleep State

Item		Symbol	Requirement	Description
Power OFF Time	Case-1	$t_{OFF-RESB}$	$200ms \leq t_{OFF-RESB}$	● Power can be turned OFF after built-in power becomes VSS.
	Case-2	t_{OFF-PW}	$0 \leq t_{OFF-PW}$	
VDD2 power ON delay		t_{OFF-V2}	No Limitation	● VDD1 and VDD2 can be powered down in any order. IC will NOT be damaged when one of VDD1 and VDD2 is ON but another is OFF. ● Recommend Setting: $-50ms \leq t_{OFF-V2} \leq$ No Limitation.

Note: In Case-2, RSTB can fall to VSS at the same time as VDDI.

OTP Operation
Referential OTP Burning Flow

```
                    ( Power ON )
                          |
                 [ Wait Power Stable ]
                          |
                    [ HW Reset ]
                          |
                   [ Delay 120ms ]
                          |
  ┌─Display Quality─ ─ ─ ─ ─ ─ ─ ─┐
  │ Adjustment                      │
  │               [ Initial LCD Module ]      Key
  │                      |
  │                [ Set Register ]         [+] C1h
  │                      |
  │          [ Show Image and Fine          [−] C2h
  │              Tune Vop ]
  └ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─┘       Adjust Vop Offset
  ┌─OTP Burning─ ─ ─ ─ ─ ─ ─ ─ ─ ─┐
  │          [ EXTB connect to VSS ]
  │                      |
  │           [ VPP connect to 6.5V ]
  │                      |
  │             [ Wait VPP Stable ]
  │                      |
  │                [ OTP Writing ]
  └ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─┘
                          |
               [ Remove 6.5V from VPP ]
                          |
               [ Remove VSS from EXTB ]
                          |
                [ Restart LCD Module ]
                          |
                 ( Check Display
                    Performance )
```

Note:

- In this section "+" and "-" key button, please execute command C1h to increase one step at Vop and execute command C2h to decrease one step at Vop.

Referential OTP Operation Code

```
void Initialization_ST7586S(void)
{
        Reset_ms(10);
        Delay_ms(120);
        Write(Command, 0xD7);                    // Disable Auto Read
        Write(Data, 0x9F);
        Write(Command, 0xE0);                    // Enable OTP Read
        Write(Data, 0x00);
        Delay_ms(10);
        Write(Command, 0xE3);                    // OTP Up-Load
        Delay_ms(20);
        Write(Command, 0xE1);                    // OTP Control Out
        Write(Command, 0x11);                    // Sleep Out
        Write(Command, 0x28);                    // Display OFF
        Delay_ms(50);
        Write(Command, 0xC0);                    // Vop = B9h
        Write(Data, 0xB9);
        Write(Data, 0x00);
        Write(Command, 0xC3);                    // BIAS = 1/9
        Write(Data, 0x05);
        Write(Command, 0xC4);                    // Booster = x8
        Write(Data, 0x07);
        Write(Command, 0xD0);                    // Enable Analog Circuit
        Write(Data, 0x1D);
        Write(Command, 0xB5);                    // N-Line = 0
        Write(Data, 0x00);
        Write(Command, 0x39);                    // Monochrome Mode
        Write(Command, 0x3A);                    // Enable DDRAM Interface
        Write(Data, 0x02);
        Write(Command, 0x36);                    // Scan Direction Setting
        Write(Data, 0x00);
        Write(Command, 0xB0);                    // Duty Setting
        Write(Data, 0x9F);
        Write(Command, 0xB4);                    // Partial Display
        Write(Data, 0xA0);
        Write(Command, 0x30);                    // Partial Display Area = COM0 ~ COM119
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x77);
        Write(Command, 0x20);                    // Display Inversion OFF

        Write(Command, 0x2A);                    // Column Address Setting
        Write(Data, 0x00);                       // SEG0 -> SEG384
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x7F);
```

```
        Write(Command, 0x2B);                   // Row Address Setting
        Write(Data, 0x00);                       // COM0 -> COM160
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x9F);

        Clear_DDRAM();                           // Clear whole DDRAM by "0" (384 x 160 x 2)

        Write(Command, 0x2A);                    // Column Address Setting
        Write(Data, 0x00);                       // SEG0 -> SEG239
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x4F);
        Write(Command, 0x2B);                    // Row Address Setting
        Write(Data, 0x00);                       // COM0 -> COM120
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x78);

        Disp_Image();                            // Fill the DDRAM Data by Panel Resolution

        Write(Command, 0x29);                    // Display ON
    }
```

```
void Set_OTP_Register(void)
{
        Write(Command, 0xB5);                   // N-Line = 13 Line Inversion (Non-Reset)
        Write(Data, 0x8C);
}


void Vop_Fine_Tune(v
{
        Disp_Image();                           // Display the image

        Write(Command, 0x29);                   // Display ON

        Write(Command, 0xC1);                   // Fine tuning Vop to adjust display quality
        or
        Write(Command, 0xC2);
}


void OTP_Write(void)
{
        Write(Command, 0x28);                   // Display OFF
        Delay_ms(50);                           // Delay 50ms

        Write(Command, 0xF1);                   // Frame Rate = 77Hz
        Write(Data, 0x12);
        Write(Data, 0x12);
        Write(Data, 0x12);
        Write(Data, 0x12);

        Write(Command, 0xE4);                   // OTP Selection Control
        Write(Data, 0x59);
        Write(Command, 0xE5);                   // OTP Programming Setting
        Write(Data, 0x0F);
        Write(Command, 0xE0);                   // OTP WR/RD Control
        Write(Data, 0x20);
        Delay_ms(100);                          // Delay 100ms
        Write(Command, 0xE2);                   // OTP Write
        Delay_ms(100);                          // Delay 100ms
        Write(Command, 0xE1);                   // OTP Control Out
}
```

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ABSOLUTE MAXIMUM RATINGS

VSS=0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	−0.3 ~ 3.6	V
Analog Power supply voltage	VDDA (VDD2~VDD5)	−0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0	−0.3 ~ 19	V
LCD Power supply voltage	VG	−0.3 ~ 5.5	V
LCD Power supply voltage	VM	−0.3 ~ VDDA+0.3	V
MPU Interface Input Voltage	Vin	−0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	−30 to +80	℃
Storage temperature	TSTR	−40 to +125	℃

Note:

1. All voltages are respect to VSS unless otherwise noted (VSS=VSS1=VSS2=VSS4=VSSX).
2. Stresses exceed the ranges listed above may cause permanent damage to IC.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Insure the voltage levels of V0, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VG > VM > VSS ≥ XV0

DC CHARACTERISTICS

VSS=VSS1=VSS2=VSS4=VSSX=0V and Ta = −30 ~ 85 ℃, unless otherwise specified.

Item	Symbol	Condition		Related Pin	Rating			Unit
					Min.	Typ.	Max.	
Digital Operating Voltage	VDDI			VDD1	1.7	–	3.4	V
Analog Operating Voltage	VDDA			VDD2~5	2.7	–	3.4	V
Input High-level Voltage	V_{IH}			MPU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}			MPU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}	I_{OH}=1.0mA, VDD1=3.0V		D[7:0] TE	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}	I_{OL}=−1.0mA, VDD1=3.0V		D[7:0] TE	VSS1	–	0.2*VDD1	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS		MPU Interface	−1.0	–	1.0	µA
ON Resistance of LCD Drivers	R_{ON}	Ta=25℃	Vop=16V, ΔV=10%	COM Drivers	–	1.0	–	KΩ
			VG=3.2V, ΔV=10%	SEG Drivers	–	1.0	–	KΩ
Frame Frequency	f_{FR}	VDDI=VDDA=3.3V, N-Line OFF, FR=0x12, Duty=1/160, Ta = 25℃		–	–	77	–	Hz
Vop Voltage Output	Vop	VDDI=VDDA=3.3V		V0-XV0[1,2]	–	–	18	V
VG Voltage Output	VG	VDDI=VDDA=3.3V		VG[1,2]	1.8	–	5	V
VM Voltage Output	VM	VDDI=VDDA=3.3V		VM[2]	0.9	–	VDDA-0.7	V

Note:

1. V0, XV0 and VG include: V0I, V0O, V0S, XV0I, XV0O, XV0S, VGI, VGO & VGS.

2. V0, XV0, VG and VM do NOT support external power supply.

The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display ON Pattern: SNOW (Static)	ISS	VDDI=VDDA=3.3V, 8x Booster, Vop = 16V, Bias=1/10 N-Line OFF, f_{FR}=77Hz, Ta=25°C	–	800	1000	µA
Sleep In	ISS	VDDI=VDDA=3.3V, Ta=25°C	–	20	25	µA

Note: The current is DC characteristic of a "Bare Chip".

TIMING CHARATERISTIC

System Bus Timing for 8080 MCU Interface
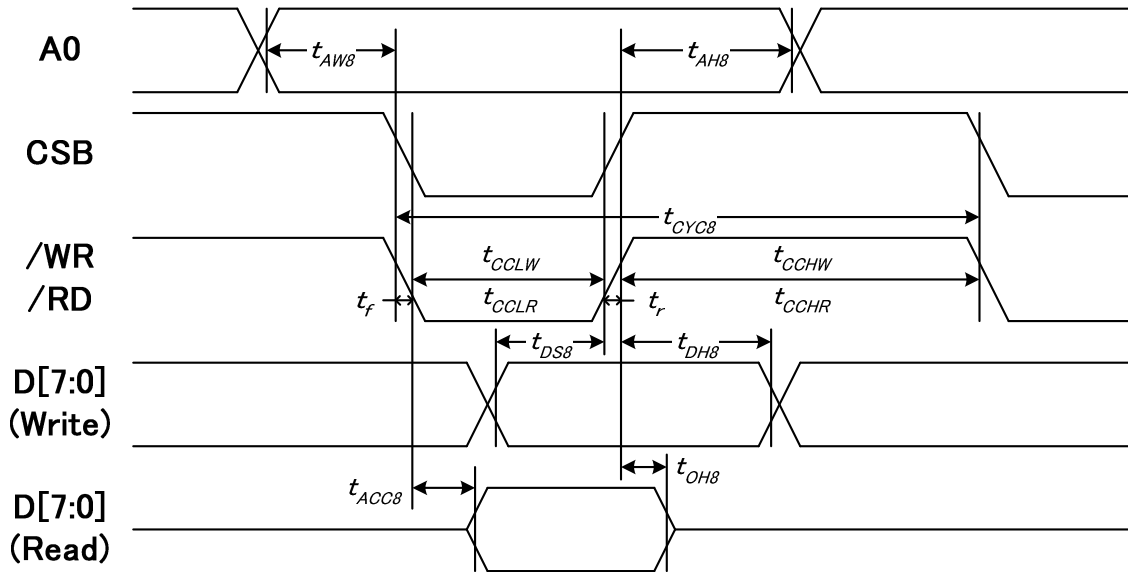
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
System cycle time (READ)	RD	tCYC8		500	—	
/RD L pulse width (READ)		tCCLR		220		
/RD H pulse width (READ)		tCCHR		220		
WRITE Data setup time	D[7:0]	tDS8		20	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) $\leq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leq$ (tCYC8 – tCCLR – tCCHR) are specified.

2. All timing is specified using 20% and 80% of VDD1 as the reference.

3. tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

System Bus Timing for 6800 MCU Interface
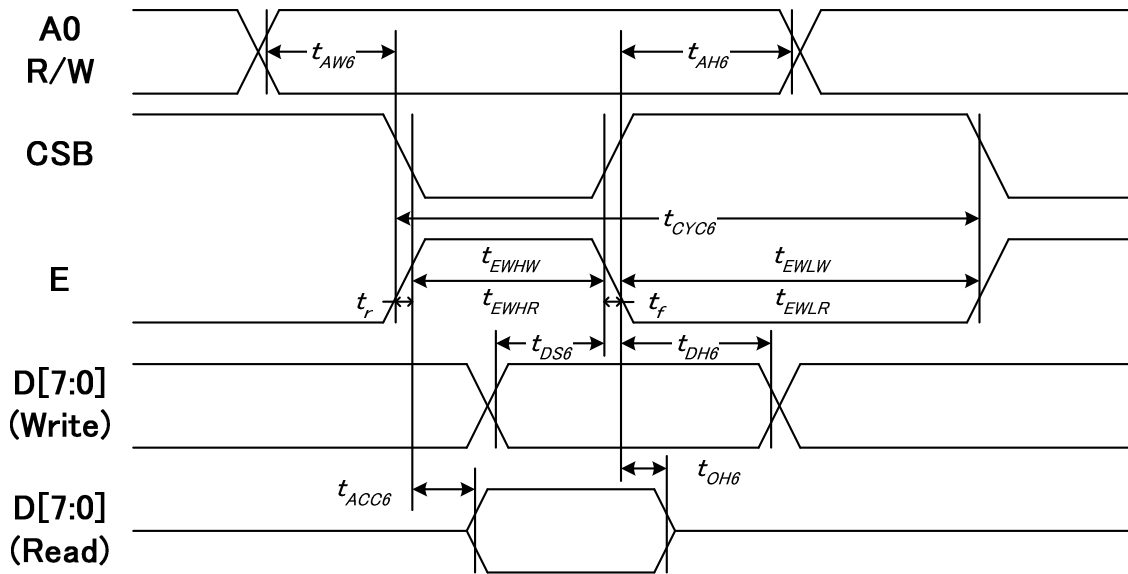
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time (WRITE)	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		100	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
System cycle time (READ)		tCYC6		500		
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		220		
Write data setup time	D[7:0]	tDS6		20	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	100	
Read data output disable time		tOH6	CL = 16 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) $\leq$ (tCYC6 – tEWLW – tEWHW) for (tr + tf) $\leq$ (tCYC6 – tEWLR – tEWHR) are specified.

2. All timing is specified using 20% and 80% of VDD1 as the reference.

3. tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

System Bus Timing for 4-Line SPI MCU Interface
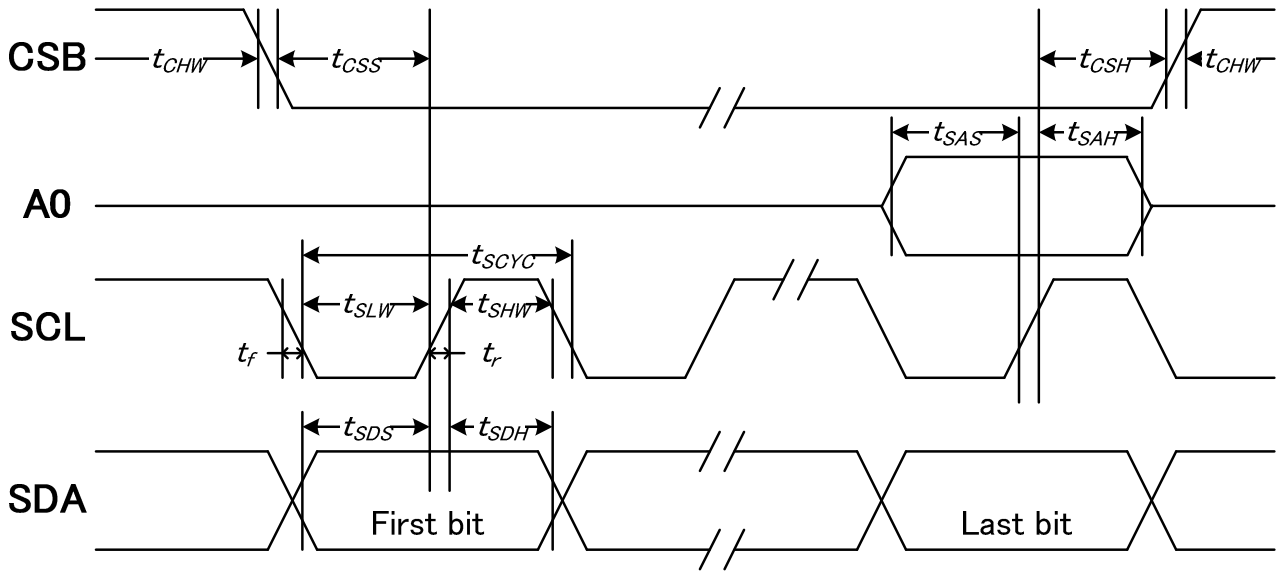
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		100	—	ns
SCLK "H" pulse width		tSHW		45	—	
SCLK "L" pulse width		tSLW		45	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		20	—	
CS "H" pulse width		tCHW		0	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

2. All timing is specified using 20% and 80% of VDD1 as the standard.

System Bus Timing for 3-Line SPI MCU Interface
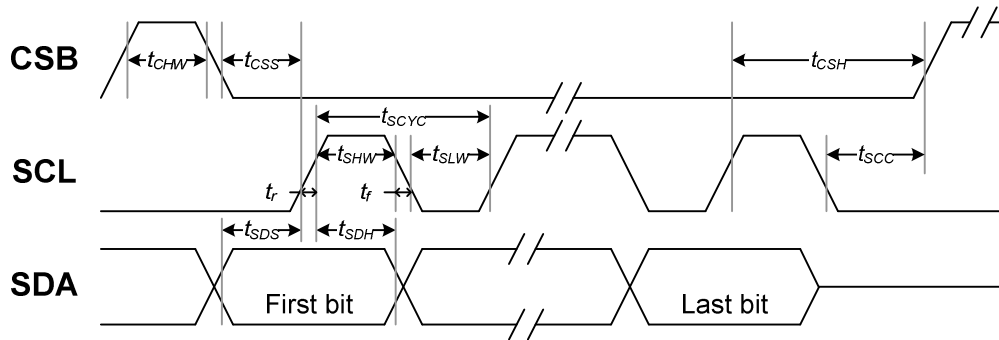
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		45	—	
SCL "L" pulse width		tSLW		45	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
		tCSH		30	—	
CS "H" pulse width		tCHW		0	—	

Note:

1.   The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

2.   All timing is specified using 30% and 70% of VDD1 as the standard.

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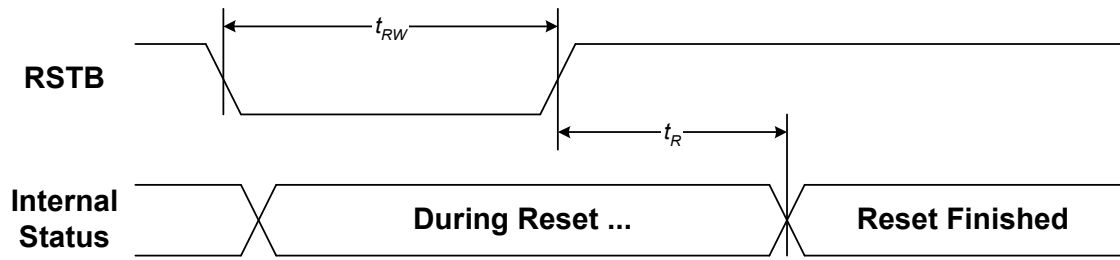
Reset Timing

VDD1 = 1.8~3.3V, Ta = 25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		120	—	ms
Reset "L" pulse width	tRW		10	—	us

APPLICATION NOTE

ITO Layout Guide

The ITO layout suggestion is shown as below:

- **For V0, XV0, VG, VDD and VSS**
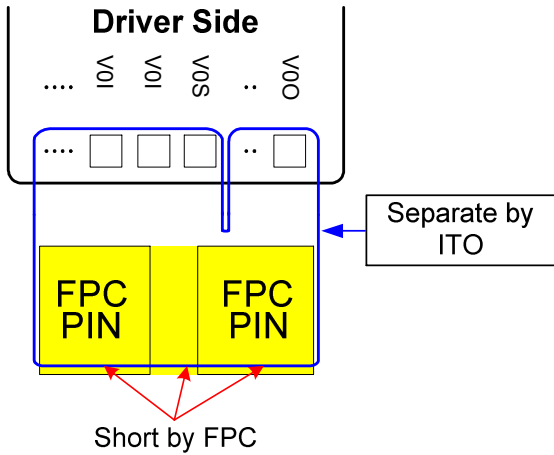
Fig. 14   V0 ITO Layout
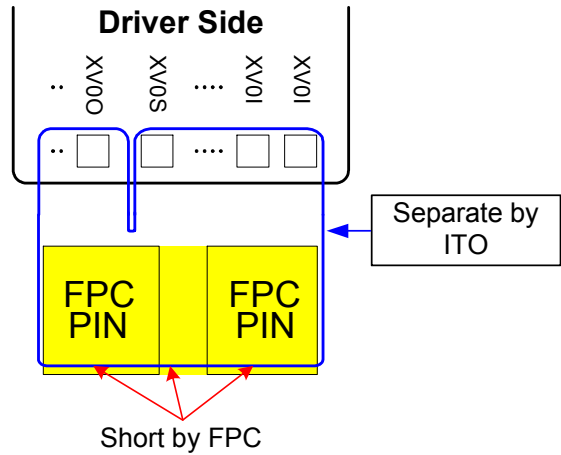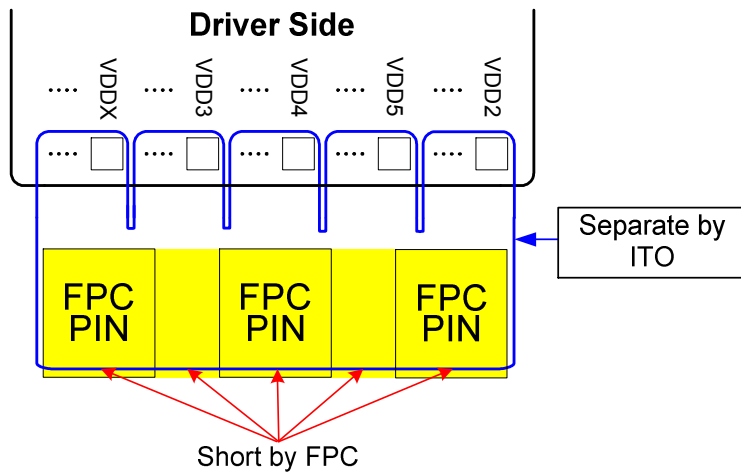

Fig. 15   XV0 ITO Layout
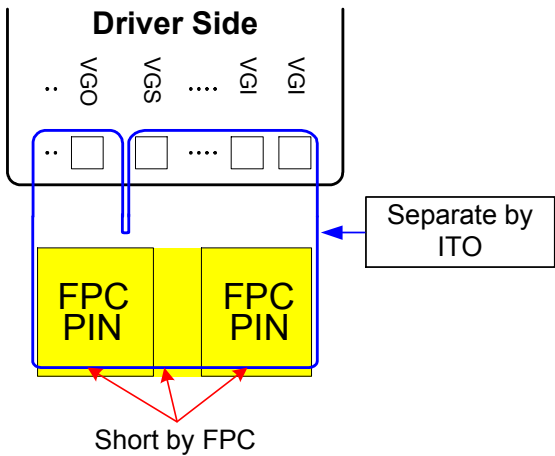
Fig. 16   VG ITO Layout
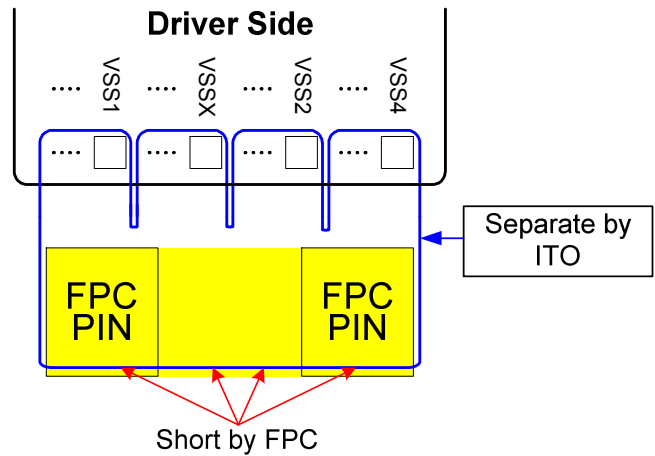
Fig. 17   VSS ITO Layout

Fig. 18   VDD ITO Layout

ST7586S

- **For VPP**

  This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

- **Enhance ESD performance for COG application**

  1. Increase RSTB resistance:

  Fig. 19   RSTB ITO Layout

  2. Add ESD protection ring:
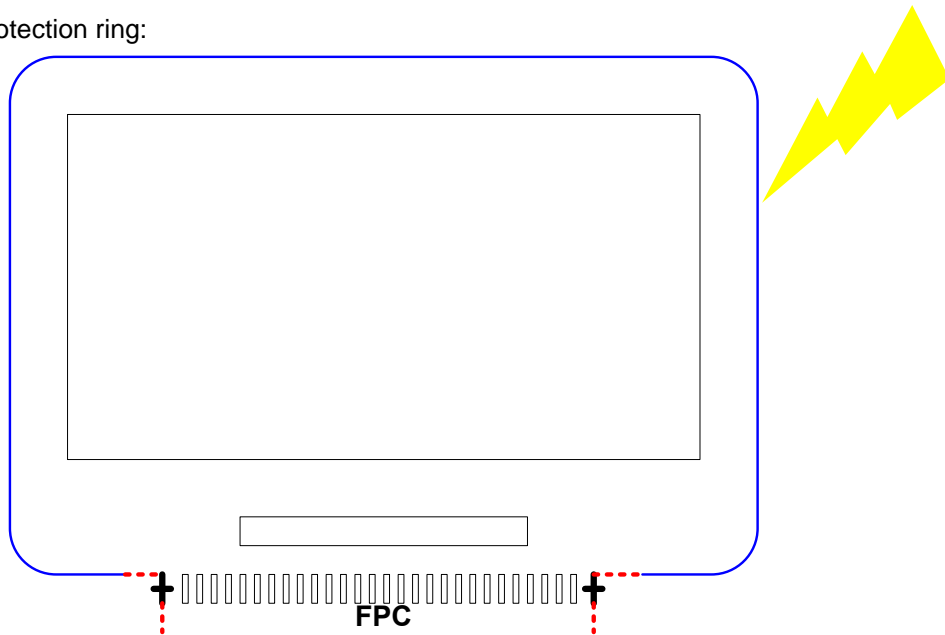
  Fig. 20 Air ESD Protection Ring

ST7586S

Selection of Liquid Crystal

Referential LCD Module Setting

VDD1=2.8V, VDD2=VDD3=VDD4=VDD5=VDDX=2.8V, Panel Size=3.0", Booster Level=X8, N-Line=Frame Inversion

Display Mode	Recommended Parameter of Liquid Crystal		
	Duty	BIAS	Vop Range
Gray Scale	80	1/9	9.0 ~ 12.3
		1/10	11.5 ~ 13.5
	160	1/10	11.5 ~ 13.5
		1/11	12.5 ~ 13.5
Monochrome	80	1/9	9.0 ~ 14.0
		1/10	11.5 ~ 14.0
	160	1/10	11.5 ~ 14.0
		1/11	12.5 ~ 14.0

● In different range of partial area, the Vop and BIAS setting must within the Recommended Parameter of Liquid Crystal after consider the temperature effect and user adjustment.

Note:

● Positive Booster: *(VDD2 x BL x BE) $\geqq$ V0* or *(VDD2 x BL x BE) $\geqq$ Vop*

● Negative Booster: *[-VDD2 x (BL – 1) x BE] $\leqq$ XV0* or *[VDD2 x (BL – 1) x BE] $\leqq$ (Vop – VG)*, where VG = Vop x 2 / N

● Vop requirement:
   VDD2 x (BL – 1) x BE $\geqq$ Vop x (N – 2) / N or *Vop $\leqq$ VDD2 x (BL – 1) x BE x N / (N-2)*, where N is bias rate.

● BL is the booster level and BE is the booster efficiency.
   Referential value are listed below: (assume VDD2~VDD5=2.8V and BL=X8)
   Module Size = 2.0"~3.0": BE=70% (Typical)
   Actual BE should be determined by module loading and ITO resistance value.

● 1.6V $\leqq$ VG < 2 x VDD2.
   Recommend VG is: VDD2-VG around 0.3~0.5V.

● VM=VG/2 and 0.8V $\leqq$ VM < VDD2

● The ITO resistance restriction of LCD module please refers to the table of ITO Resistance Limitation.

ST7586S

Application Circuit
Parallel 8080 Interface

ST7586S

Parallel 6800 Interface

4-Line SPI Interface

3-Line SPI Interface

REVERSION HISTORY

Version	Date	Description
0.1	2009/06/29	• Redraw figures. • Fix naming issue. • Fix font error.
0.1a	2009/06/30	• Add Page 52 & 53. • Fix VDDI/VDDA range.
0.2	2009/07/01	• Fix VDD1 naming in PAD CENTER COORDINATES.
0.3	2009/07/10	• Fix pin description mistakes.
0.3a	2009/07/13	• Rename as ST7586S Fix typing mistakes in • DC CHARACTERISTICS.
0.4	2009/08/15	• Modify section of FUNCTION DESCRIPTION,. • Add sections of RESET CIRCUIT, INSTRUCTION TABLE, INSTRUCTION DESCRIPTION, OPERATION FLOW and TIMING CHARATERISTIC.
0.4a	2009/09/17	• Modify the description of VG power pin. • Modify the range of ITO Resistance Limitation. • Modify the instructions of Inverse Display and All Pixel ON/OFF.
0.5	2009/10/06	• Add the display mode of 4-level gray scale. • Modify the operating voltage range. • Modify the bump height. • Add the physical description of L-Mark. • Modify the range of ITO Resistance Limitation. • Modify the capacity of DDRAM. • Modify the table of RESET CIRCUIT. • Modify the range of operating temperature. • Add the section of "Selection of Liquid Crystal". • Add the OTP burning flow and the referential OTP burning code.
1.0	2009/10/28	• Modify the mistake of DC CHARACTERISTICS. • Modify the description of ABSOLUTE MAXIMUM RATINGS. • Add the specification of TIMING CHARATERISTIC. • Add the referential operation flows of Power ON and Power OFF. • Remove the T.B.D mark.
1.1	2009/11/24	• Modify the operating voltage range of VDD1.
1.1a	2009/11/30	• Modify the mistake of N-Line Inversion. • Add the instruction of Frame Rate for 4-level gray scale mode. • Modify the mistake of Referential OTP Operation Code. • Add figure of DDRAM Mapping.
1.1b	2009/12/23	• Modify description of Part Number and Bump Height. • Modify the value of TIMING CHARATERISTIC. • Modify the mistake of Application Circuit.
1.2	2010/02/05	• Add application circuit for parallel 6800, 4-Line SPI and 3-Line SPI.
1.2a	2010/05/28	• Add tCHW for 4-Line SPI MCU Interface. • Modify the mistake of system timing for 3-Line SPI MCU Interface.
1.3	2010/11/12	• Modify the description of Display Control. • Modify the VDD1 range of TIMING CHARATERISTIC.
1.3a	2010/11/25	• Modify Application Circuit.

1.4	2011/06/22	● Add 16-level gray scale mode. ● Add initial condition for RESET CIRCUIT. ● Modify recommended condition for Selection of Liquid Crystal.
1.5	2012/08/29	● Remove Vop Offset Command.
1.6	2012/09/24	● Modify Reset Default Value.