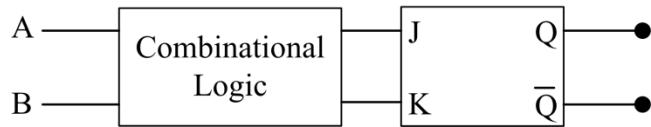


10<sup>th</sup> November, 2016**Home Assignment – 13**

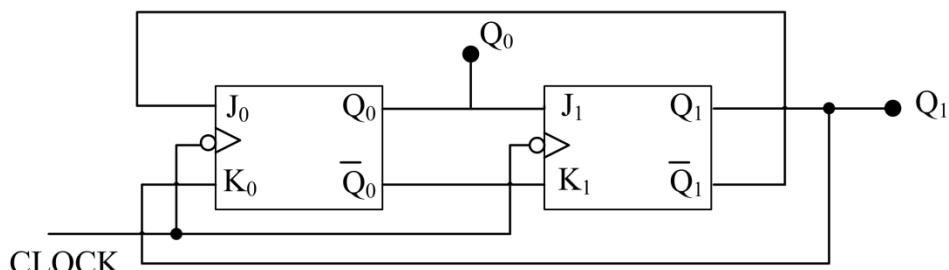
1. (a) Realize a **D** flip flop from **T** flip flop and vice-versa.  
 (b) Convert a **JK** flip flop to **D** flip flop.
2. Give a circuit realization of the combinational logic block shown in **Fig. 1(a)** to obtain the truth table shown in **Fig. 1(b)**.

**Fig. 1(a)**

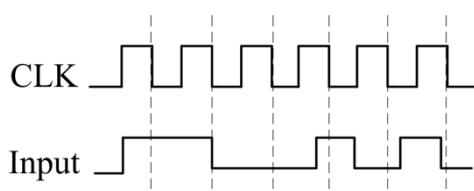
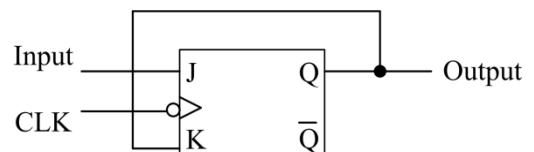
A	B	Q
0	0	$\bar{Q}_n$
0	1	1
1	0	$Q_n$
1	1	0

**Fig. 1(b)**

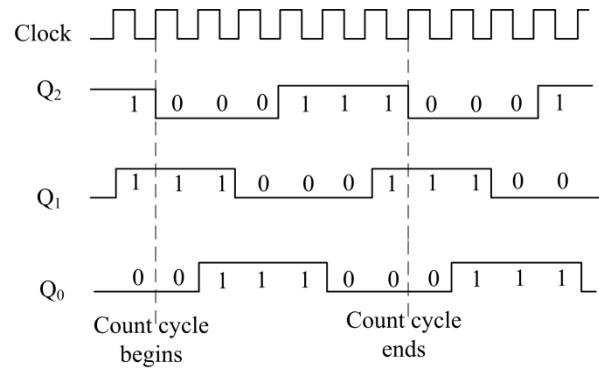
3. A sequential circuit with two **D** flip flops (**A** and **B**), two inputs **X** and **Y** and one output **Z** is specified by the input equations,  $D_A = \bar{X}.Y + X.A$ ,  $D_B = \bar{X}.B + X.A$  and  $Z = X.B$ .
  - a) Draw logic diagram of the circuit.
  - b) Derive the state table.
  - c) Derive the state diagram.
4. In **Fig. 2** initially  $Q_0 = Q_1 = 0$ . Find the logic states of  $Q_0$  and  $Q_1$  immediately after 777<sup>th</sup> clock pulse.

**Fig. 2**

5. The waveform of the clock as shown in **Fig. 3(a)** excites the circuit shown in **Fig. 3(b)**. Sketch the output waveform.

**Fig. 3(a)****Fig. 3(b)**

6. Design a **synchronous counter** using **JK** flip flops with the following binary sequences 4, 1, 3, 7, 6, 4, 1, ..... (States which do not arise should be treated as “**don’t care**” conditions).
7. Design a **synchronous** counter with three **positive edge triggered JK** flip flops using K-maps for the three pairs of inputs  $J_2\ K_2$ ;  $J_1\ K_1$  and  $J_0\ K_0$  to produce 3 phase waveforms at the outputs of the three flip flops  $Q_2$ ,  $Q_1$  and  $Q_0$  respectively as shown in **Fig. 4**. (States which do not arise should be treated as “**don’t care**” conditions).

**Fig. 4**

8. Design a **3- bit asynchronous counter** which counts 0, 3, 6, 1, 4, 7, 2, 5, 0, 3,... using **JK** flip flops.
9. Design a **BCD Ripple down counter** using **JK** flip flops.

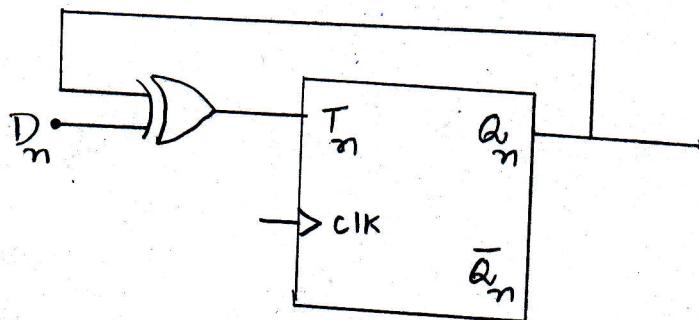
a)

$Q_n$	$\bar{Q}_{n+1}$	$D_n$	$T_n$
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

To realize D-flip flop from T-flip flop, we have to express  $T_n$  in terms of  $D_n$  and  $Q_n$ .

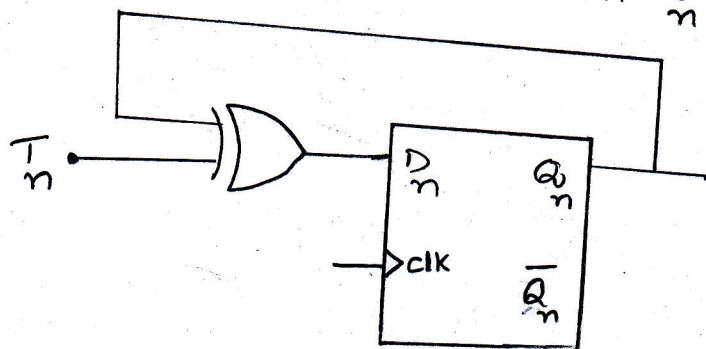
$$\text{So, } T_n = D_n \bar{Q}_n + \bar{D}_n Q_n = D_n \oplus Q_n$$

The logic diagram is,



To realize T-flip flop from D-flip flop, we have to express  $D_n$  in terms of  $T_n$  and  $Q_n$ .

$$\text{So, } D_n = T_n \bar{Q}_n + \bar{T}_n Q_n = T_n \oplus Q_n$$

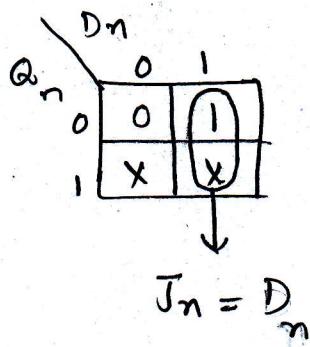


is the desired logic diagram.

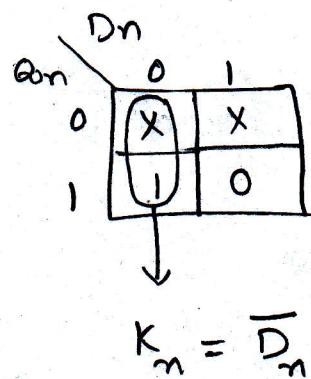
b) JK flip flop to D-flip flop.

$Q_n$	$Q_{n+1}$	$J_n$	$K_n$	$D_n$
0	0	0	X	0
0	1	1	X	1
1	0	X	1	0
1	1	X	0	1

Now using K-map we find the relation between  $J$  and  $D$  and  $K$  and  $D$ :

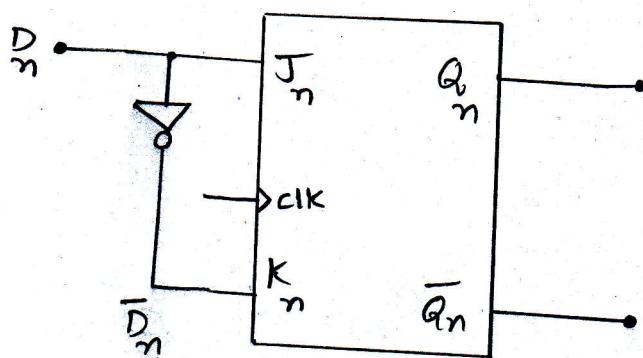


$$J_n = D_n$$



$$K_n = \overline{D_n}$$

Finally, the logic diagram becomes



The given truth table is,

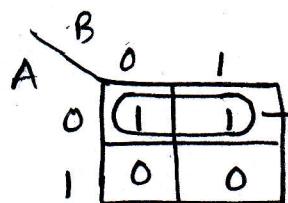
A	B	Q
0	0	$\bar{Q}_n$
0	1	1
1	0	$Q_n$
1	1	0

To obtain above 'Q' values for a given 'A-B' combination, we need following values of 'J' and 'K'.

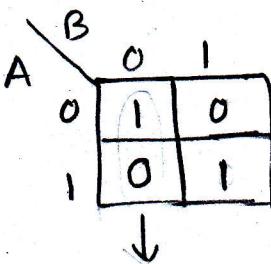
A	B	J	K	Q
0	0	1	1	$\bar{Q}_n$
0	1	1	0	1
1	0	0	0	$Q_n$
1	1	0	1	0

To give the circuit realization of the combinational logic block, we have to express its output (J,K) in terms of its input (A,B).

This is done as shown below.



$$J = \bar{A}$$

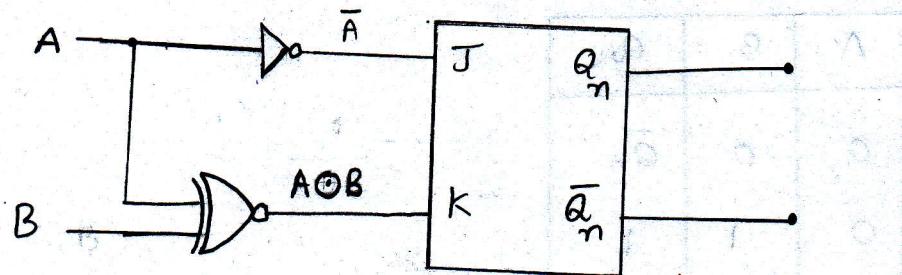


$$K = \bar{A}\bar{B} + A\cdot B$$

$$= A \oplus B$$

The final logic diagram is,

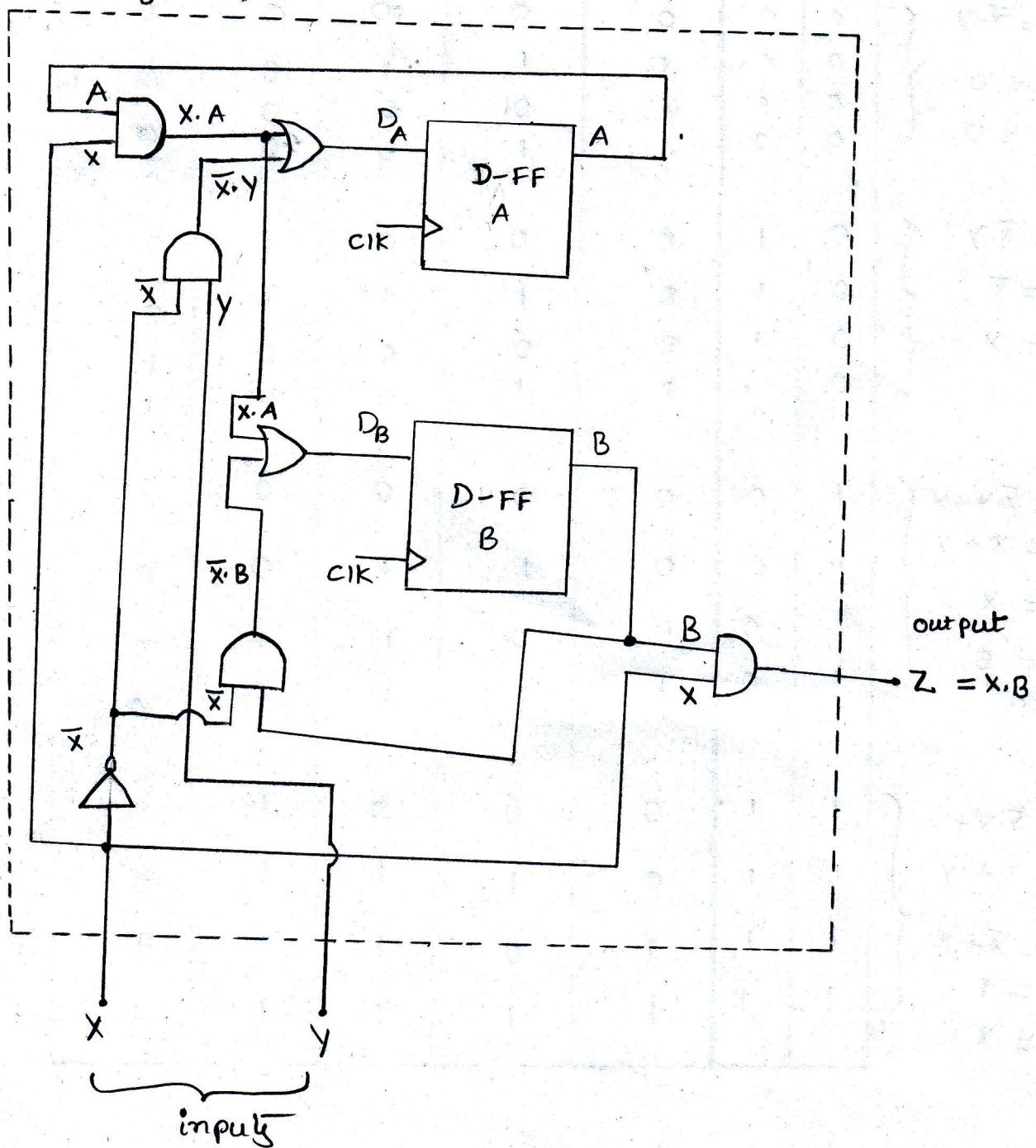
P-1



given  $D_A = \bar{X} \cdot Y + X \cdot A$

$D_B = \bar{X} \cdot B + X \cdot A$  and  $Z = X \cdot B$ .

a) logic diagram,



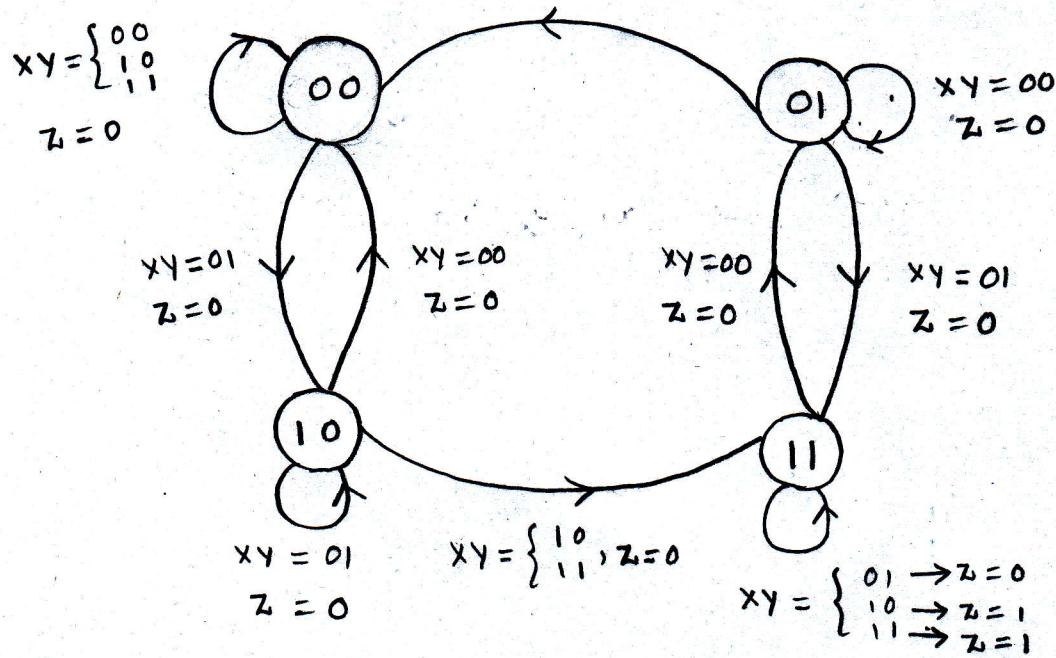
b) State Table : Represents present states ( $A_n, B_n$ ), next states ( $A_{n+1}, B_{n+1}$ ), input ( $x, y$ ) and output ( $z$ ).

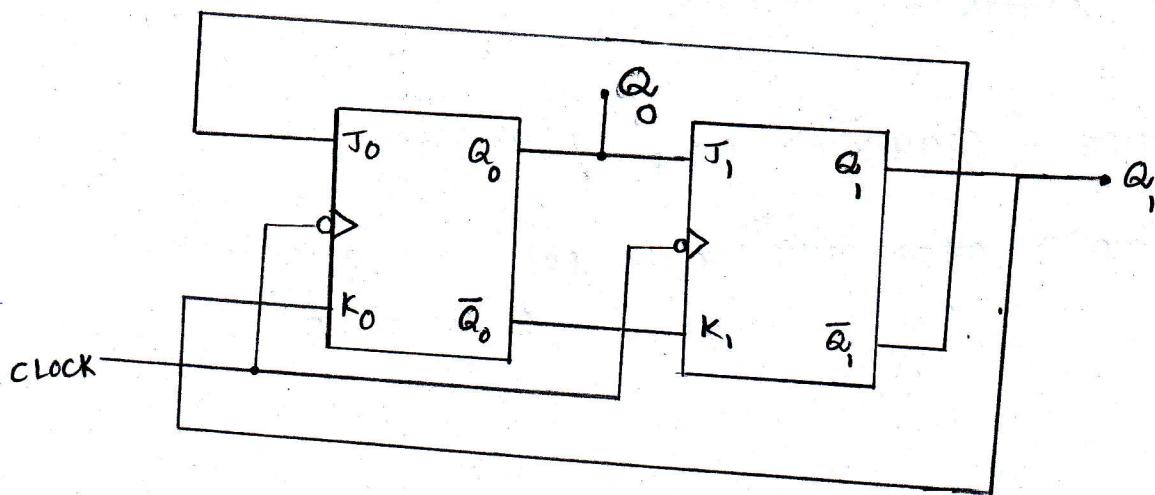
$A_n$	$B_n$	$X$	$Y$	$A_{n+1}$	$B_{n+1}$	$Z$
$D_A = \bar{X} \cdot Y$	0	0	0	0	0	0
	0	0	0	1	0	0
	0	0	1	0	0	0
	0	0	1	0	0	0
$D_B = 0$	0	1	0	0	1	0
	0	1	0	1	1	0
	0	1	1	0	0	1
	0	1	1	0	0	1
$Z = 0$	0	1	0	0	1	0
	0	1	0	1	1	0
	0	1	1	0	0	1
	0	1	1	0	0	1
$D_A = \bar{X} \cdot Y$	1	0	0	0	0	0
	1	0	0	1	0	0
	1	0	1	0	1	0
	1	0	1	1	1	0
$D_B = X$	1	1	0	0	1	0
	1	1	0	1	1	0
	1	1	1	0	1	1
	1	1	1	1	1	1
$Z = 0$	1	1	0	0	1	0
	1	1	0	1	1	0
	1	1	1	0	1	1
	1	1	1	1	1	1
$D_A = \bar{X} \cdot Y + X$ $= X + Y$	1	1	0	0	0	0
	1	1	0	1	0	0
	1	1	1	0	1	0
	1	1	1	1	1	0
$D_B = X$	1	1	0	0	1	0
	1	1	0	1	1	0
	1	1	1	0	1	1
	1	1	1	1	1	1
$Z = 0$	1	1	0	0	1	0
	1	1	0	1	1	0
	1	1	1	0	1	1
	1	1	1	1	1	1
$D_A = \bar{X} \cdot Y + X$ $= X + Y$	1	1	0	0	0	0
	1	1	0	1	0	0
	1	1	1	0	1	0
	1	1	1	1	1	0
$D_B = \bar{X} + X$ $= 1$	1	1	0	0	1	1
	1	1	0	1	1	1
	1	1	1	0	1	1
	1	1	1	1	1	1
$Z = X$	1	1	0	0	1	0
	1	1	0	1	1	0
	1	1	1	0	1	1
	1	1	1	1	1	1

c) state diagram.

The information available in state table can be shown graphically using a state diagram.

$$xy = \{ \begin{matrix} 10 \\ 11 \end{matrix}, z=1$$





The characteristic table of a JK flip flop is,

J	K	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$$(J_0 = \bar{Q}_1; J_1 = Q_0 \\ K_0 = Q_1; K_1 = \bar{Q}_0)$$

The logic states for successive clock pulses are shown below.

	$Q_0$	$Q_1$	$J_0$	$K_0$	$J_1$	$K_1$	$Q_0(n+1)$	$Q_1(n+1)$
After 1 <sup>st</sup> clock	0	0	1	0	0	0	1	1
After 2 <sup>nd</sup> clock	1	0	1	0	1	0	1	0
After 3 <sup>rd</sup> clock	1	1	0	1	1	0	0	1
After 4 <sup>th</sup> clock	0	1	0	1	0	1	0	1
After 5 <sup>th</sup> clock	0	0	1	0	0	1	0	0
After 6 <sup>th</sup> clock	1	0	1	0	1	0	1	1

The above logic states reveal that after every 4 clock pulses the states will repeat.

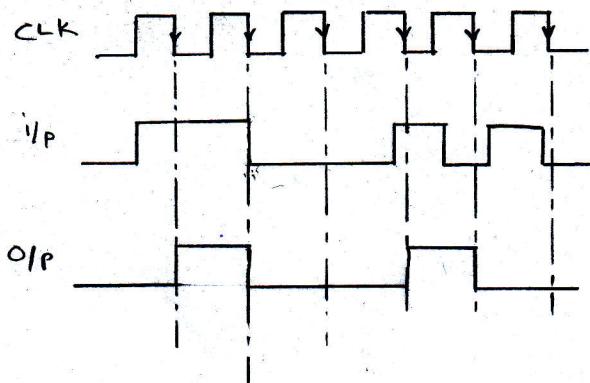
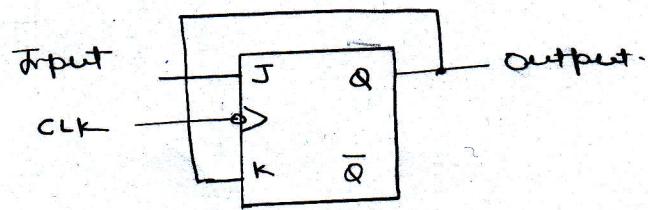
Now,

$$777 = (194 \times 4) + 1$$

This implies after 777<sup>th</sup> clock pulse we arrive at

$$Q_0 \cdot Q_1 = 10.$$

$\therefore$  J-K flip flop is -ve edge triggered.



$\therefore$  for J-K flip flop

$$Q(t+1) = J\bar{Q} + KQ.$$

$$\because K = Q \quad \& \quad \bar{Q}Q = 0.$$

$$\Rightarrow Q(t+1) = J\bar{Q}$$

∴ counts are 4, 1, 3, 7, 6, 4, 1  
so 3 flip flops are required.

P.S. N.S.

$Q_A$	$Q_B$	$Q_C$	$Q_A$	$Q_B$	$Q_C$	$J_A$	$K_A$	$J_B$	$K_B$	$J_C$	$K_C$
1	0	0	0	0	1	X	1	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	1	1	1	1	X	X	0	X	0
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	0	X	0	X	1	0	X

all unused states are don't cares.

$J_A$

$Q_A \backslash Q_B Q_C$

		00	01	11	10
0	0	X	0	1	X
	1	X	X	X	X

$K_A$

$Q_A \backslash Q_B Q_C$

		00	01	11	10
0	0	X	X	X	X
	1	1	X	0	0

$J_B$

$Q_A \backslash Q_B Q_C$

		00	01	11	10
0	0	X	1	X	X
	1	0	X	X	X

$K_B$

$Q_A \backslash Q_B Q_C$

		00	01	11	10
0	0	X	X	0	X
	1	X	X	0	1

$$J_B = Q_C$$

$$K_B = \bar{Q}_C$$

(or  $J_B = \bar{Q}_A$  : another solution)

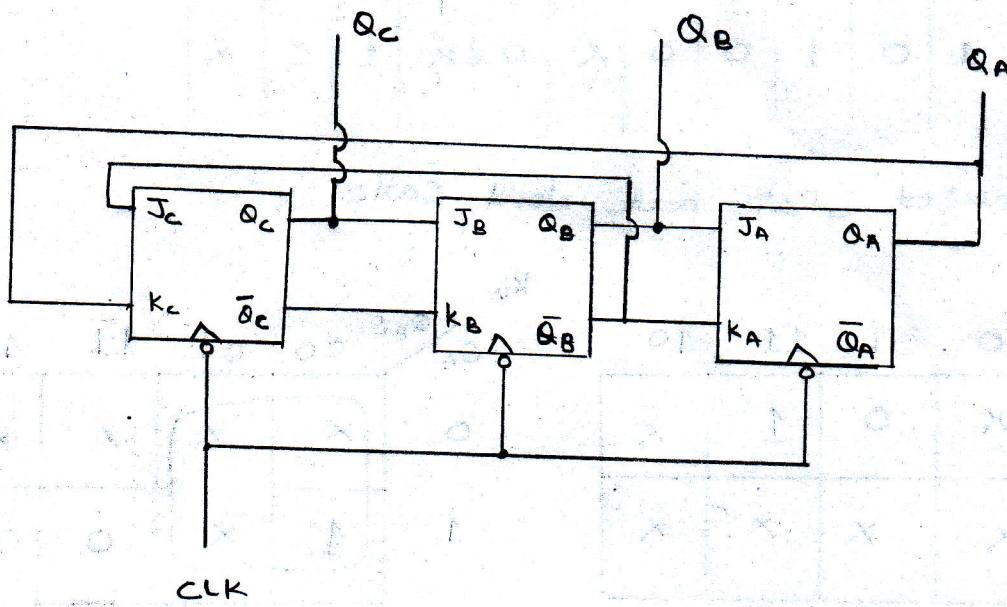
$J_C$	$Q_A$	$Q_B$	$Q_C$	00	01	11	10
0	$X$	$X$	$X$	$X$	$X$	$X$	$X$
1	1	$X$	$X$	$X$	$X$	0	0

$J_C$	$Q_A$	$Q_B$	$Q_C$	00	01	11	10
0	0	$X$	$O$	$O$	$X$	$O$	$X$
1	$X$	$X$	1	$X$	$X$	1	$X$

$$J_C = \bar{Q}_B$$

$$K_C = Q_A$$



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P.S.: Present State

N.S.: Next State

P.S.			N.S.								
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	0	0	1	0	x	x	1	x	0
0	0	1	1	0	1	1	x	0	x	x	0
1	0	1	1	0	0	x	0	0	x	x	1
1	0	0	1	1	0	x	0	1	x	0	x
1	1	0	0	1	0	x	1	x	0	0	x

$J_2$  \  $Q_2 Q_0$

	00	01	11	10
0	x 1	0 0		
1	x x	x x		

$$J_2 = \overline{Q_1}$$

$K_2$  \  $Q_2 Q_0$

	00	01	11	10
0	x x	x x	x x	
1	0 0	x x	x 1	1

$$K_2 = Q_1$$

$J_1$  \  $Q_2 Q_0$

	00	01	11	10
0	x	0	x	x
1	1	0	x	x

$$J_1 = \overline{Q_0}$$

$K_1$  \  $Q_2 Q_0$

	00	01	11	10
0	x	x	1	0
1	x	x	x	0

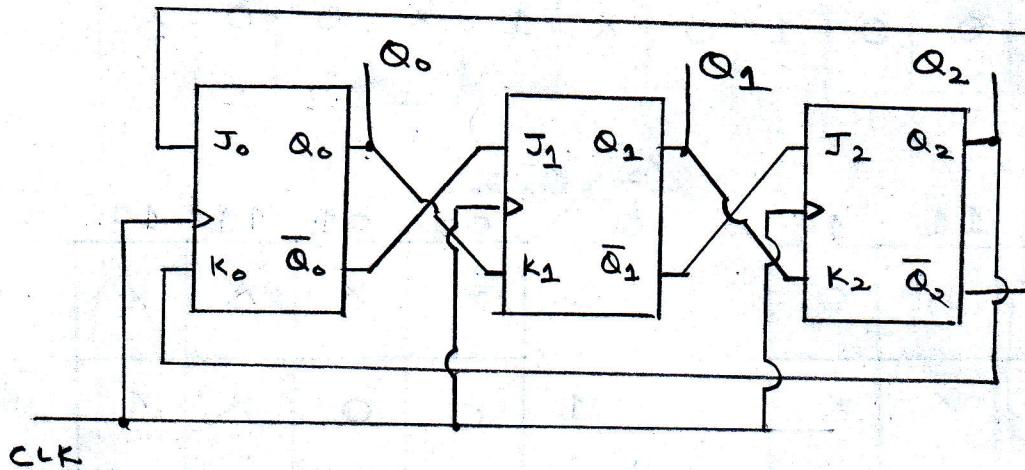
$$K_1 = Q_0$$

$J_0$	$Q_2 \bar{Q}_0$	00	01	11	10
0	$\times$	$\times$	$\times$	1	
1	0	$\times$	$\times$	0	

$K_0$	$Q_2 \bar{Q}_0$	00	01	11	10
0	0	$\times$	0	0	$\times$
1	$\times$	1	$\times$	$\times$	$\times$

$$J_0 = \overline{Q_2}$$

$$K_0 = Q_2.$$



∴ counts are 0, 3, 6, 1, 4, 7, 2, 5, 0, 3.

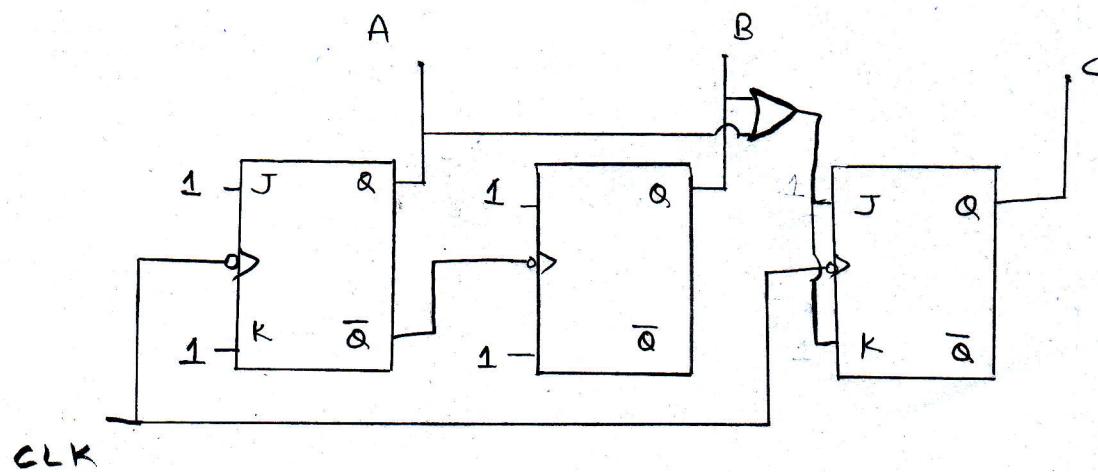
MSB

C	B	A
0	0	0
0	1	1
1	1	0
0	0	1
1	0	0
1	1	1
0	1	0
1	0	1
0	0	0

- here Bit A toggles at each step.
- Bit B changes its state when Bit A shows transition from low to high.
- Bit C changes its state whenever atleast one of the previous value of A or B is '1'.

$$C(n+1) = \overline{C(n)} \text{ if } A(n)+B(n)=1$$

$$\text{and } C(n+1)=C(n) \text{ if } A(n)+B(n)=0$$



$\therefore$  This is a BCD Ripple Down Counter.

$\therefore$  Output sequence is 0, 9, 8, 7, 5, 4, 3, 2, 1, 0...

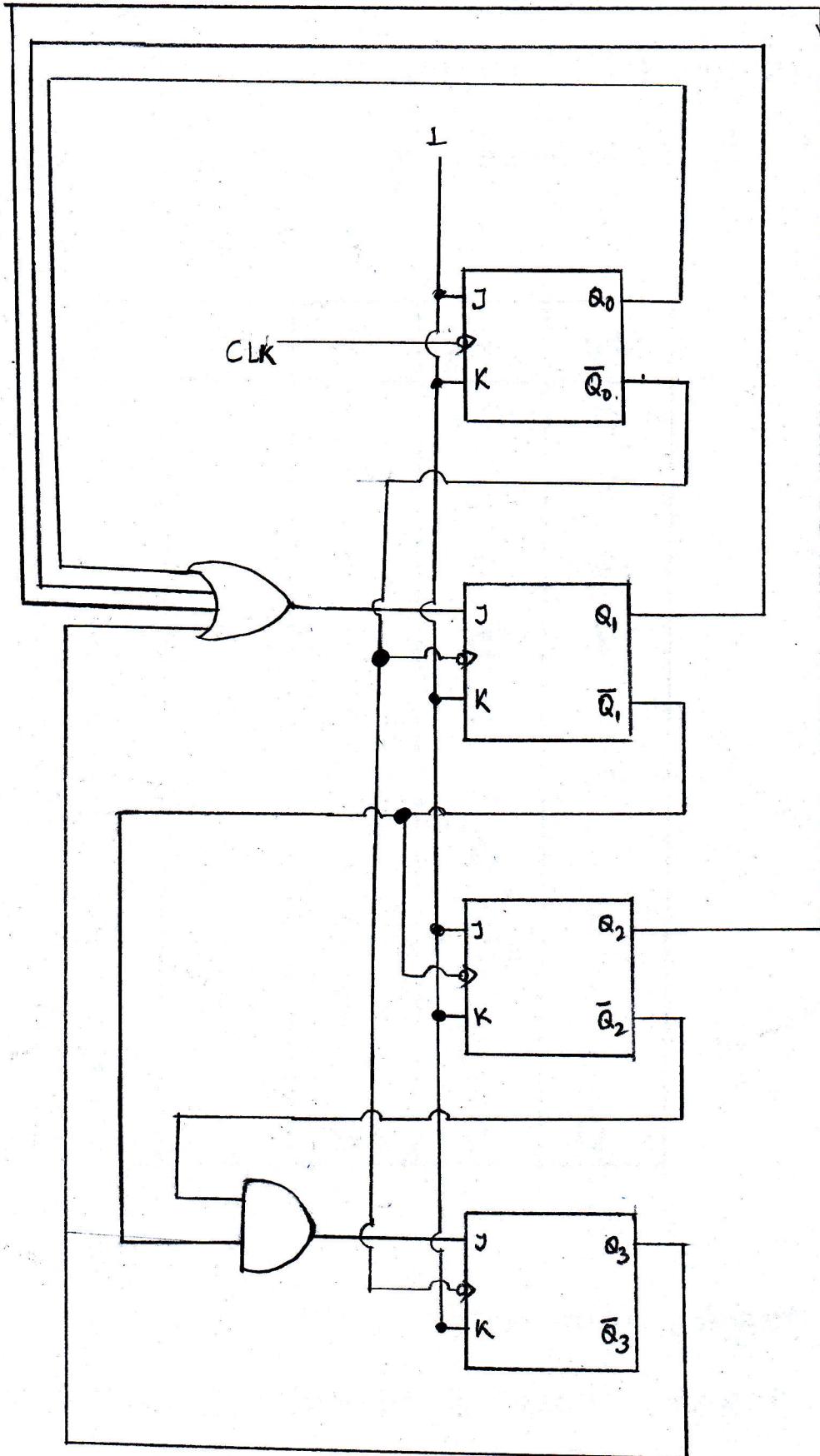
State	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

$Q_0$  toggles with each clock transition.

$Q_1$  toggles when  $Q_0$  transits  $0 \rightarrow 1$  ( $\bar{Q}_0$  transits  $1 \rightarrow 0$ )  
and atleast one of  $Q_0, Q_1, Q_2, Q_3$  is 1

$Q_2$  toggles when  $Q_1$  transits  $0 \rightarrow 1$  ( $\bar{Q}_1$  transits  $1 \rightarrow 0$ )

$Q_3$  toggles when  $Q_0$  transits  $0 \rightarrow 1$  ( $\bar{Q}_0$  transits  $1 \rightarrow 0$ )  
and both  $Q_2 = Q_1 = 0$  ( $\bar{Q}_2 = \bar{Q}_1 = 1$ )



All clocks are negative edge triggered