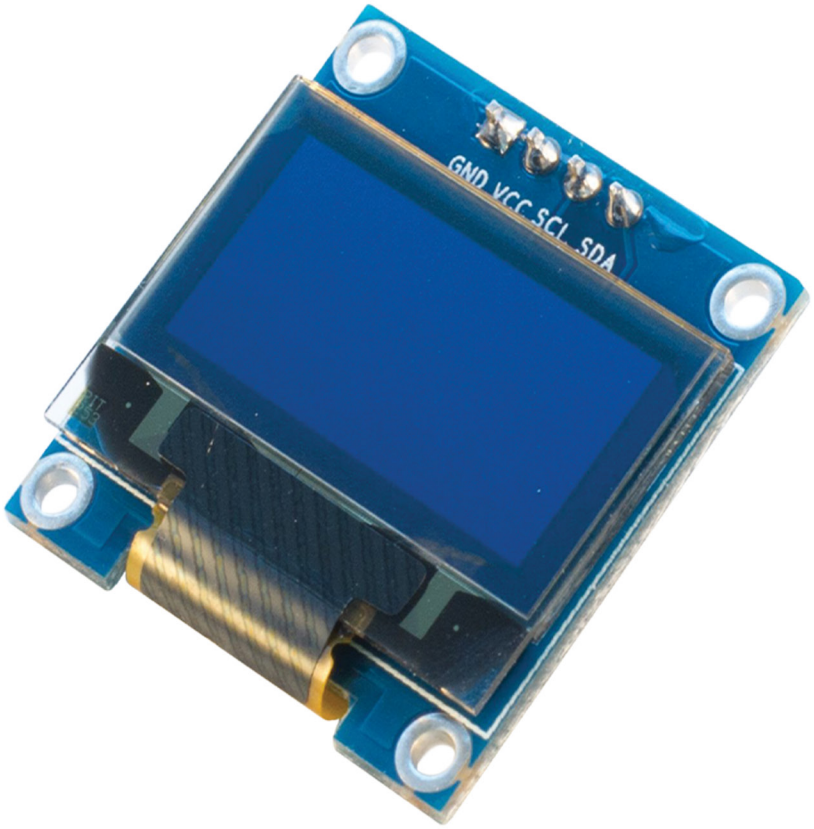
0,96 Zoll I2C OLED Display Datenblatt



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1. Scope

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. Features

(1) Small molecular organic light emitting diode.
(2) Color : White
(3) Panel matrix : 128*64
(4) Driver IC : SSD1306Z2
(5) Excellent quick response time.
(6) Extremely thin thickness for best mechanism design : 1.41mm
(7) High contrast : 2000:1
(8) Wide viewing angle : 160°
(9) 8-bit 6800/8080-series parallel interface, 4 wire Serial Peripheral Interface, I2C Interface
(10) Wide range of operating temperature : -40 to 70 °C
(11) Anti-glare polarizer.

3. Mechanical Data

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.154 (W) x 0.154 (H)	mm^2
3	Dot Pitch	0.17 (W) x 0.17 (H)	mm^2
4	Aperture Rate	78	%
5	Active Area	21.744 (W) x 10.864 (H)	mm^2
6	Panel Size	26.7 (W) x 19.26 (H)	mm^2
7*	Panel Thickness	1.22 ± 0.1	mm
8	Module Size	26.7 (W) x 31.26 (H) x 1.41 (D)	mm^3
9	Diagonal A/A size	0.96	inch
10	Module Weight	1.43 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4. Maximum Ratings

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	4	V	Ta = 25℃	IC maximum rating
Supply Voltage (V_{BAT})	-0.3	5	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	85	℃		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Life Time	27,000	-	Hrs	70 cd/m², 50% checkerboard	(Charge pump) Note (1)
Life Time	24,000	-	Hrs	80 cd/m², 50% checkerboard	(Charge pump) Note (2)
Life Time	19,000	-	Hrs	100 cd/m², 50% checkerboard	(External DC/DC) Note (3)
Life Time	16,000	-	Hrs	120 cd/m², 50% checkerboard	(External DC/DC) Note (4)
Life Time	13,000	-	Hrs	140 cd/m², 50% checkerboard	(External DC/DC) Note (5)

Note:

(A) Under Vcc = 7V (Charge Pump), Ta = 25°C, 50% RH.

Vcc = 12V (External DC/DC)

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 70 cd/m2 : (Charge Pump)

- Contrast setting : 0x42

- Frame rate : 105Hz

- Duty setting : 1/64

(2) Setting of 80 cd/m2 : (Charge Pump)

- Contrast setting : 0x66

- Frame rate : 105Hz

- Duty setting : 1/64

(3) Setting of 100 cd/m2 : (External DC/DC)

- Contrast setting : 0x22

- Frame rate : 105Hz

- Duty setting : 1/64

(4) Setting of 120 cd/m2 : (External DC/DC)
- Contrast setting : 0x34
- Frame rate : 105Hz
- Duty setting : 1/64

(5) Setting of 140 cd/m2 : (External DC/DC)
- Contrast setting : 0x44
- Frame rate : 105Hz
- Duty setting : 1/64

5. Electrical Characteristics

D.C Electrical Characteristics:

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Operating Voltage (Charge Pump)	-	7	-	7.5	V
V_{CC}	Operating Voltage (External DC/DC)	-	11.5	12	12.5	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.3	V
V_{BAT}	Charge Pump Regulator Supply Voltage	-	3.5	-	4.2	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8* V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2*V_{DD}	V
$I_{DD, SLEEP}$	I_{DD}, Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
$I_{CC, SLEEP}$	I_{CC}, Sleep mode Current	V_{DD} = 1.65V~3.3V, V_{CC} = 7V~15V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12, IREF =12.5uA, No Panel attached, Display ON, All ON	Contrast = FFh	-	430	780	uA
I_{DD}	V_{DD} Supply Current V_{DD} =2.8V, V_{CC} = 12, IREF =12.5uA , No Panel attached, Display ON, All ON,		-	50	150	uA
I_{SEG}	Segment Output Current, V_{DD} = 2.8V, V_{CC} =12V, IREF=12.5uA, Display ON.	Contrast=FFh	-	100	-	uA
		Contrast=AFh	-	69	-	
		Contrast=3Fh	-	25	-	

Electro-Optical Characteristics
Panel Electrical Specifications

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current (IBAT) (Charge Pump)	-	20	22	mA	All pixels on (1)
Normal mode current (ICC) (External DC/DC)	-	9	11	mA	All pixels on (3)
Standby mode current(IBAT) (Charge Pump)	-	3	4	mA	Standby mode 10% pixels on (2)
Standby mode current(ICC) (External DC/DC)	-	2	3	mA	Standby mode 10% pixels on (4)
Normal Luminance (Charge Pump)	70	80	-	cd/m^2	Display Average
Normal Luminance (External DC/DC)	100	120	-	cd/m^2	Display Average
Standby Luminance (Charge Pump)	-	45	-	cd/m^2	Display Average
Standby Luminance (External DC/DC)	-	60	-	cd/m^2	Display Average
CIEx (White)	0.28	0.32	0.36		x, y (CIE 1931)
CIEy (White)	0.31	0.35	0.39		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition : (Charge Pump)
- Contrast setting : 0x66
- Frame rate : 105Hz
- Duty setting : 1/64

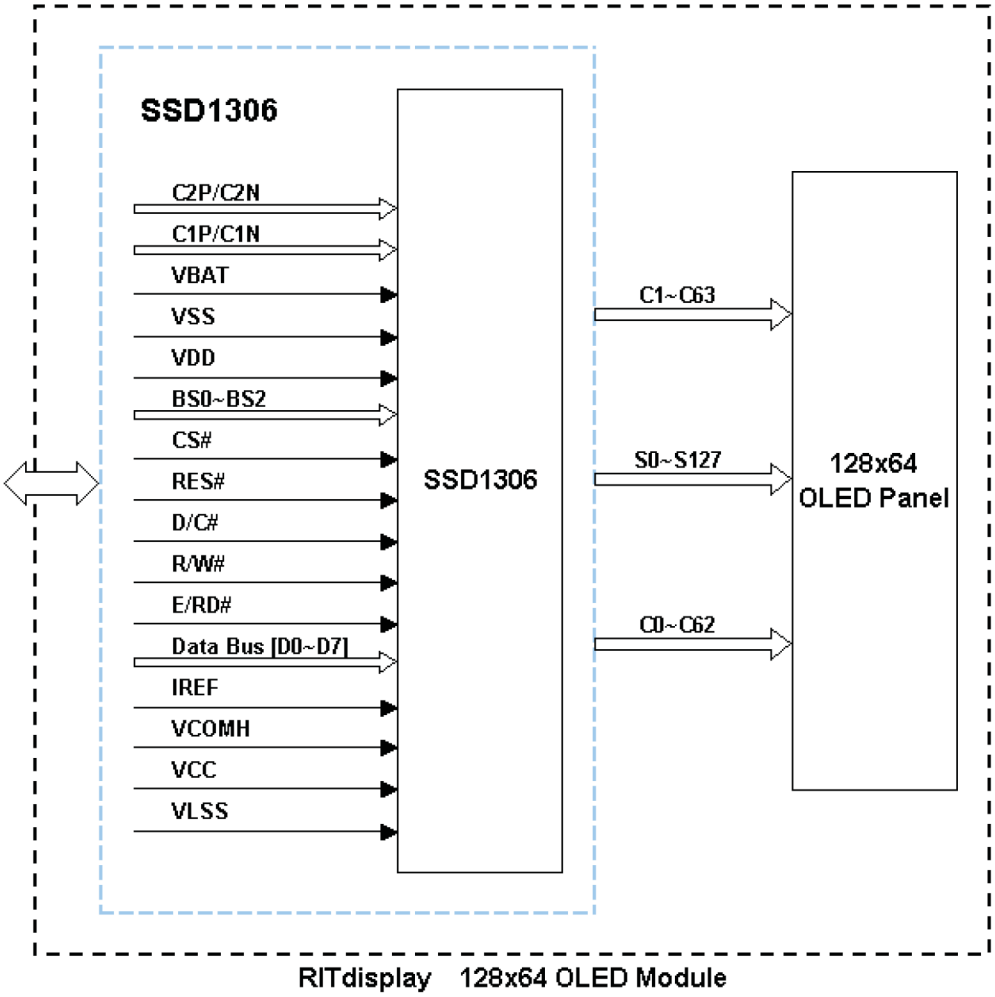
(2) Standby mode condition : (Charge Pump)
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Normal mode condition : (External DC/DC)
- Driving Voltage : 12V - Contrast setting : 0x34
- Frame rate : 105Hz
- Duty setting : 1/64

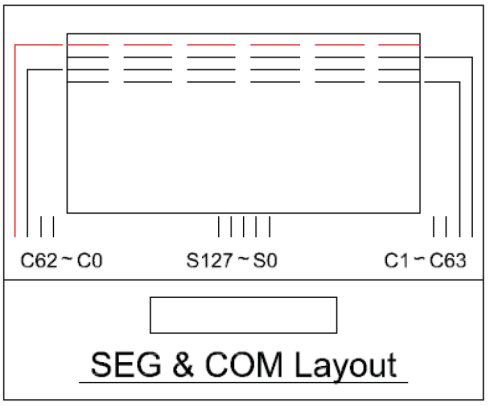
(4) Standby mode condition : (External DC/DC)
- Driving Voltage : 12V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/6 4

6. Interface

Function Block Diagram:



Panel Layout Diagram:

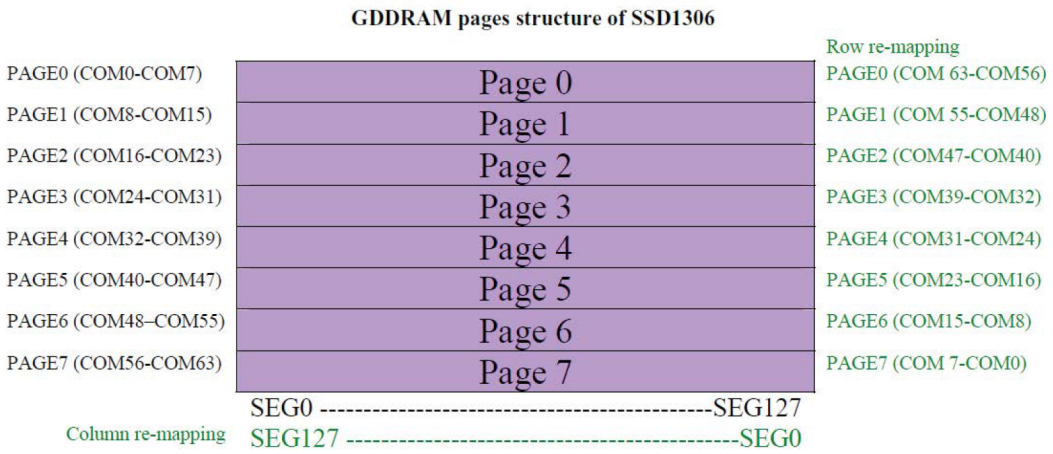


Pin Assignments:

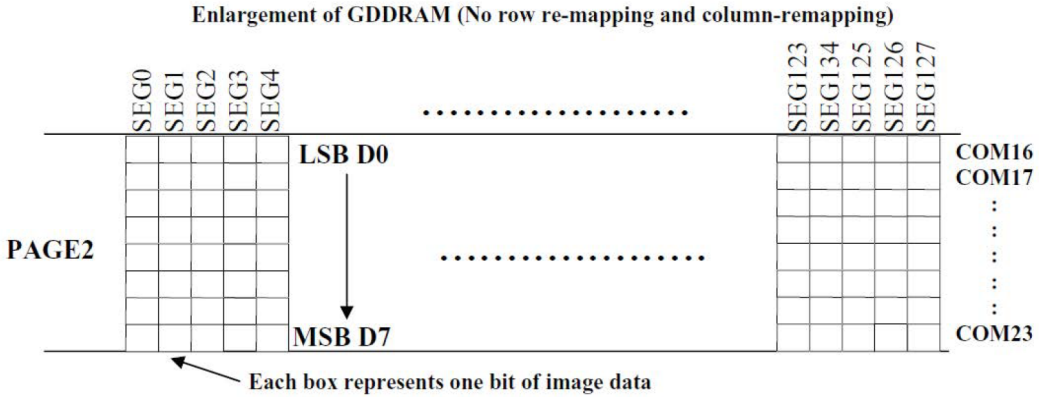
Pin No.	Pin Name	Description
1	NC(GND)	Reserved pin. It should be connected to VSS.
2	C2P	C2P/C2N – Pin for charge pump capacitor; Connect to each other with a capacitor.
3	C2N	
4	C1P	C1P/C1N – Pin for charge pump capacitor; Connect to each other with a capacitor.
5	C1N	
6	VBAT	Power supply for charge pump regulator circuit.
7	NC	No connection.
8	VSS	Ground pin.
9	VDD	Power supply pin for core logic operation.
10	BS0	MCU bus interface selection pins.
11	BS1	
12	BS2	
13	CS#	This pin is the chip select input connecting to the MCU.
14	RES#	This pin is reset signal input.
15	D/C#	This pin is Data/Command control pin connecting to the MCU.
16	R/W#	This pin is read / write control input pin connecting to the MCU interface. 8080: data write enable pin; 6800:Read/Write select pin. When serial or I^2C interface is selected, this pin must be connected to VSS.
17	E/RD#	8080: data read enable pin; 6800:Read/Write enable pin. When serial or I^2C interface is selected, this pin must be connected to VSS.
18	D0	These pins are bi-directional data bus connecting to the MCU data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I^2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
19	D1	
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	
26	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.
27	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
28	VCC	Power supply for panel driving voltage.
29	VLSS	Ground pin.
30	NC(GND)	Reserved pin. It should be connected to VSS.

Graphic Display Data Ram (GDD RAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.



When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

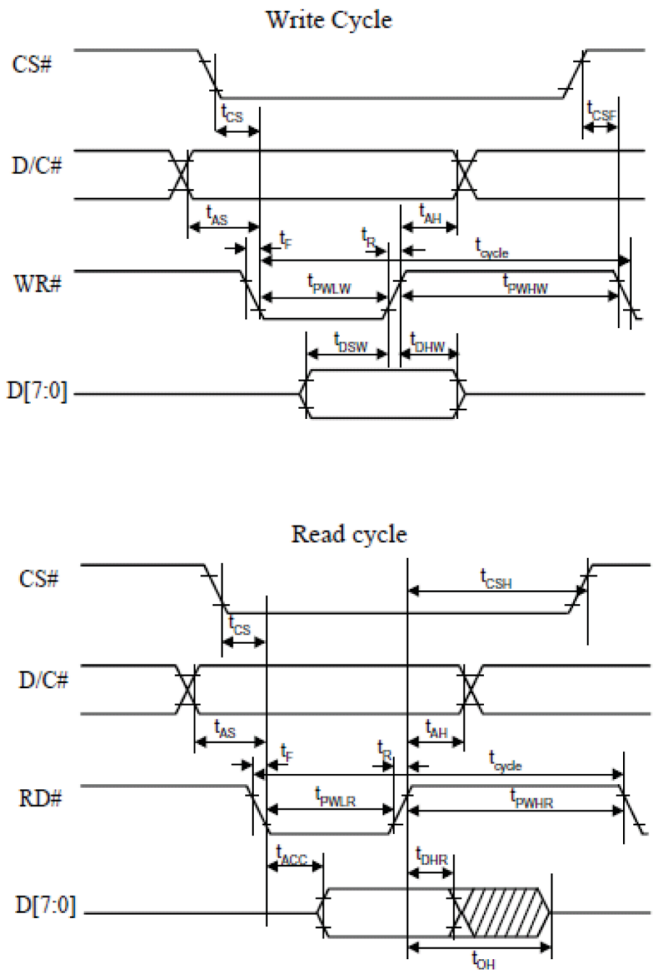
Interface Timing Chart

8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics



7. Power ON/OFF Sequence and Aplication Circuit

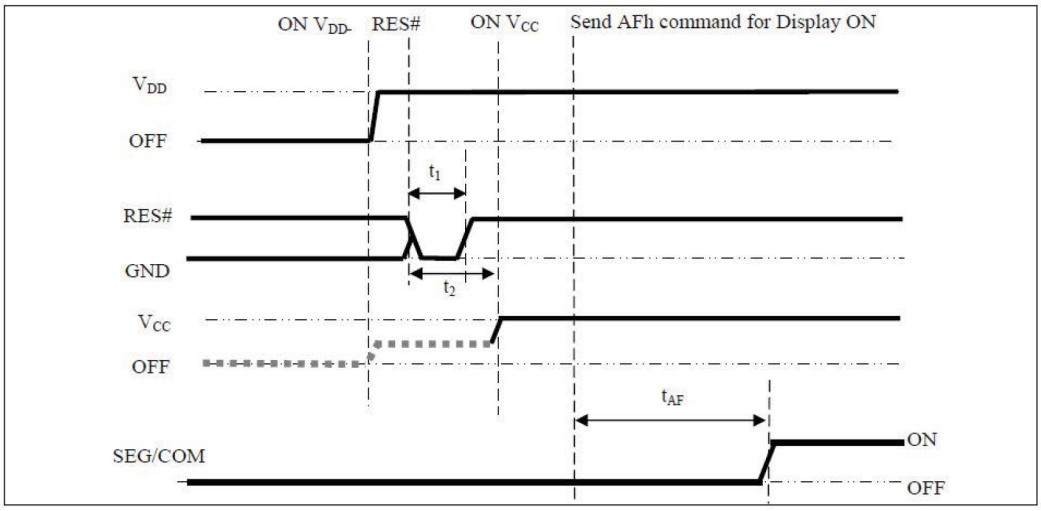
Power ON and OFF Sequence with external DC/DC Application:

The following figures illustrate the recommended power ON and power OFF sequence of SSD1306 with external DC/DC application.

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

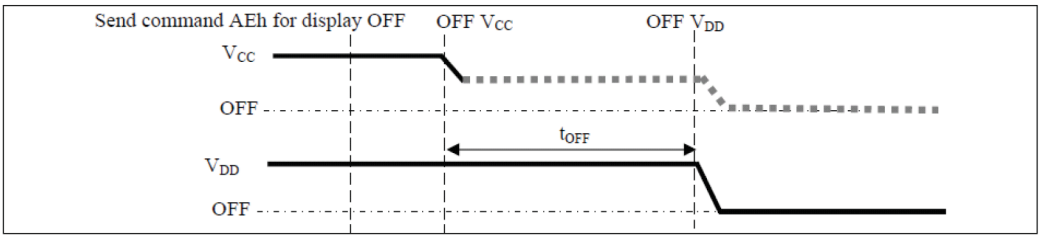
The Power ON Sequence



Power OFF sequence :

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. [1], [2], [3]
3. Power OFF V_{DD} after t_{OFF}. [5] (where Minimum t_{OFF}=80ms,Typical t_{OFF}=100ms)

The Power OFF Sequence



Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures. (2) V_{CC} should be disabled when it is OFF

(3) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

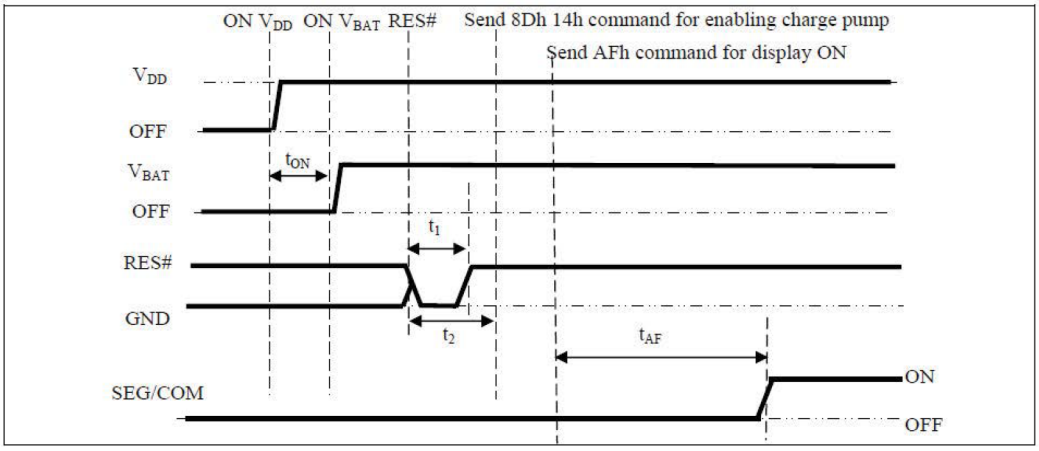
(5) V_{DD} should not be Power OFF before V_{CC} Power OFF.

Power ON and OFF Sequence with Charge Pump Application:
The following figures illustrate the recommended power ON and power OFF sequence of SSD1306 with charge pump application.

***Power ON sequence*:**

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}.[(1), (2)] (where Minimum t_{ON}=0ms)
3. After V_{BAT} become stable, set RES# pin LOW (logic low) for at least 3us (t1) [(3)] and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t2). Then input commands with below sequence:
   a. 8Dh 14h for enabling charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

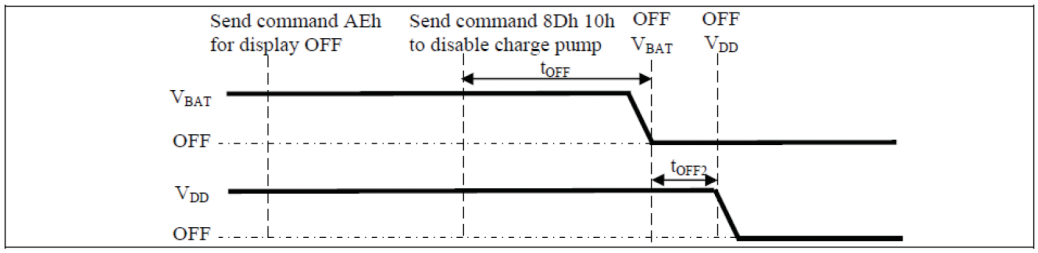
The Power ON Sequence With Charge Pump Application



***Power OFF sequence*:**

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}. [(1), (2)] (Typical t_{OFF}=100ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2}=0ms [(4)], Typical t_{OFF2}=5ms)

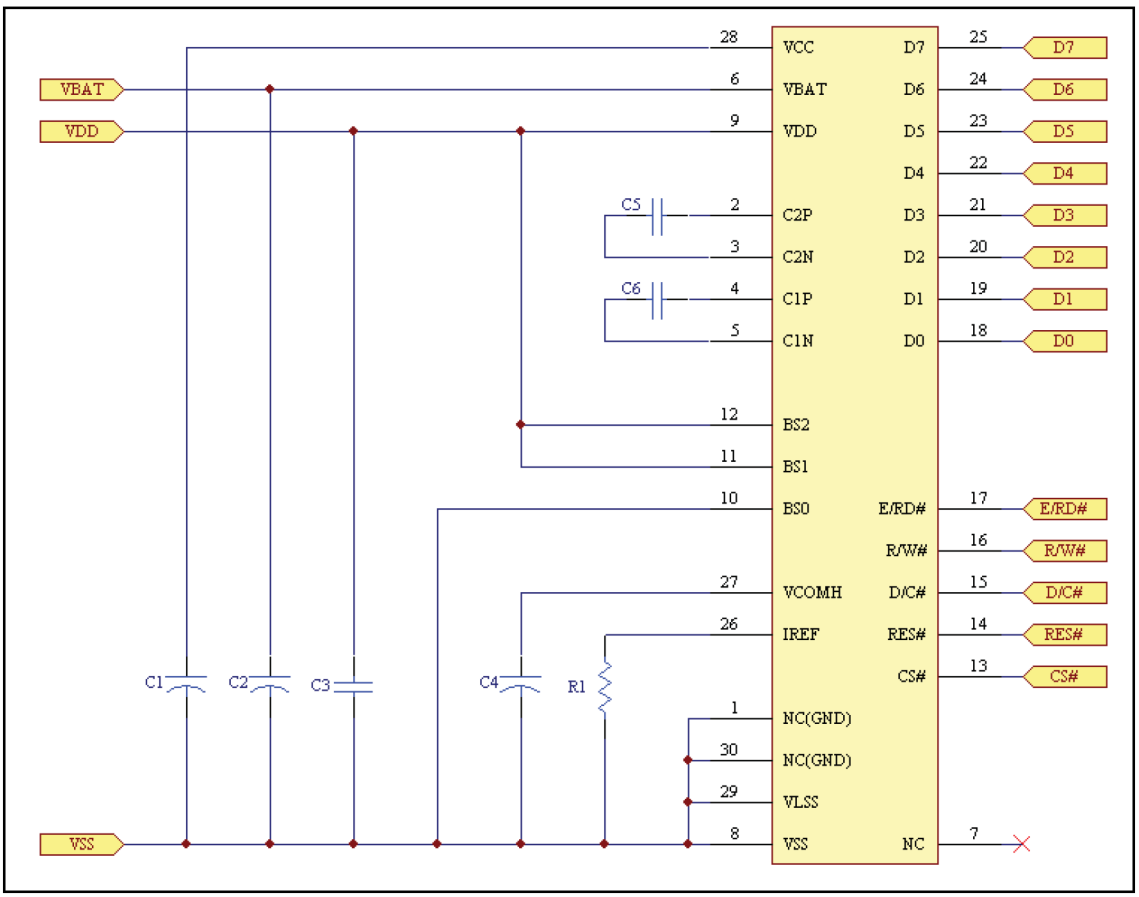
The Power OFF Sequence With Charge Pump Application



Note:

(1) V_{BAT} should be disabled when it is OFF.
(2) Power Pins (V_{DD} , V_{BAT}) can never be pulled to ground under any circumstance. (3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{BAT} Power OFF.

Application Circuit (Charge Pump) :



Recommended components:

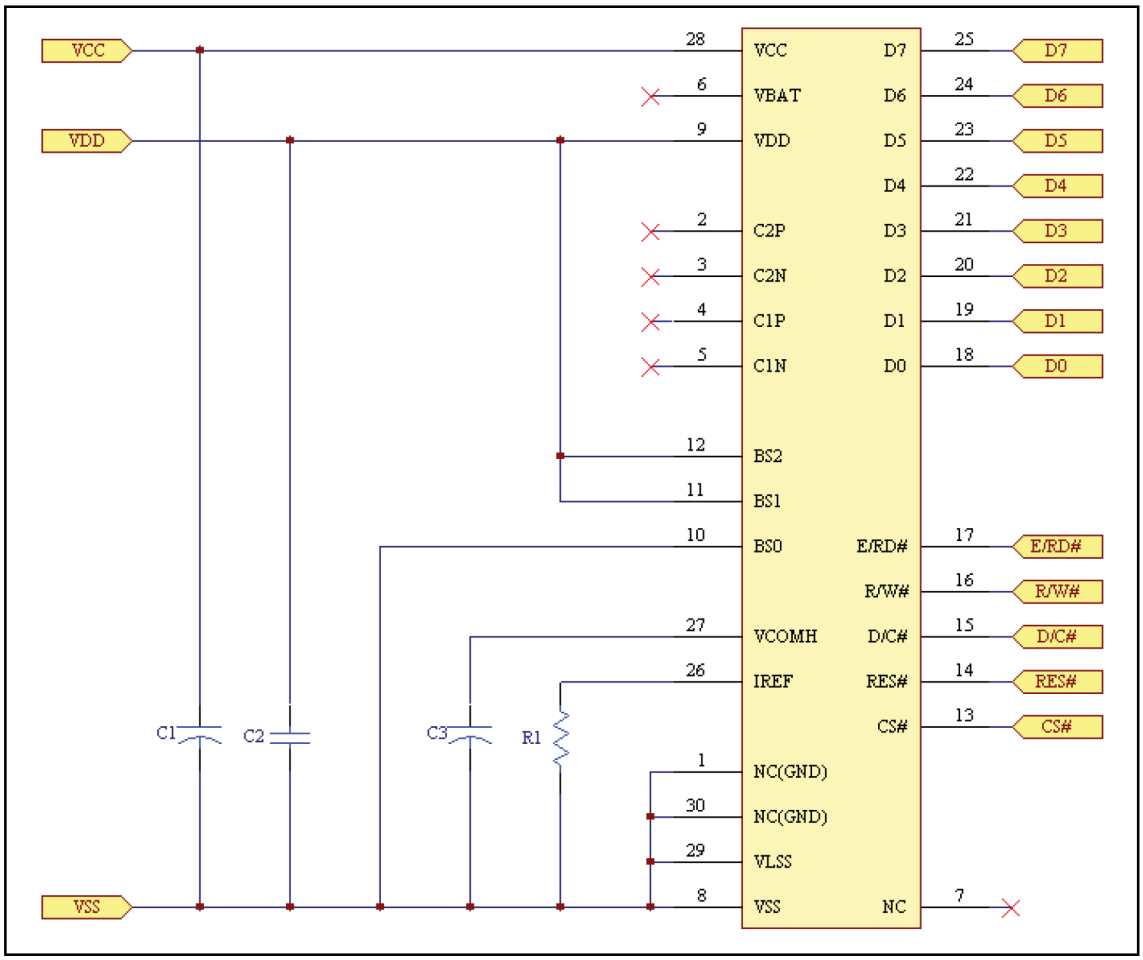
C1: 2.2uF/25V(0805)

C2,C3,C5,C6: 1uF/16V (0603)

C4: 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T) R1: 620K ohm (0603) 1%

This circuit is designed for 8080 8-bit interface.

(External DC/DC):



Recommended components:
C1: 2.2uF/25V(0805)
C2: 1uF/16V (0603)
C3: 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)
R1: 620K ohm (0603) 1%
This circuit is designed for 8080 8-bit interface.

Command Table:

Refer to SSD1306Z2 IC Spec.

8. Reliability Test Conditions

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

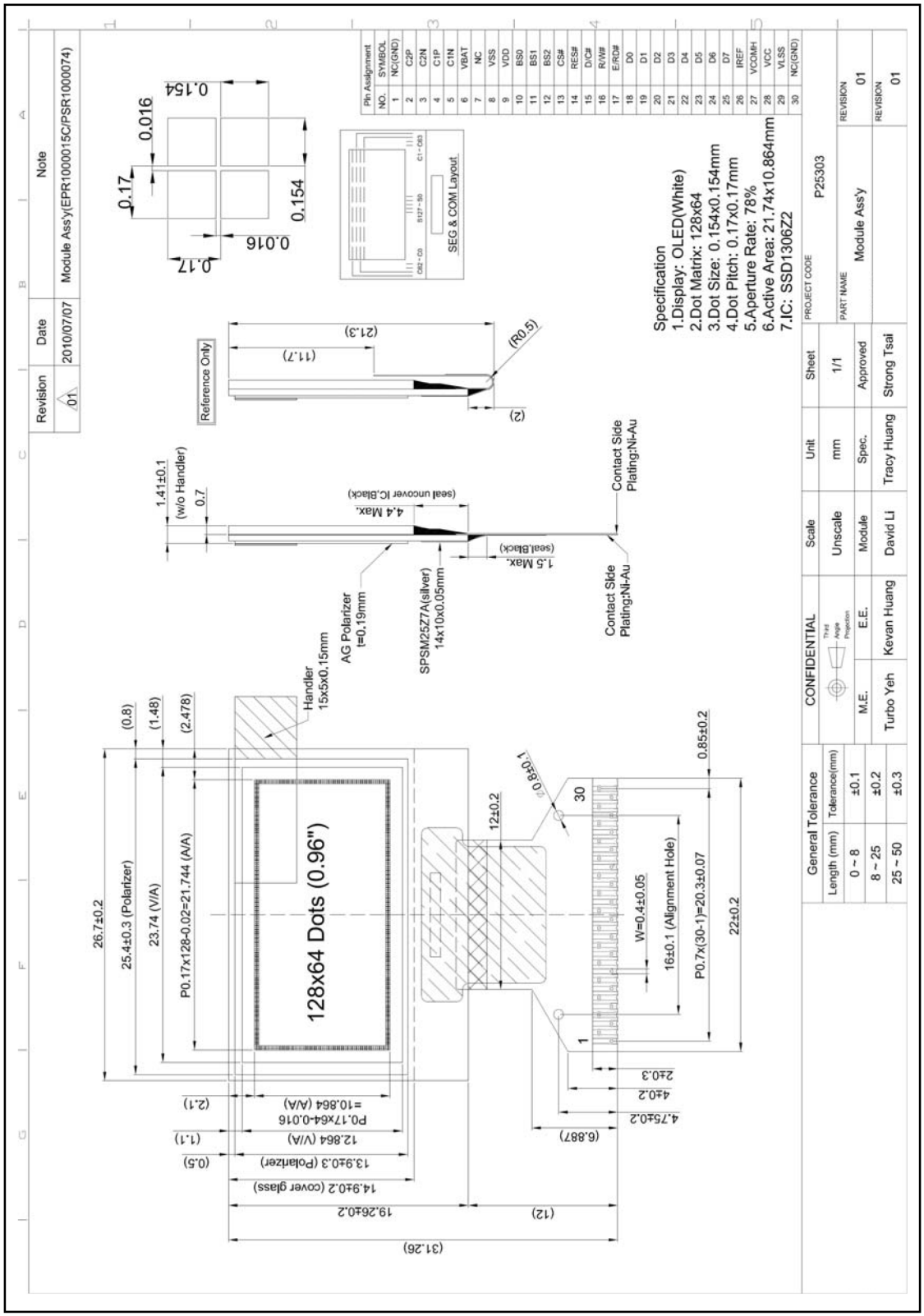
Test and measurement conditions:

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

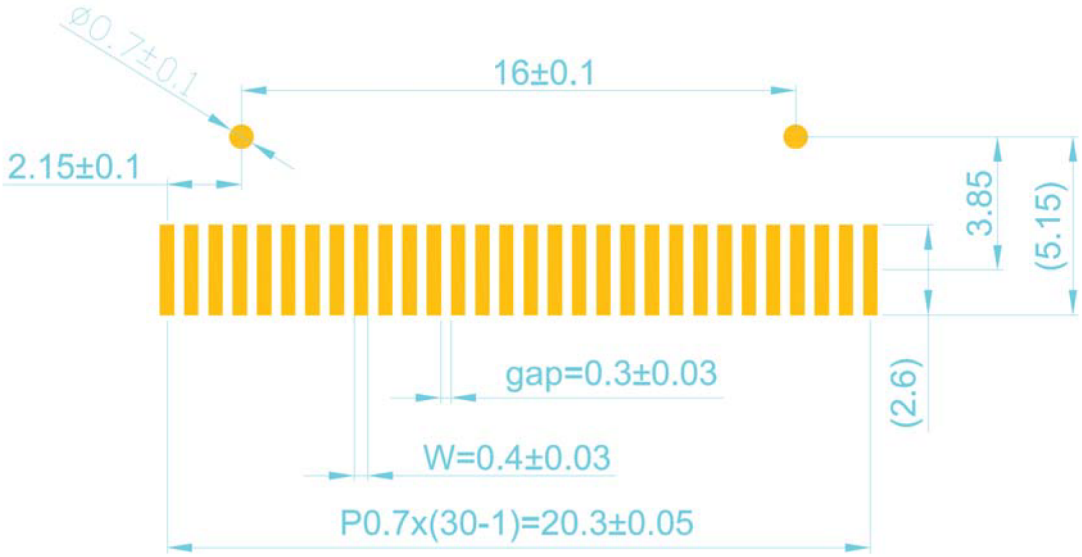
Evaluation criteria:

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ⊠50% of initial value.

9. External Dimension



Suggested PCB mounting dimensions



10. Appendixes

Appendix 1: Definitions

a) Definition Of Chromaticity Coordinate

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

b) Definition Of Contrast Ratio

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

c) Definition Of Response Time

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance.
The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance.
It is shown in Figure 2.

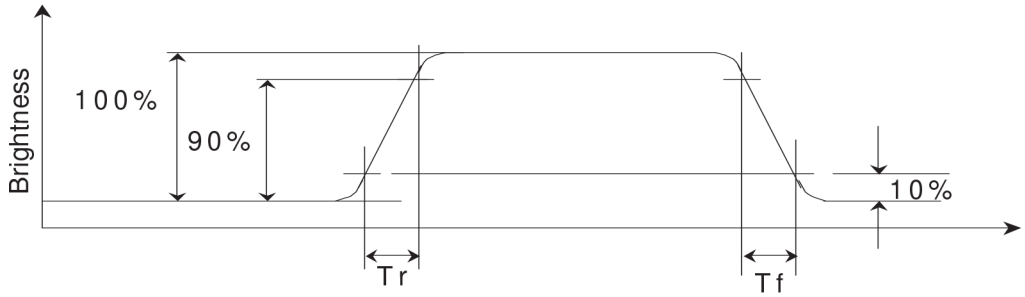
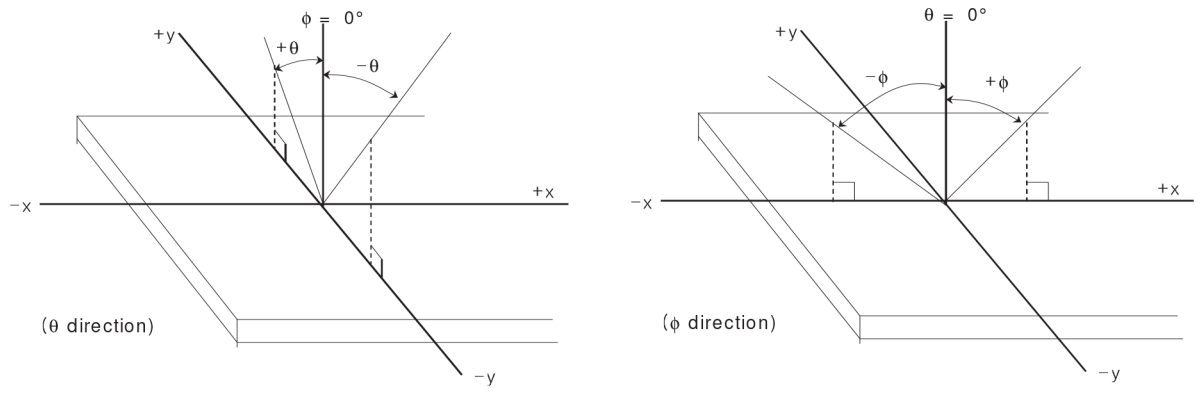


Figure 2: Response time

d) Definition Of Viewing Angle:

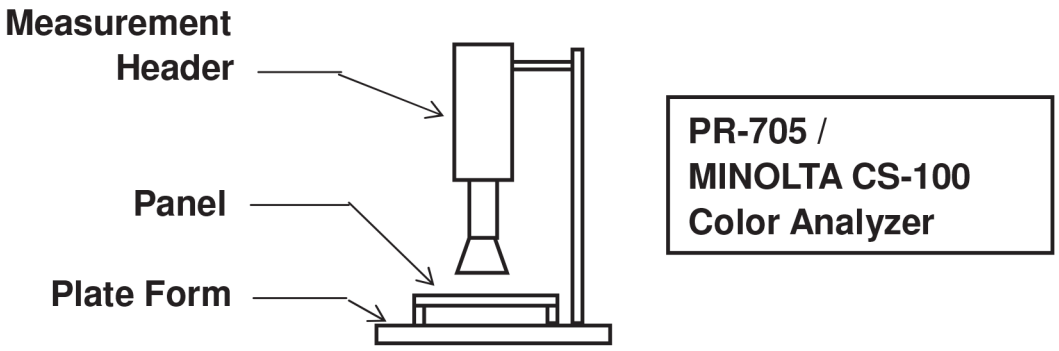
The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

Figure 3: Viewing Angle



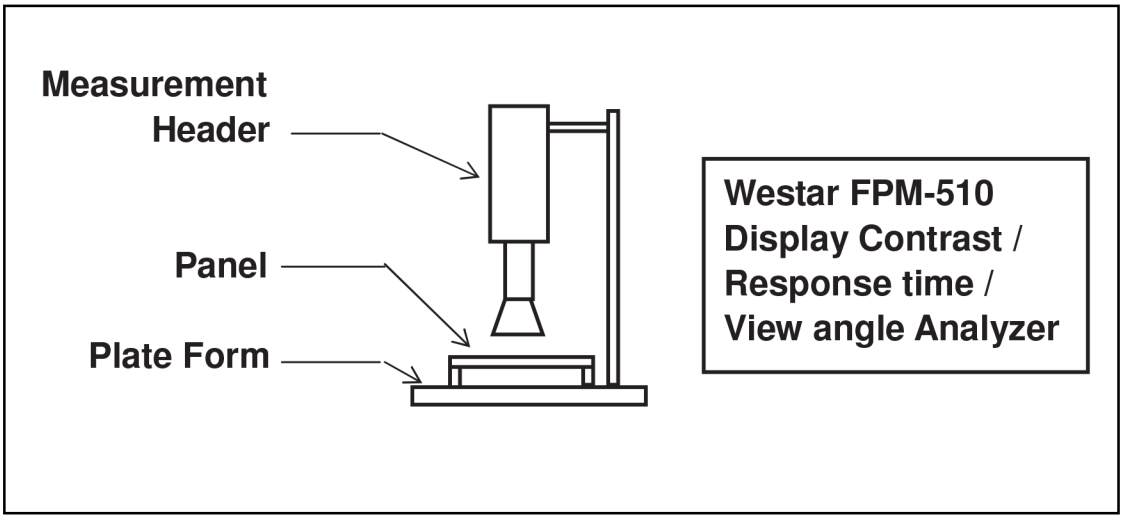
Appendix 2: Measurement Apparatus:

a) Luminance/Color Coordinate
Photo Research PR-705, MINOLTA CS-100

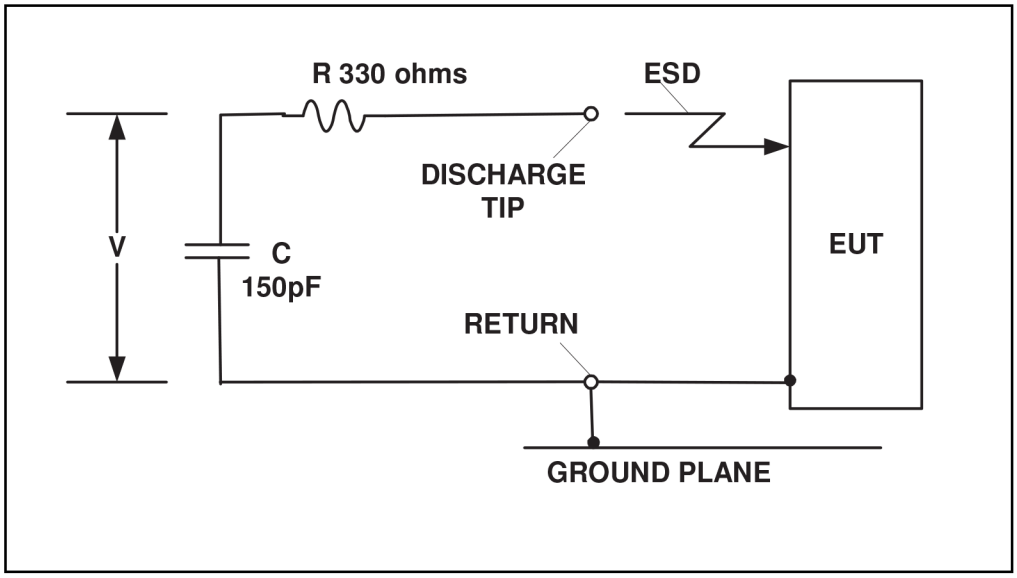


b) Contrast / Response Time / View Angle

Westar Corporation FPM-510



c) ESD on Air Discharge Mode



Appendix 3:
Precautions:

a) Residue Image

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.