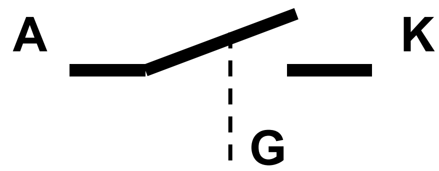
第7章 软开关谐振功率变换技术

- 什么是 软开关技术（soft switching）？
- 为什么要使用 soft switching？
- 如何实现 soft switching？

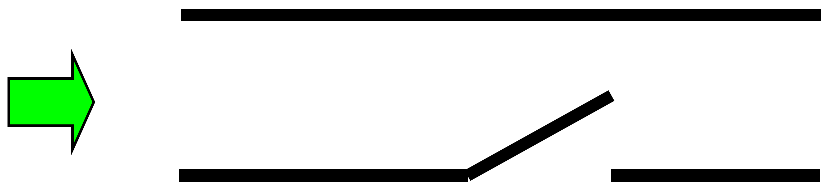
课程教材：徐德鸿、马皓、汪槱生主编 电力电子技术

软开关的概念 Concept of soft switching

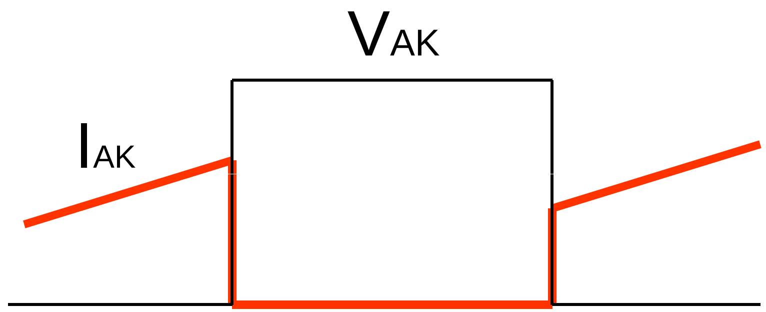
(1) 理想开关（Ideal switch）

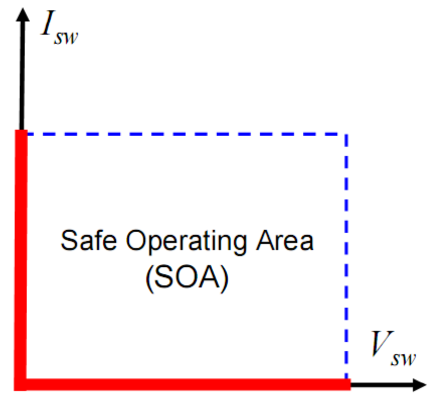


- Static characteristics
  - ON state R=0
  - Off state R=infinite



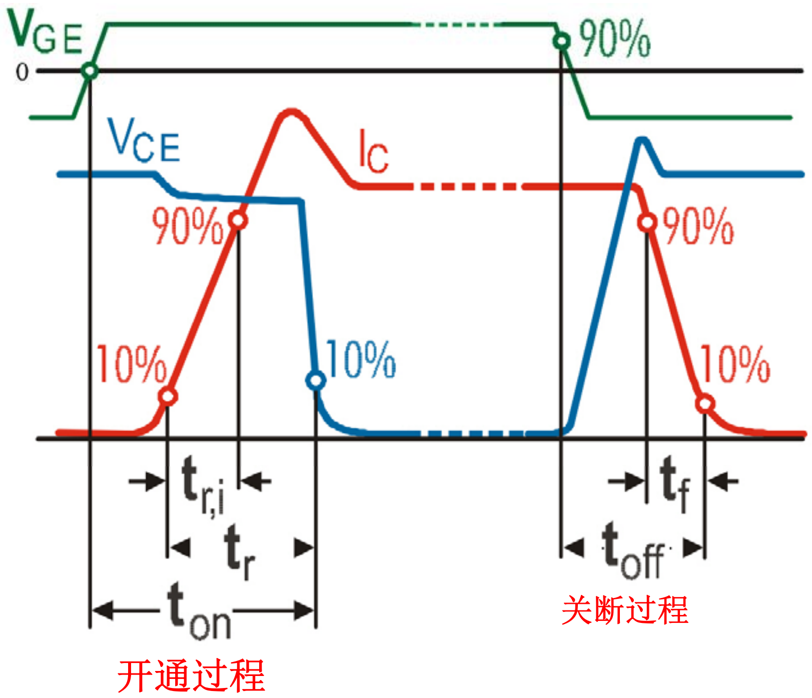
- Dynamic characteristics
  - Turn on time=0
  - Turn off time=0

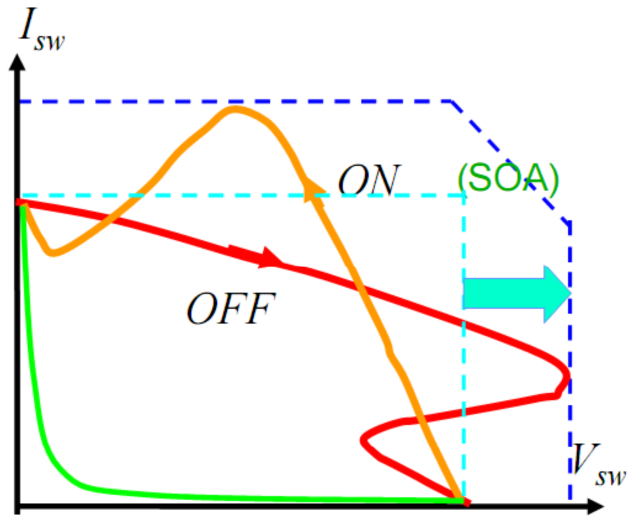




（2）实际的功率器件的开关过程

◆ 特性：拖拉、动作不干脆

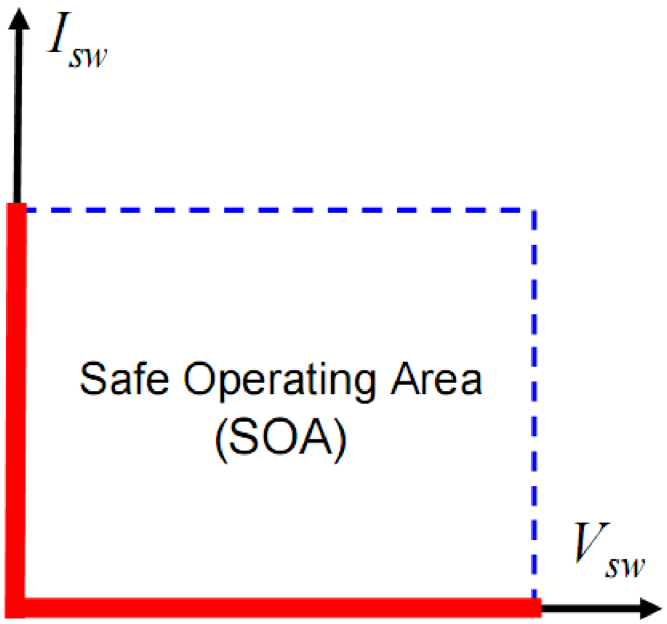




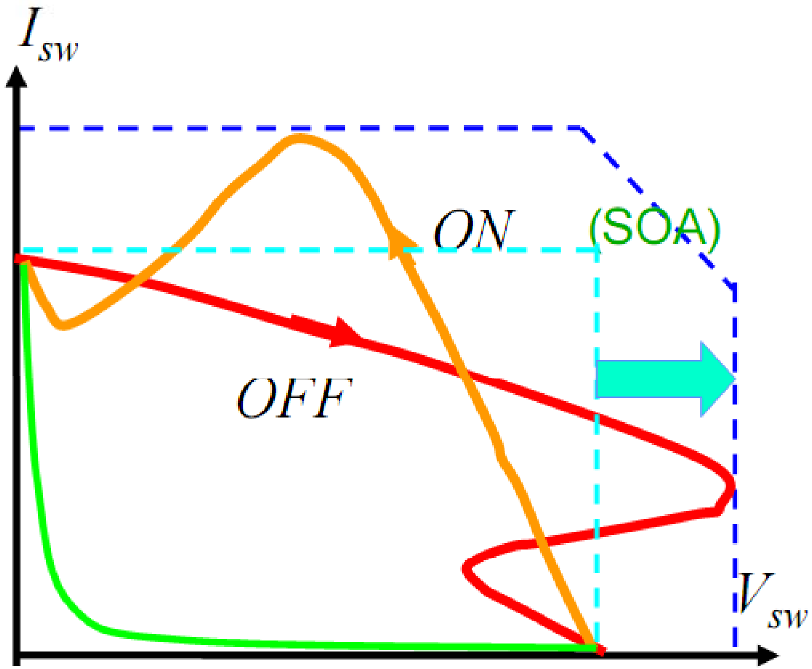
此外,存在通态压降

比较

Ideal Switching



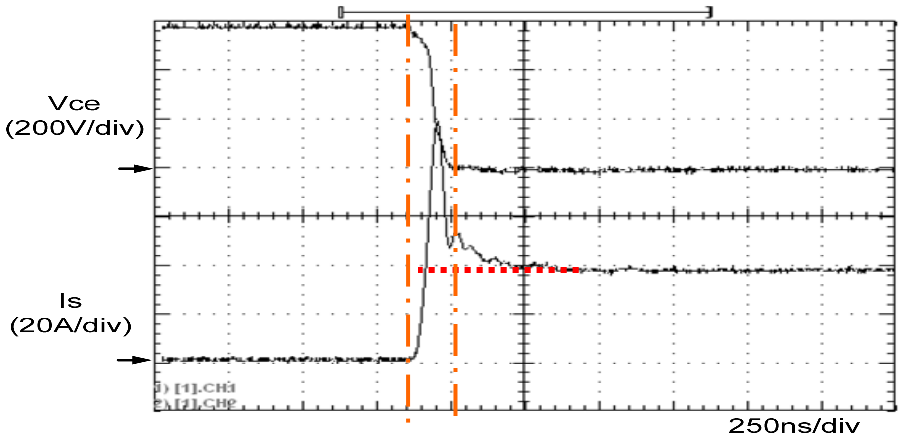
Actual Switching



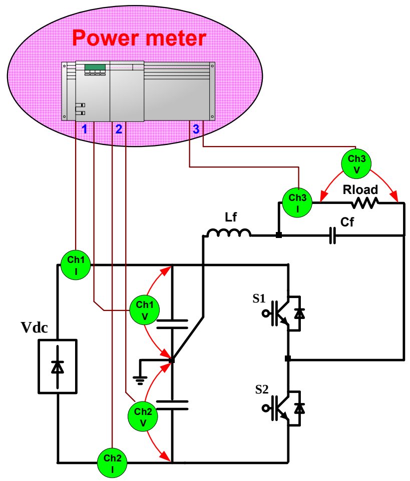
IGBT开关过程

器件: U-Series IGBT+Si FWD (2MBI150U4B)
IGBT: 150A/1200V   Si diode: 150A/1200V

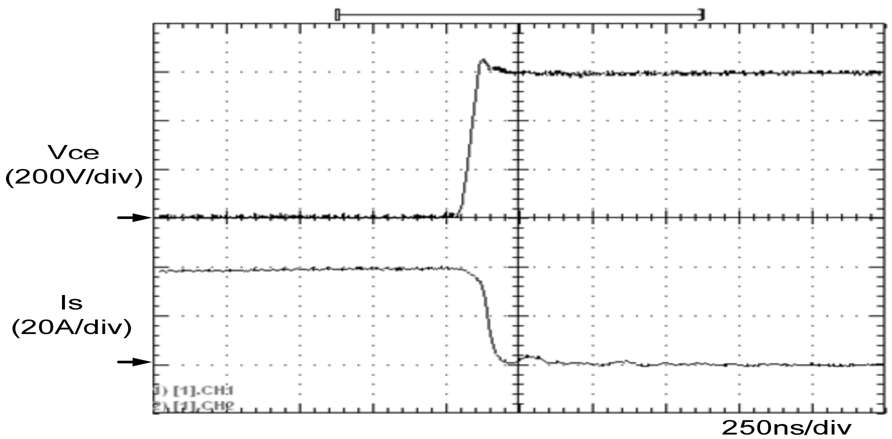
@Vce=600V Ic=40A Rg=2.2Ω



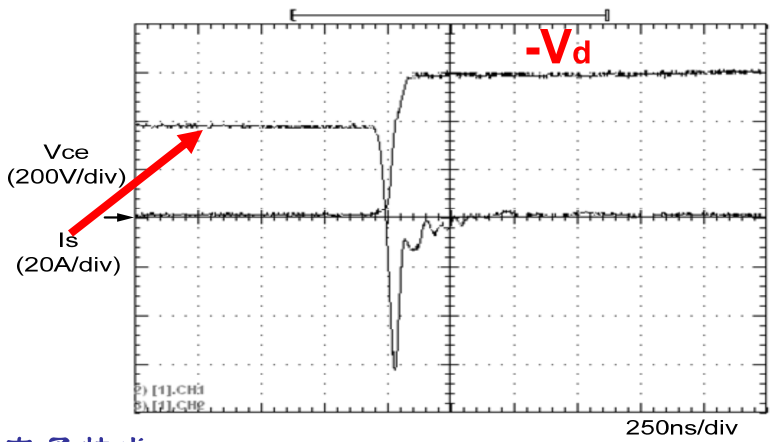
Switch-on



$$P_{sw} = f \cdot \sum_{n=1}^{N} \left[E_{off}\left(i_o(n)\right) + E_{on}\left(i_o(n)\right) + E_{rr}\left(i_o(n)\right) \right]$$

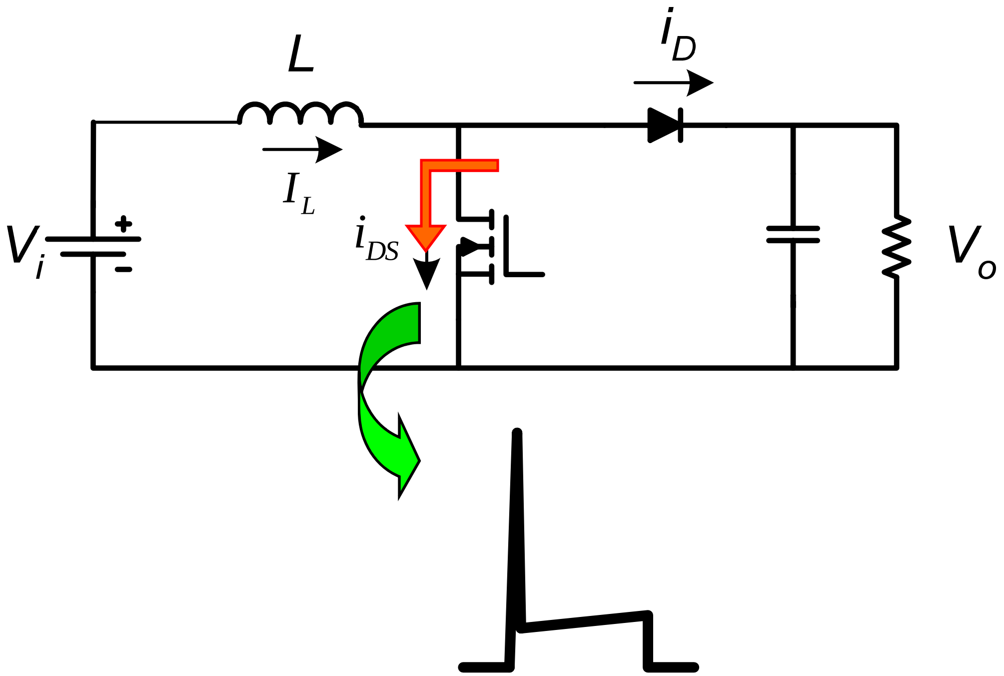


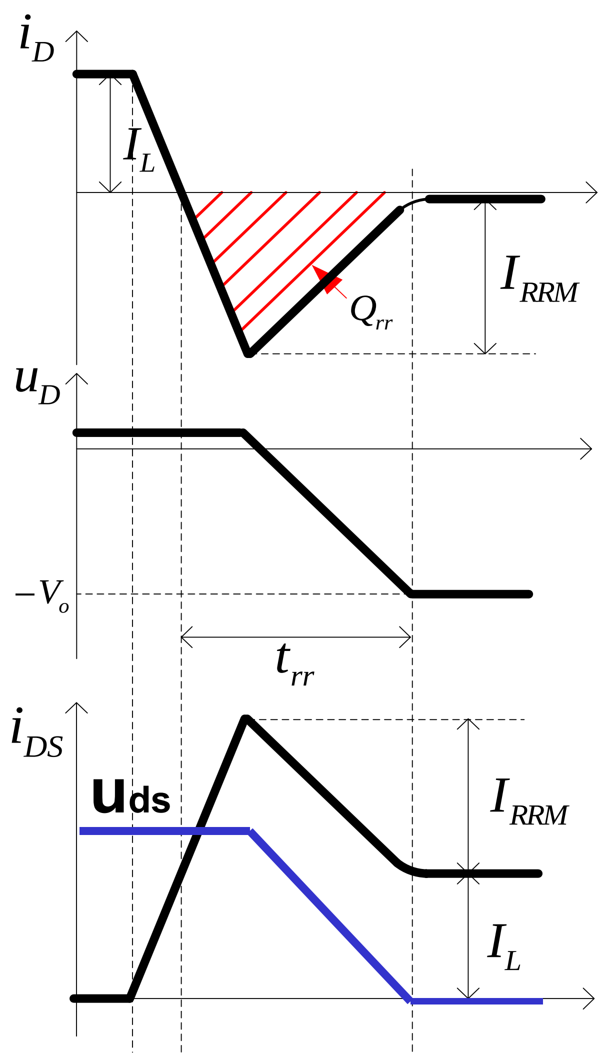
Switch-off



Reverse recovery

二极管反向恢复过程（Diode reverse recovery）

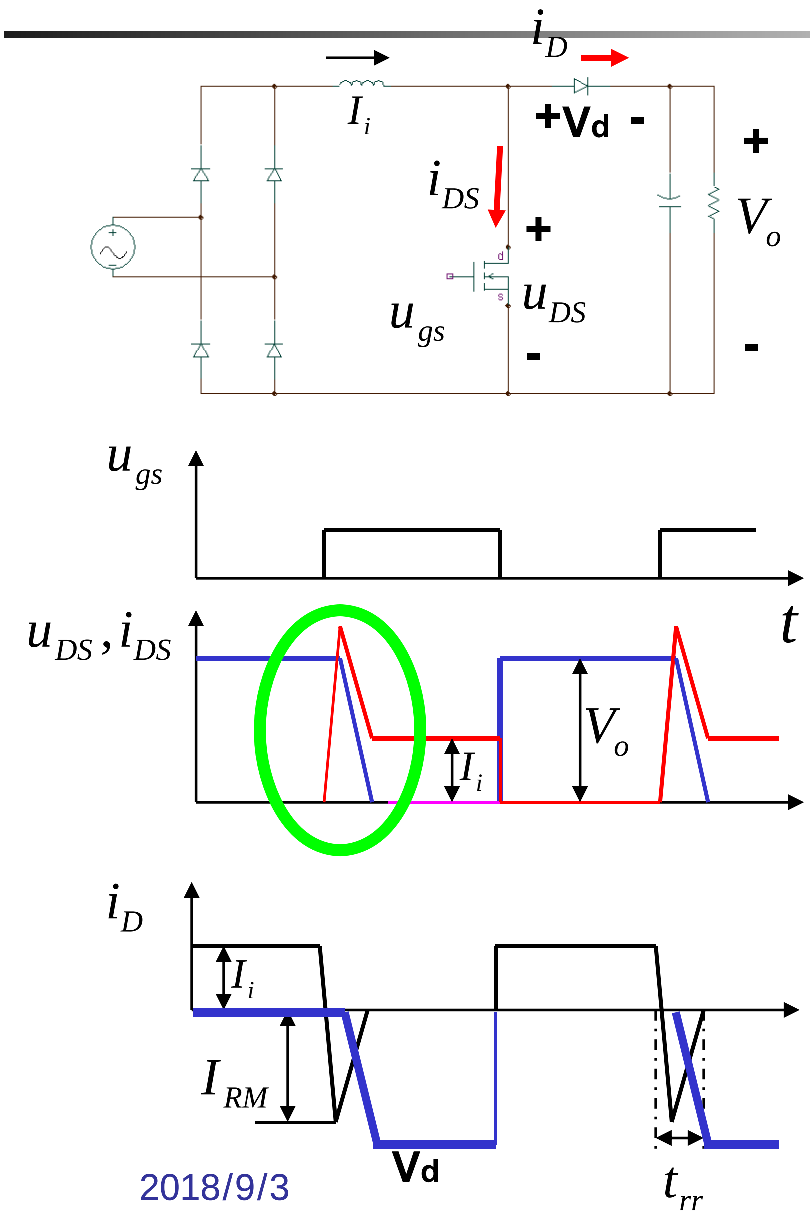


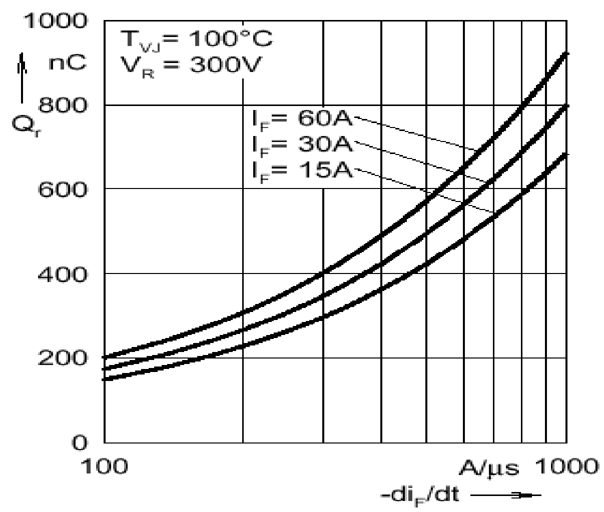


- High di/dt, EMI problem
- High loss on switch and diode

In the future SiC Schottky diode

反向恢复过程引起的损耗
（Switching loss resulting from reverse recovery）





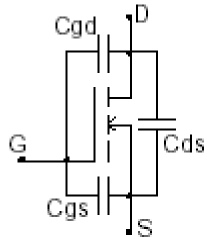
Reverse recovery charge Q_{rr} **vs.** $\frac{dI_F}{dt}$

- **Turn-on loss in switch and boost diode**

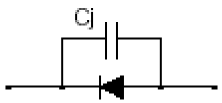
$$A_{turn\_on} = Q_{rr}V_o + I_i \int_0^{t_{rr}} u_{DS}\,dt + \frac{1}{2}C_{oss}V_o^2$$

寄生电容（Parasitic capacitance)

Power MOSFET

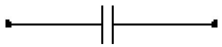


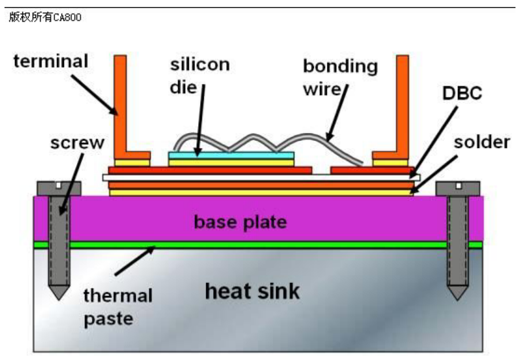
Diode



Layout stray capacitance

Transformer winding capacitance





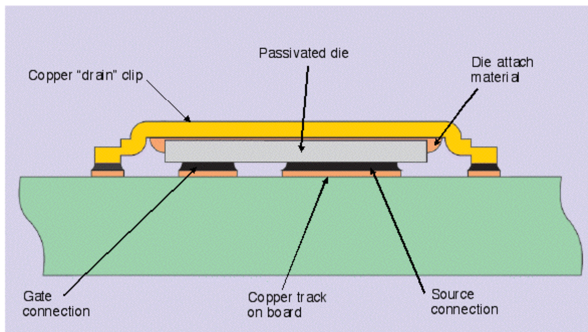
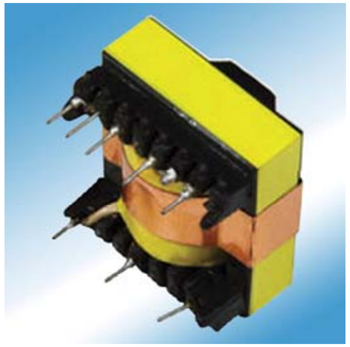
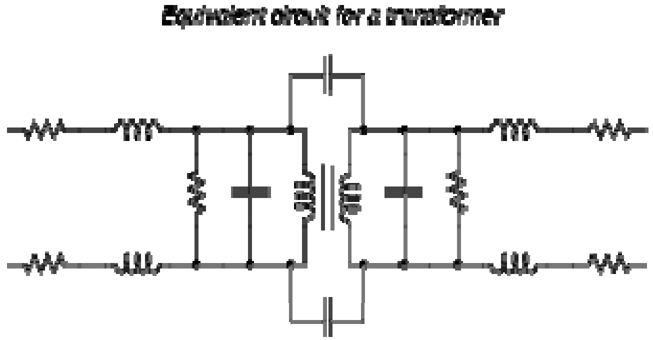


Fig 1 Cross-Section of a DirectFET MOSFET Soldered to PCB

寄生电感（Parasitic inductance)

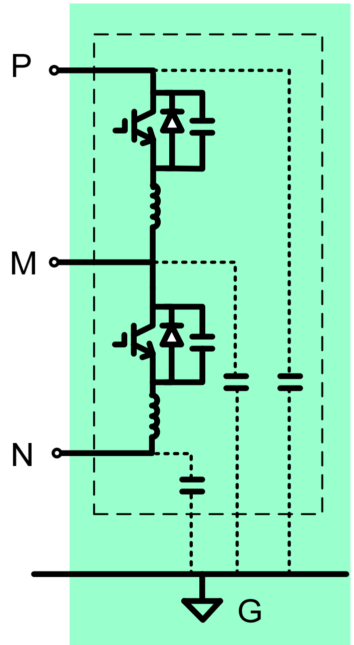
Leakage inductance of the transformer



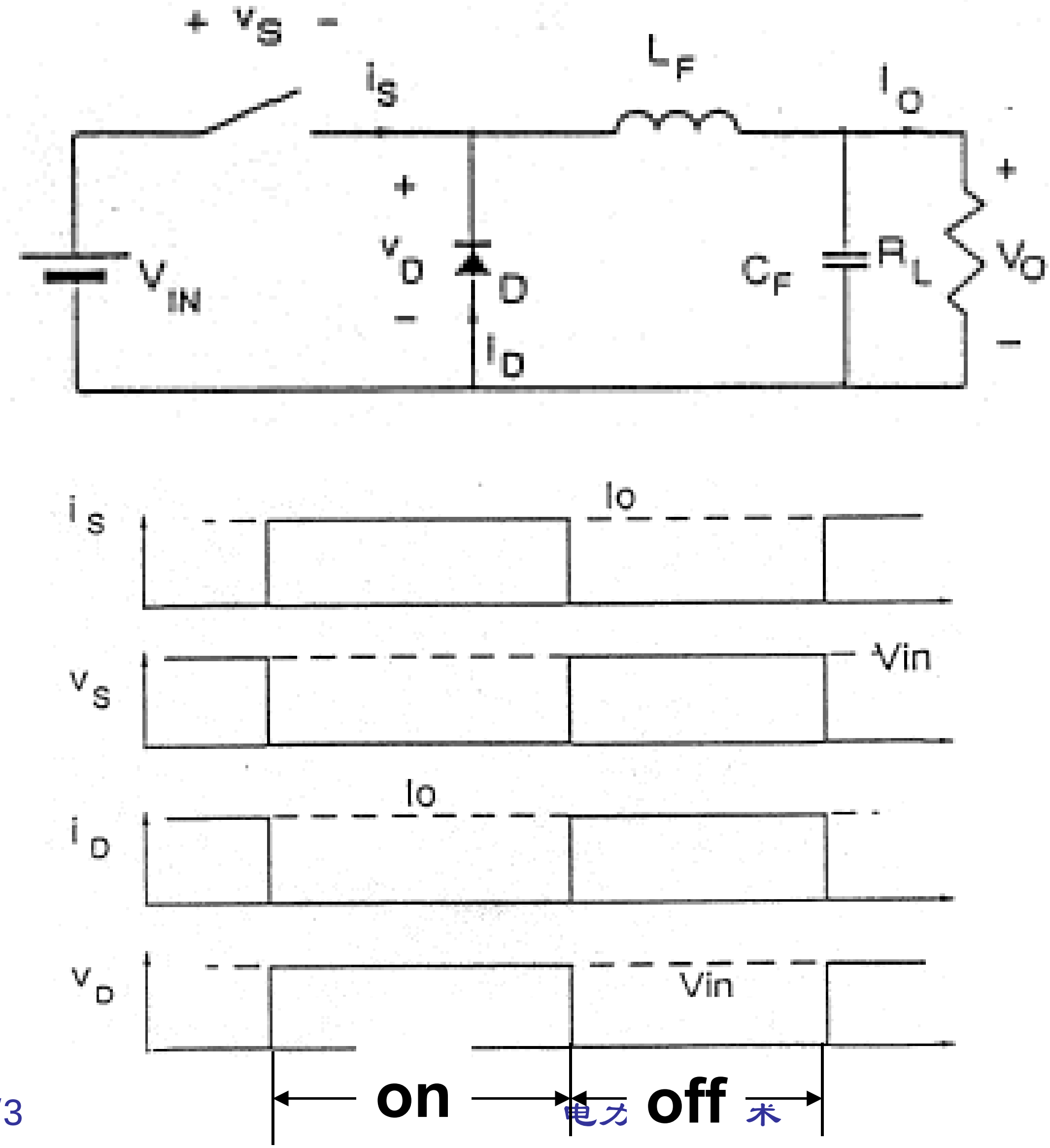


Stray inductance

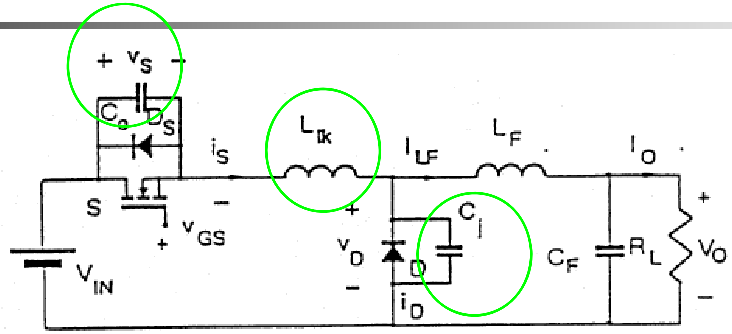
- Layout
- Wire bonds in device packages
- Leads of devices



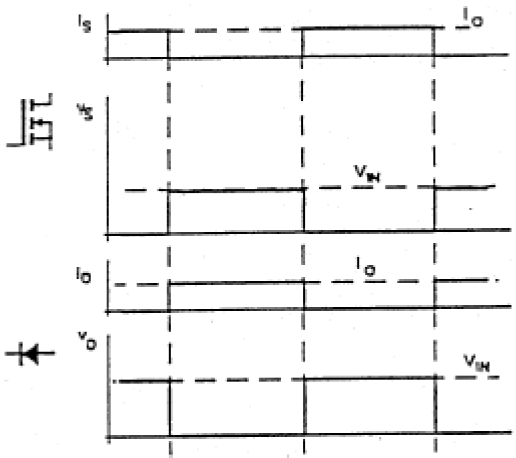
理想元件构成的Buck变换器（Ideal Buck converter）



实际元件构成的Buck变换器（Practical Buck converter）



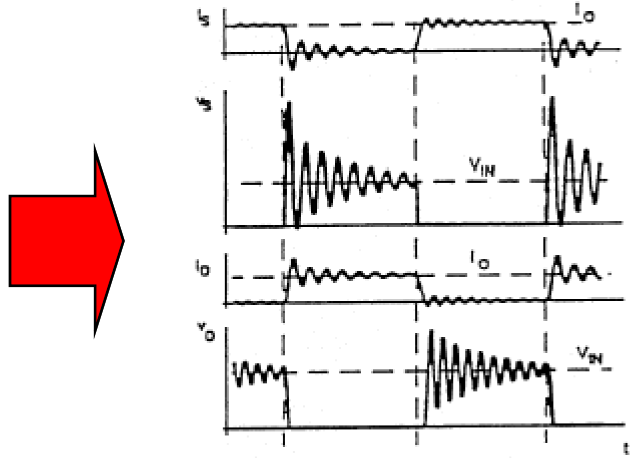
Ideal



Square Waveforms

No Switching Loss

Practice



Parasitic Oscillations

Switching Loss

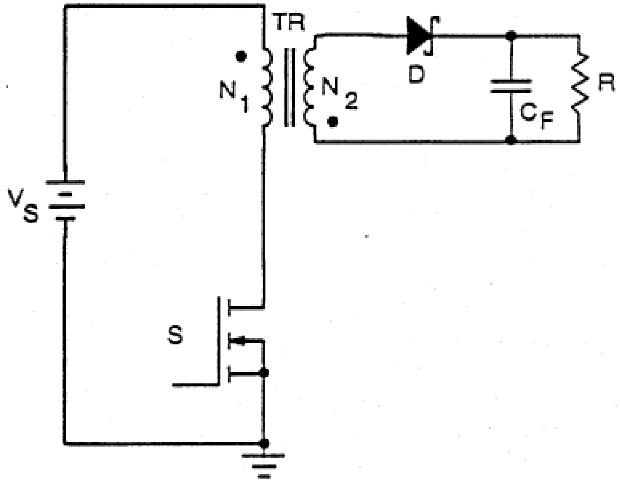
Snubber Loss

Gate-Drive Miller Effect

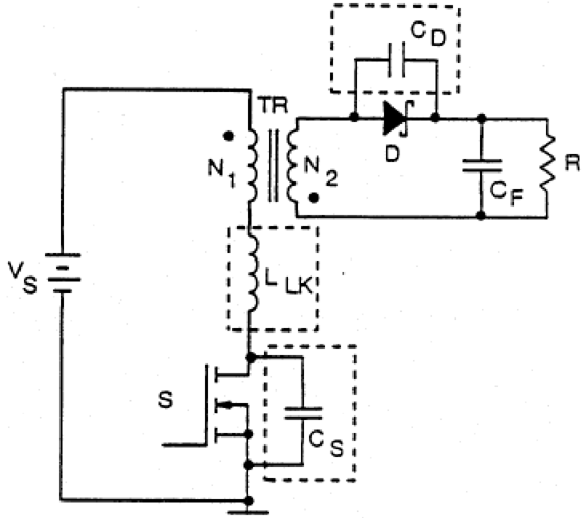
Low Efficiency at HF

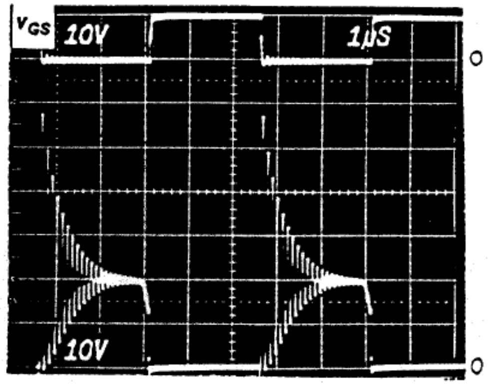
反激变换器（Flyback converter ）

without parasitic

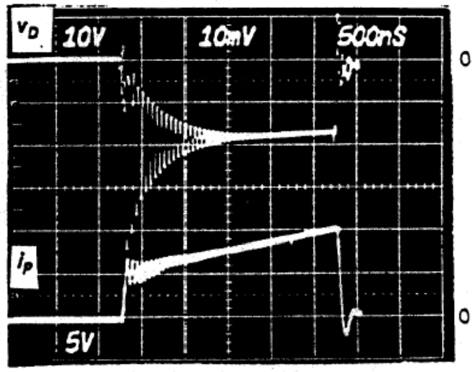


with parasitic



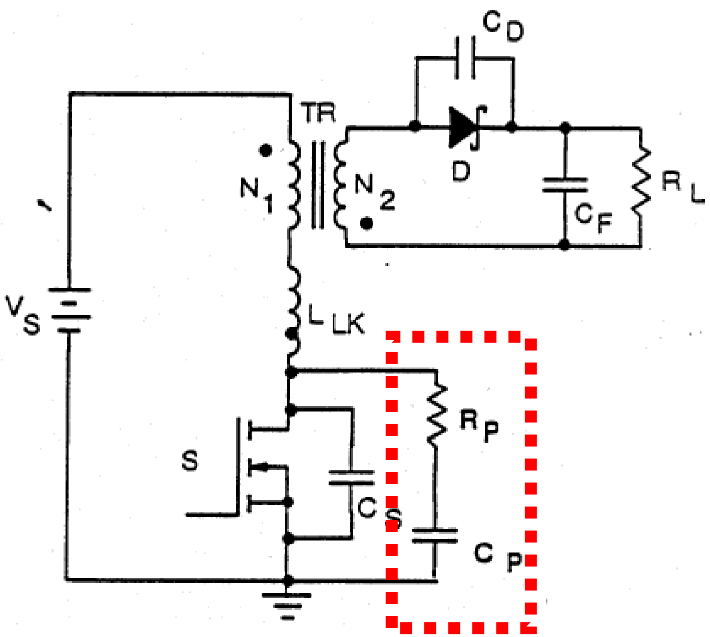


Gate-to-source (v_{GS}) and drain-to-source (v_{DS}) voltage waveforms of a PWM flyback converter without snubbers.
scales: 10 V/div ; 1 μ/div

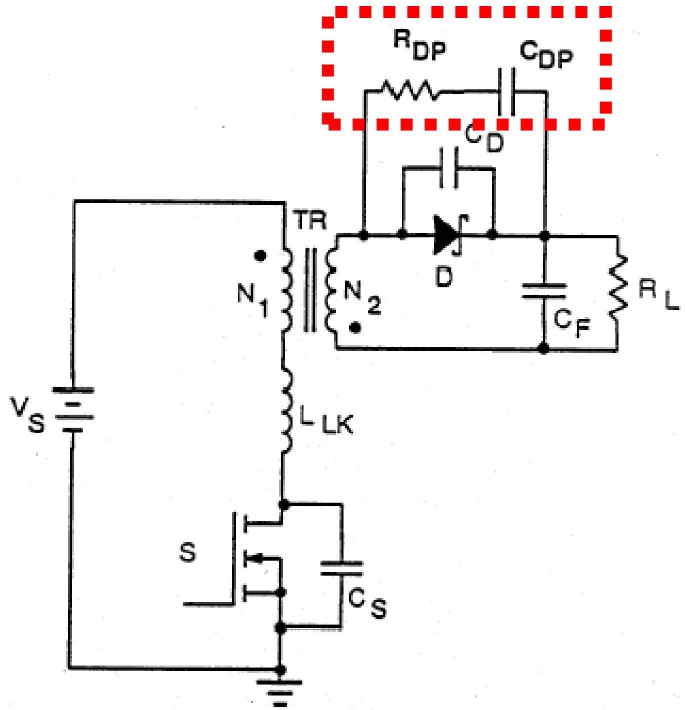


Rectifier voltage (v_D) waveform and primary current (I_p) waveform of a PWM flyback converter without snubbers.
scales: 10 V/div ; 1 A/div ; 500 ns/div.

吸收电路



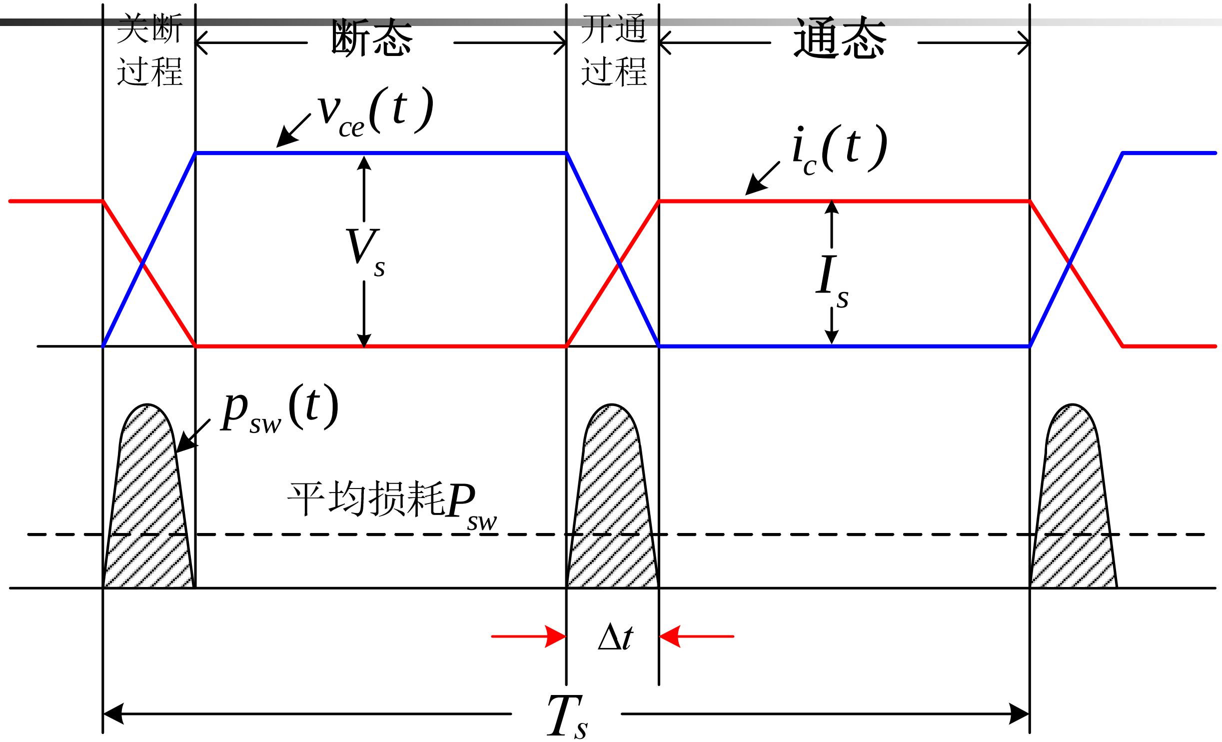
Primary switch RC snubber

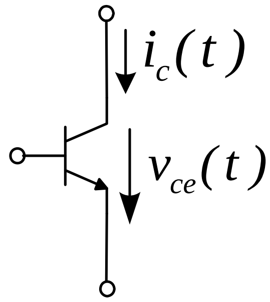


Rectifier snubber

振荡被抑制,但造成能量的损耗

开关过程和开关损耗（Hard switching operation）





$$P_{sw}=\frac{1}{T_s}\int_0^{T_s} v_{ce}(t)\cdot i_c(t)dt=\frac{2}{T_s}\int_0^{\Delta t} v_{ce}(t)\cdot i_c(t)dt$$

$$=\frac{2}{T_s}\int_0^{\Delta t}\left(-\frac{V_s}{\Delta t}t+V_s\right)\frac{I_s}{\Delta t}tdt=\frac{1}{3}V_sI_sf_s\Delta t$$

开关频率 $f_s=\frac{1}{T_s}$

开关损耗（Switching loss）

$$P_{sw}=\frac{1}{T_s}\int_0^{T_s} v_{ce}(t)\cdot i_c(t)dt=\frac{2}{T_s}\int_0^{\Delta t} v_{ce}(t)\cdot i_c(t)dt$$

$$=\frac{2}{T_s}\int_0^{\Delta t}(-\frac{V_s}{\Delta t}t+V_s)\frac{I_s}{\Delta t}tdt=\frac{1}{3}V_sI_sf_s\Delta t$$

平均开关损耗功率与开关频率 f_s 和重叠时间 Δt 之积成正比

在高频应用场合为抑制开关损耗，需选用开关速度快的器件

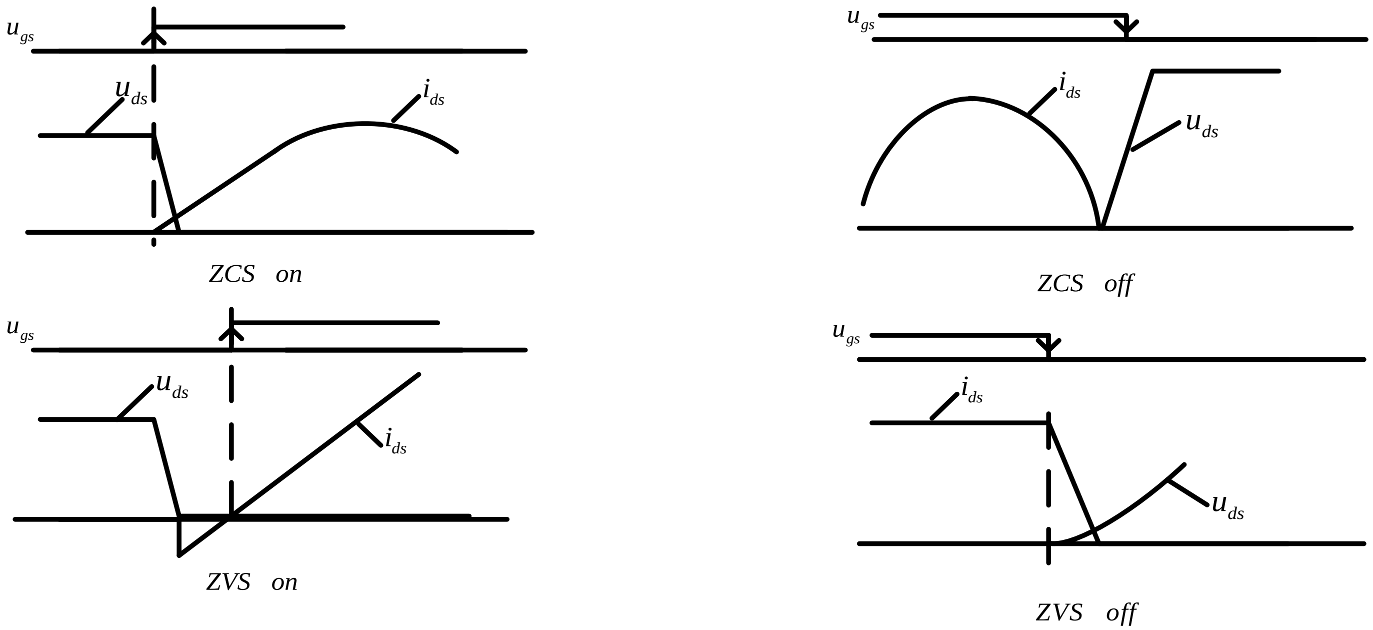
减少重叠时间（Reduce overlapping time）

- **电力电子电路的高频化**
  - 可以减小滤波器、变压器的体积和重量，电力电子装置小型化、轻量化。
  - 开关损耗增加，电路效率严重下降，电磁干扰增大。

- **软开关技术**
  - 降低开关损耗和开关噪声。
  - 使开关频率可以大幅度提高。

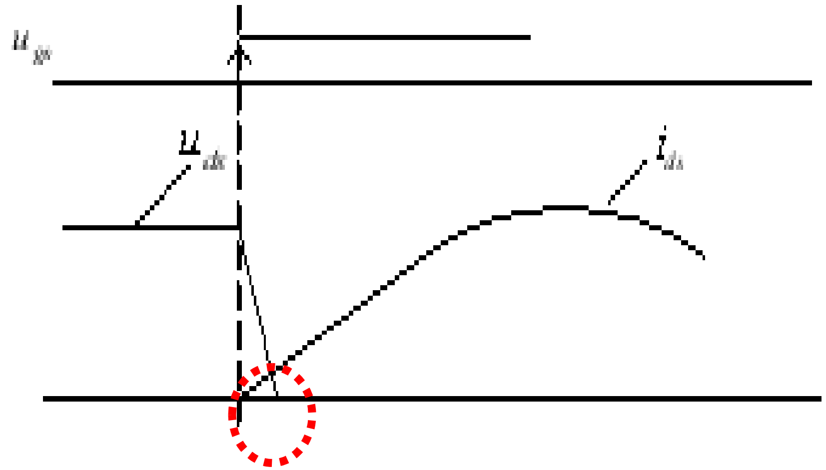
软开关的分类（Types of soft switching）

- **Cut down turn-on loss:**
  - **ZCS on**
  - **ZVS on**
- **Cut down turn-off loss:**
  - **ZCS off**
  - **ZVS off**



零电流开通Zero current switch on(ZCS on)

Turn on with zero current



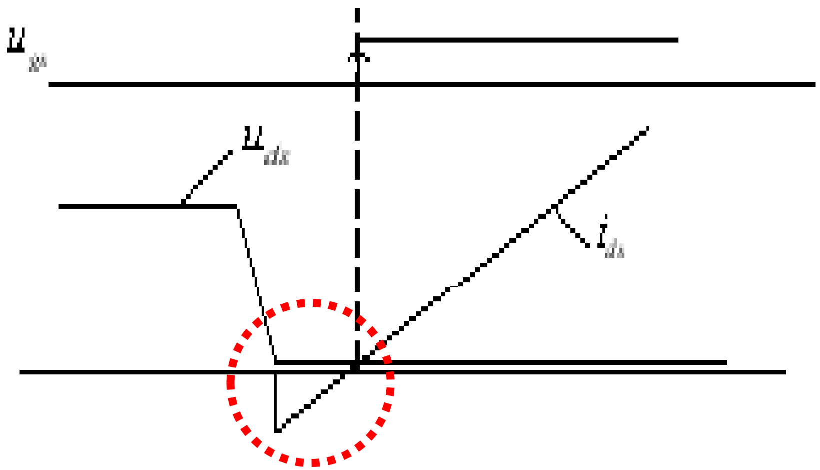
Overlap time still exist

But integral of multiplication of u_{ds} and i_{ds} is reduced

Turn-on switching loss is reduced

零电压开通Zero voltage switch on(ZVS on)

Turn on with zero voltage



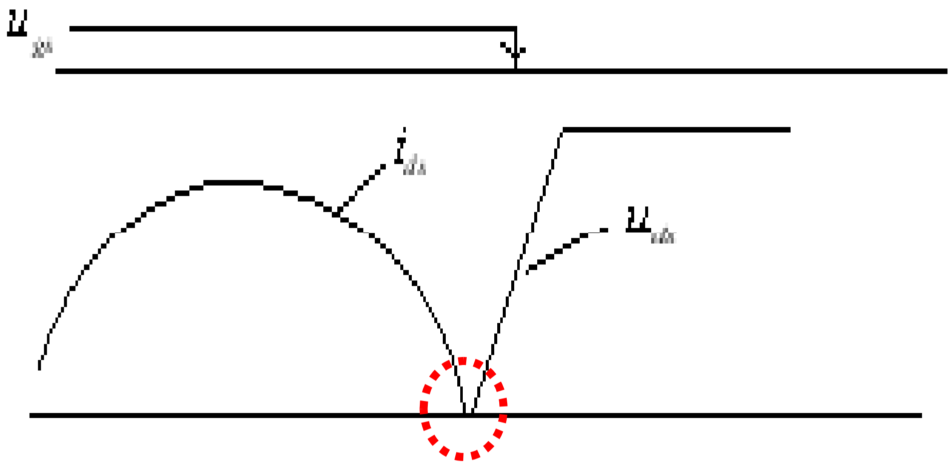
Overlap time is zero

integral of multiplication of u_{ds} and i_{ds} is 0

Turn-on switching loss is 0

零电流关断Zero current switch off(ZCS off)

Turn off with zero current



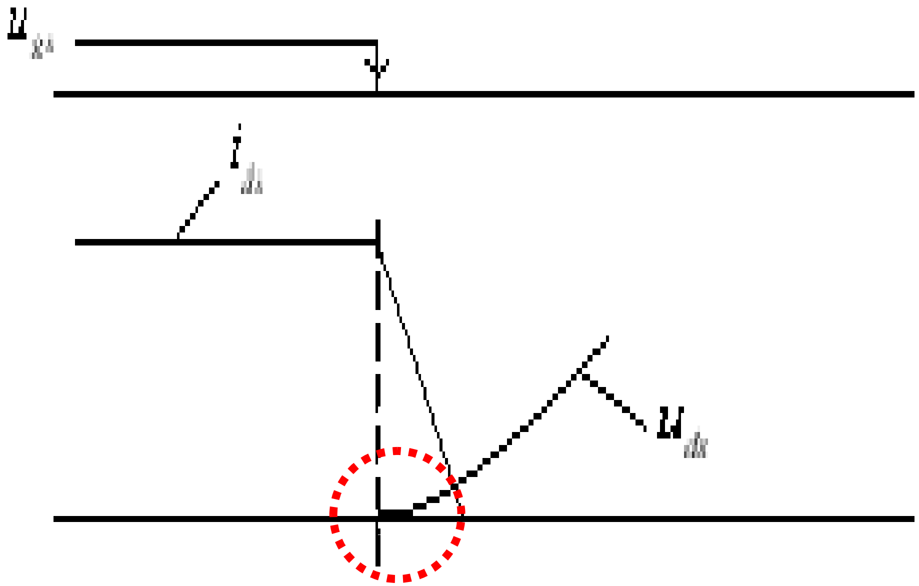
Overlap time is zero

integral of multiplication of u_{ds} and i_{ds} is 0

Turn-off switching loss is 0

零电压关断Zero voltage switch off(ZVS off)

Turn off with zero voltage

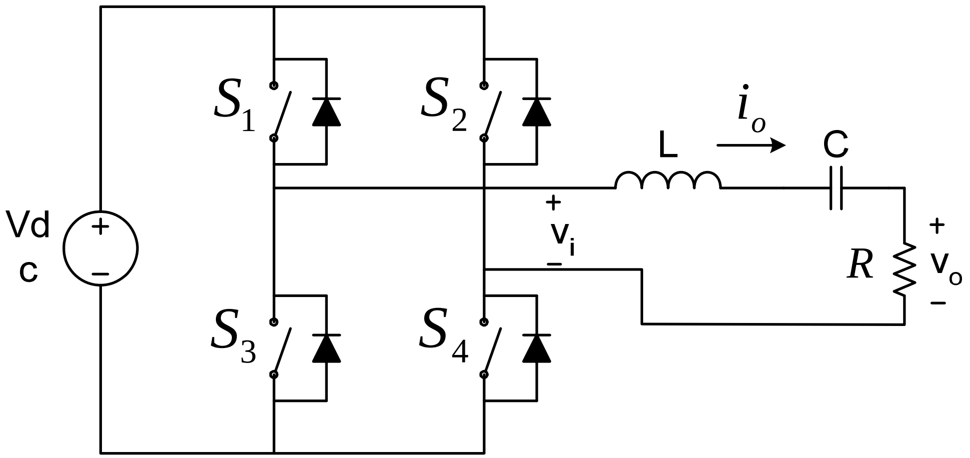


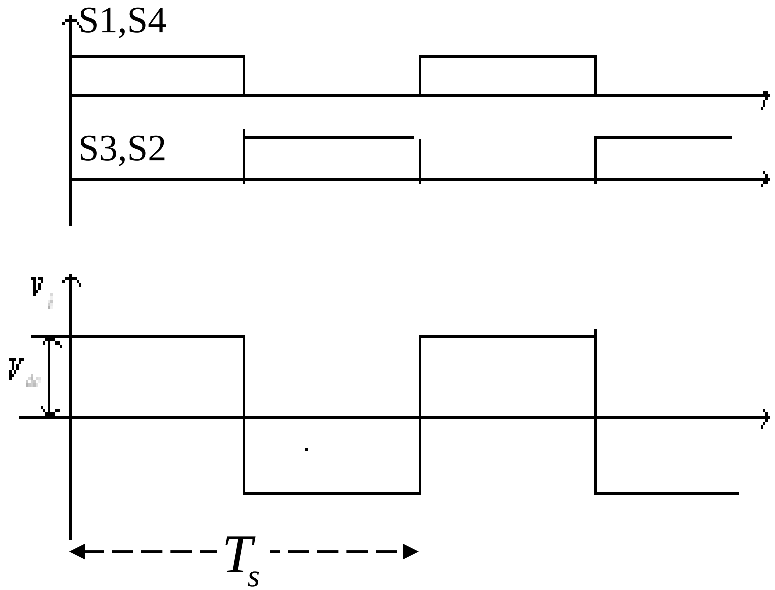
Overlap time still exist

But integral of multiplication of u_{ds} and i_{ds} is reduced

Turn-off switching loss is reduced

串联谐振逆变器（Series resonant inverter）





- Gate signal for S1 and S4 are the same
- Gate signal for S2 and S3 are the same
- Duty ratio of all the switches is 50%

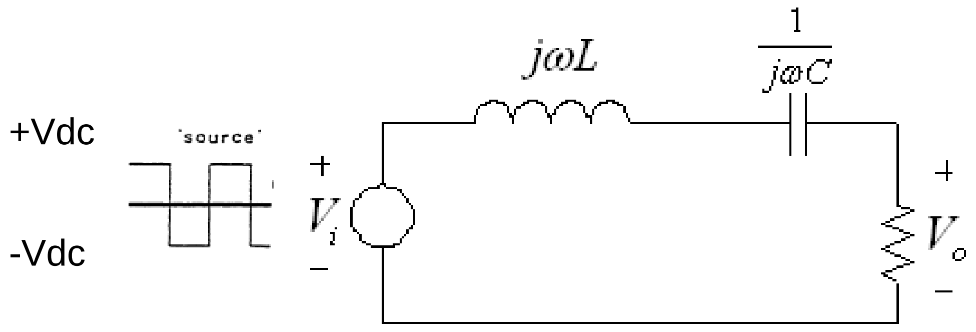
- ✓ S1 and S3 operate complementally
- ✓ S2 and S4 also operate complementally
- ✓ V_i is square wave, freq: fs=1/Ts

基波等效电路（Equivalent circuit ）

简化:分析基波分量之间的关系，而忽略谐波分量的作用

- Vi: square waveform   Amplitude: ±Vdc   freq: fs
- Amplitude of fundamental component

$$V_1 = \frac{4V_{dc}}{\pi}$$



- In-out ratio:

$$\frac{V_o}{V_i} = \frac{R}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} = \frac{1}{\sqrt{1 + (\frac{\omega L}{R} - \frac{1}{\omega RC})^2}}$$

$$\omega = 2\pi f_s$$

fs: Switching frequency

输入输出比（Input-output ratio）

$$\frac{V_o}{V_i}=\frac{R}{\sqrt{R^2+(\omega L-\frac{1}{\omega C})^2}}=\frac{1}{\sqrt{1+\frac{L}{R^2C}(\omega\sqrt{L}\sqrt{C}-\frac{1}{\omega\sqrt{L}\sqrt{C}})^2}}$$

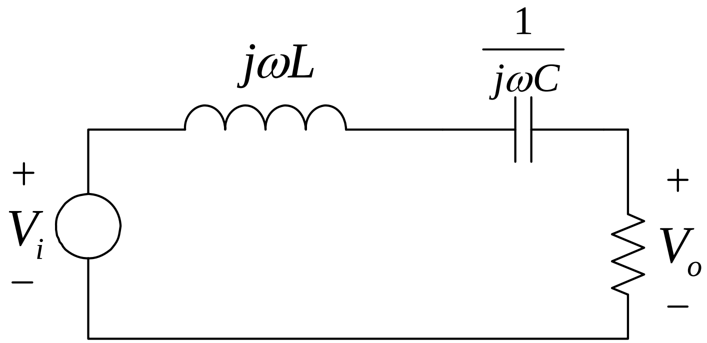
- Quality factor

$$Q=\frac{\omega_o L}{R}=\frac{1}{\omega_o RC}=\frac{\sqrt{\frac{L}{C}}}{R}$$

  - Natural resonant frequency $\omega_o=2\pi f_o=\frac{1}{\sqrt{LC}}$

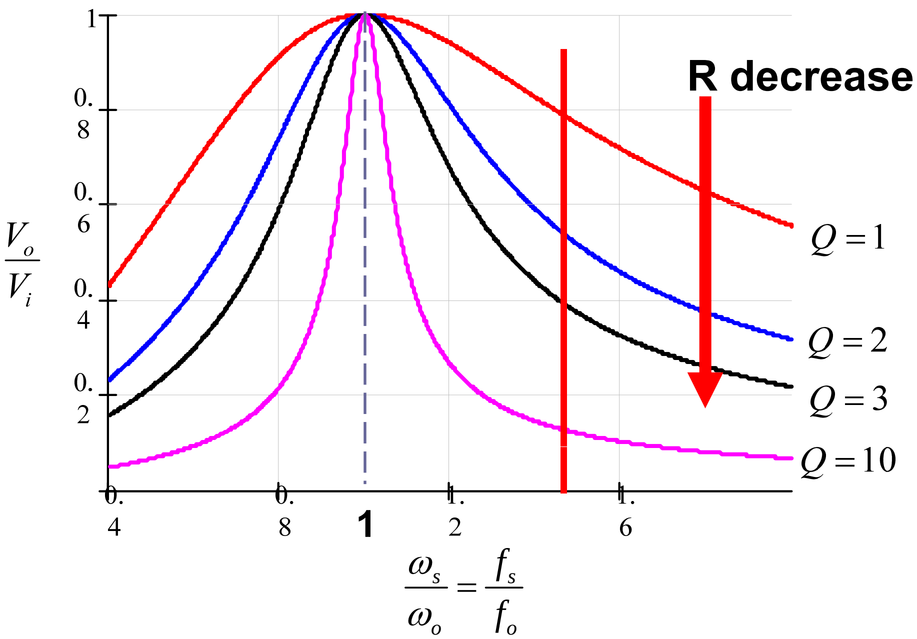
$$\frac{V_o}{V_i}=\frac{1}{\sqrt{1+Q^2(\frac{\omega}{\omega_o}-\frac{\omega_o}{\omega})^2}}=\frac{1}{\sqrt{1+Q^2(\frac{f}{f_o}-\frac{f_o}{f})^2}}$$

输入输出比（Input-output ratio）



$$\frac{V_o}{V_i} = \frac{1}{\sqrt{1+Q^2\left(\frac{\omega}{\omega_o}-\frac{\omega_o}{\omega}\right)^2}}$$

$$Q = \frac{\sqrt{L/C}}{R}$$



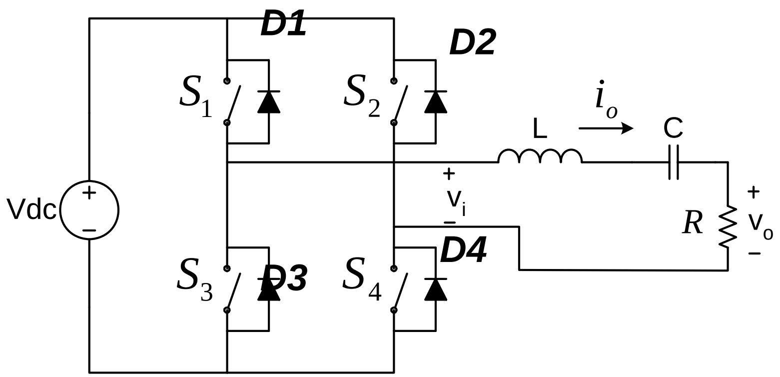
- Common point: (f*=1, Vo/Vi=1)
- Q increases, then Vo decrease w/ fixed fs
- f*>1, inductive load, delayed phase
- f*<1, capacitive load, leading phase

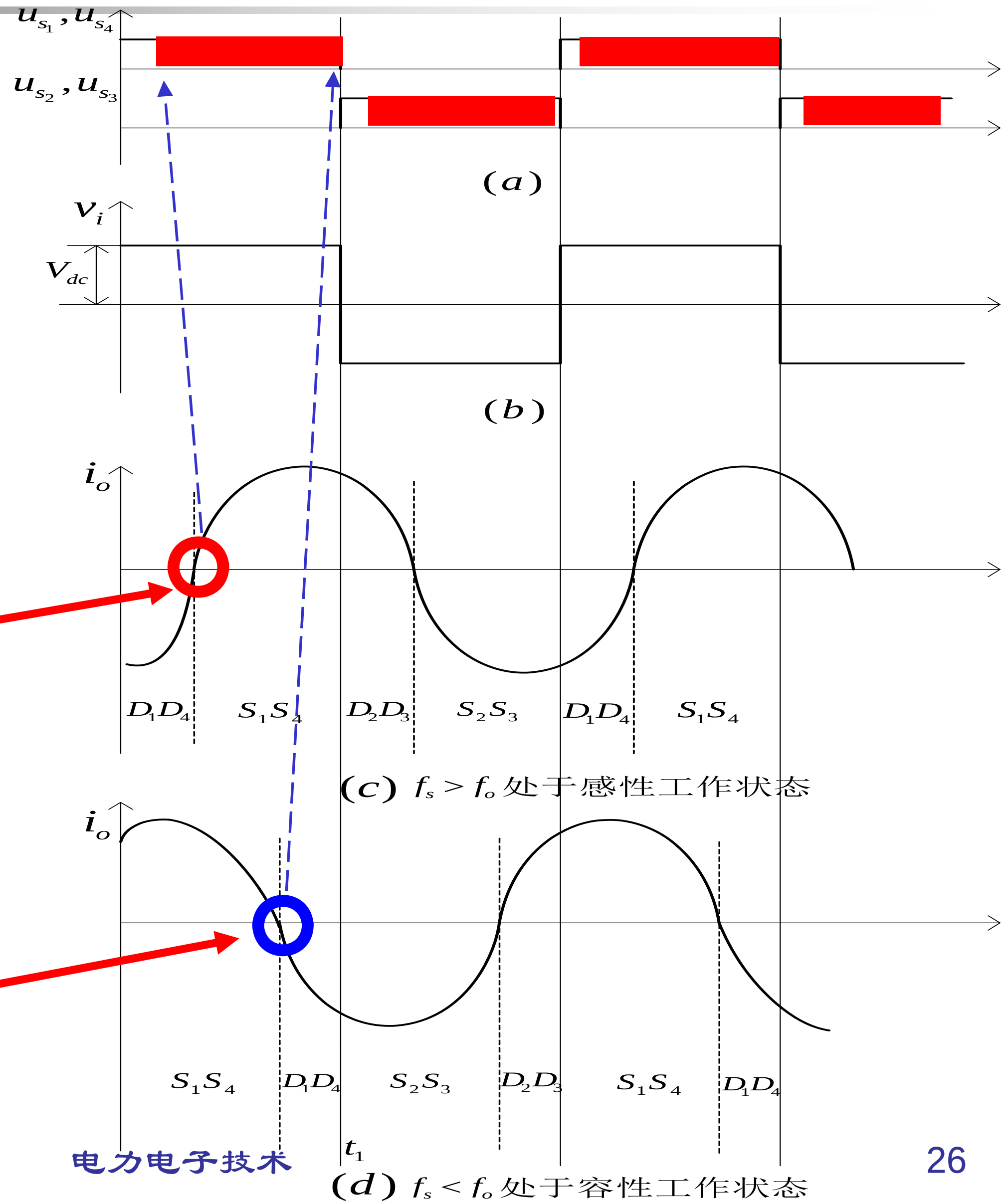
Vo vs. f* curve w/ constant Q

- f*>1, decrement function
- f*<1, increment function
- Vo can be regulated by changing fs

f*=fs/fo

Inverter stage analysis





$f_s > f_o$

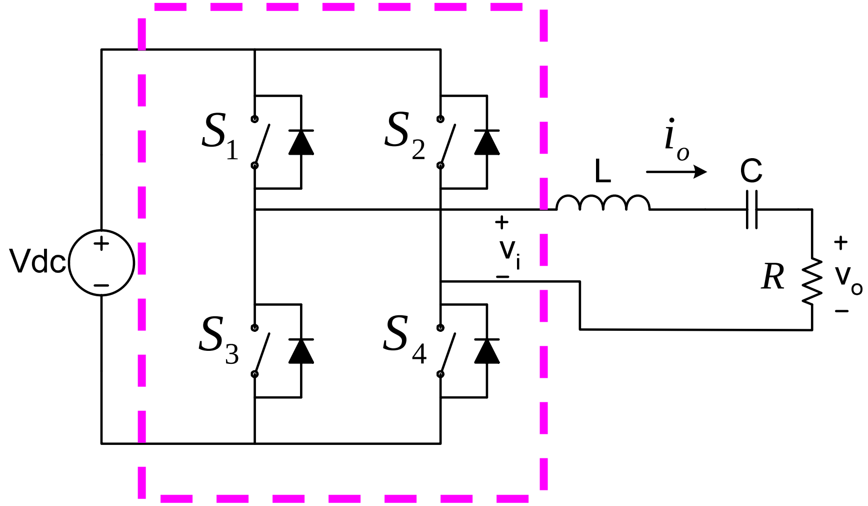
- RLC load is inductive
- *Vi* is leading to *Io*
- ZVS switching on

$f_s < f_o$

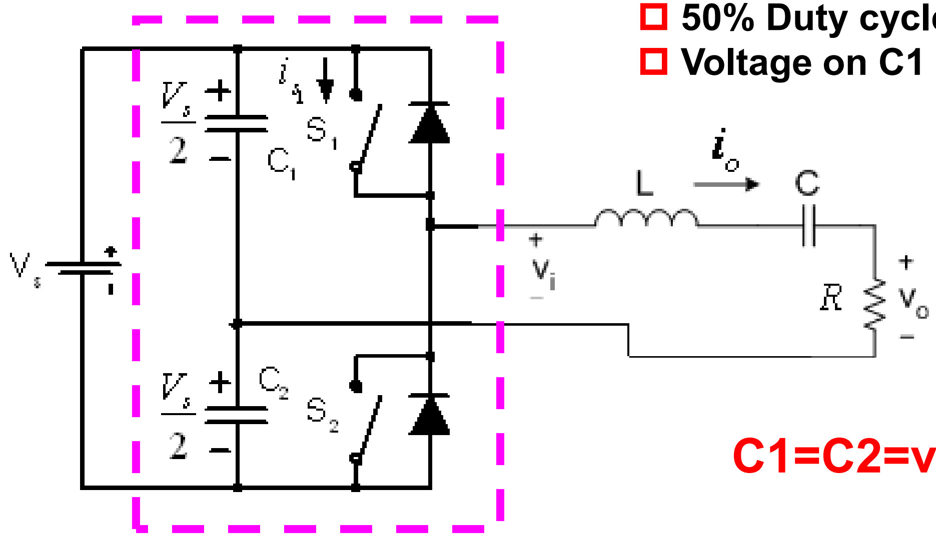
- RLC load is capacitive
- *Io* is leading to *Vi*
- ZCS switching off

Inverter bridge variations

- Full bridge



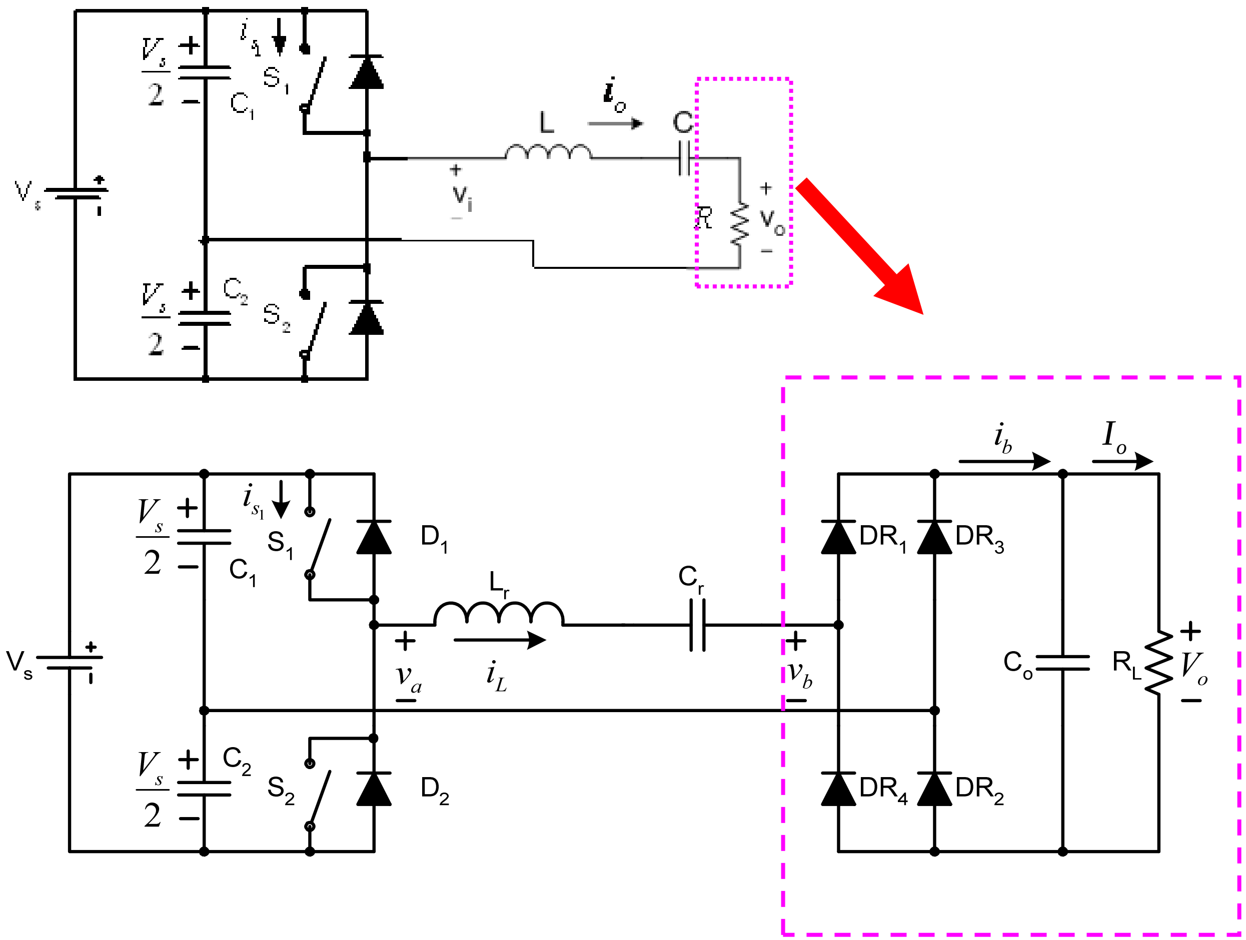
- Half bridge



- S1 and S2 gate signal are complement
- 50% Duty cycle
- Voltage on C1 and C2 are constant, =Vs/2

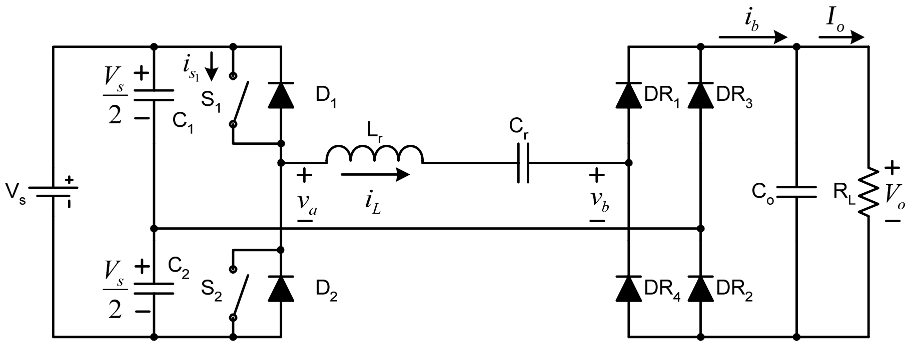
C1=C2=very large

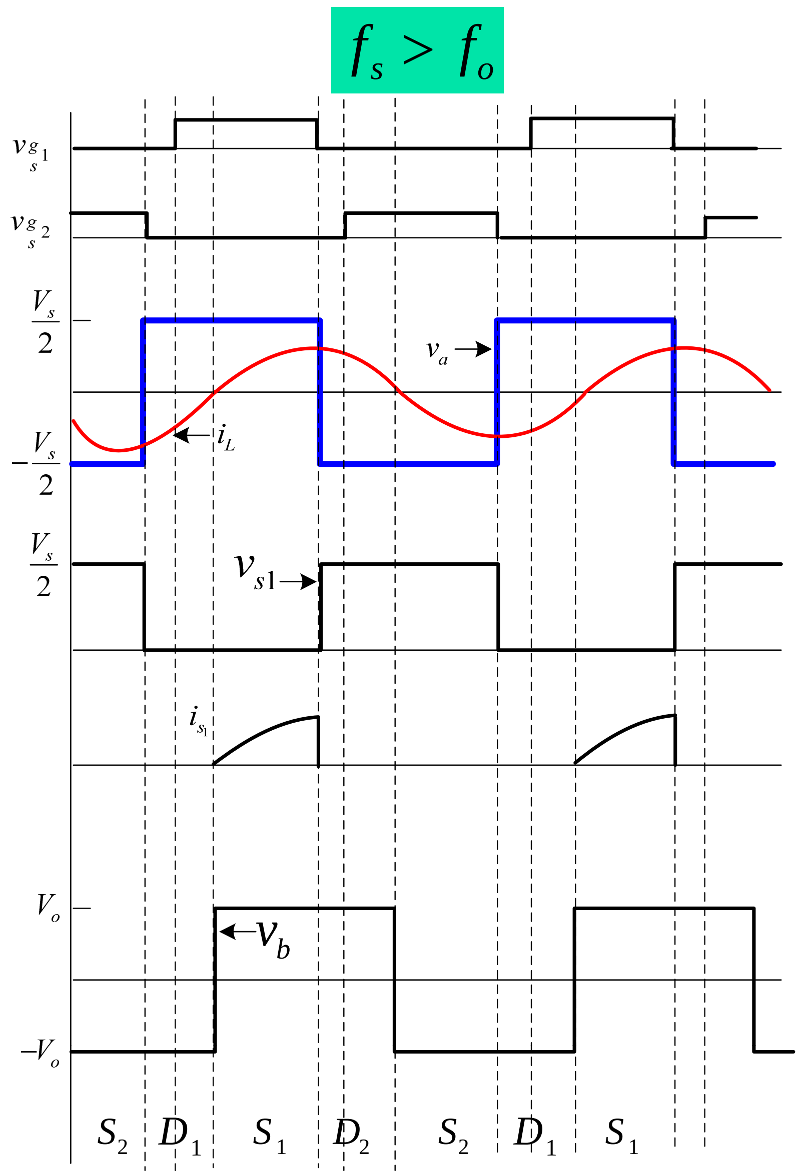
串联谐振变换器（Series resonant DC/DC converter）



R **in the resonant inverter is replaced by a full bridge rectifier**

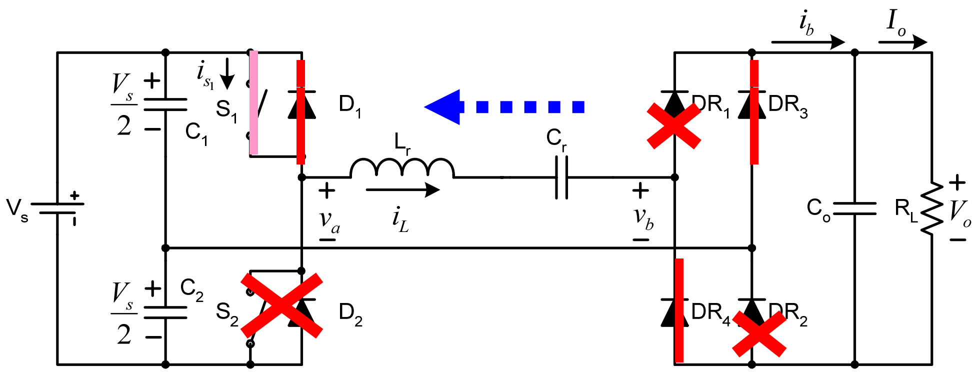
感性方式（Inductive operation）

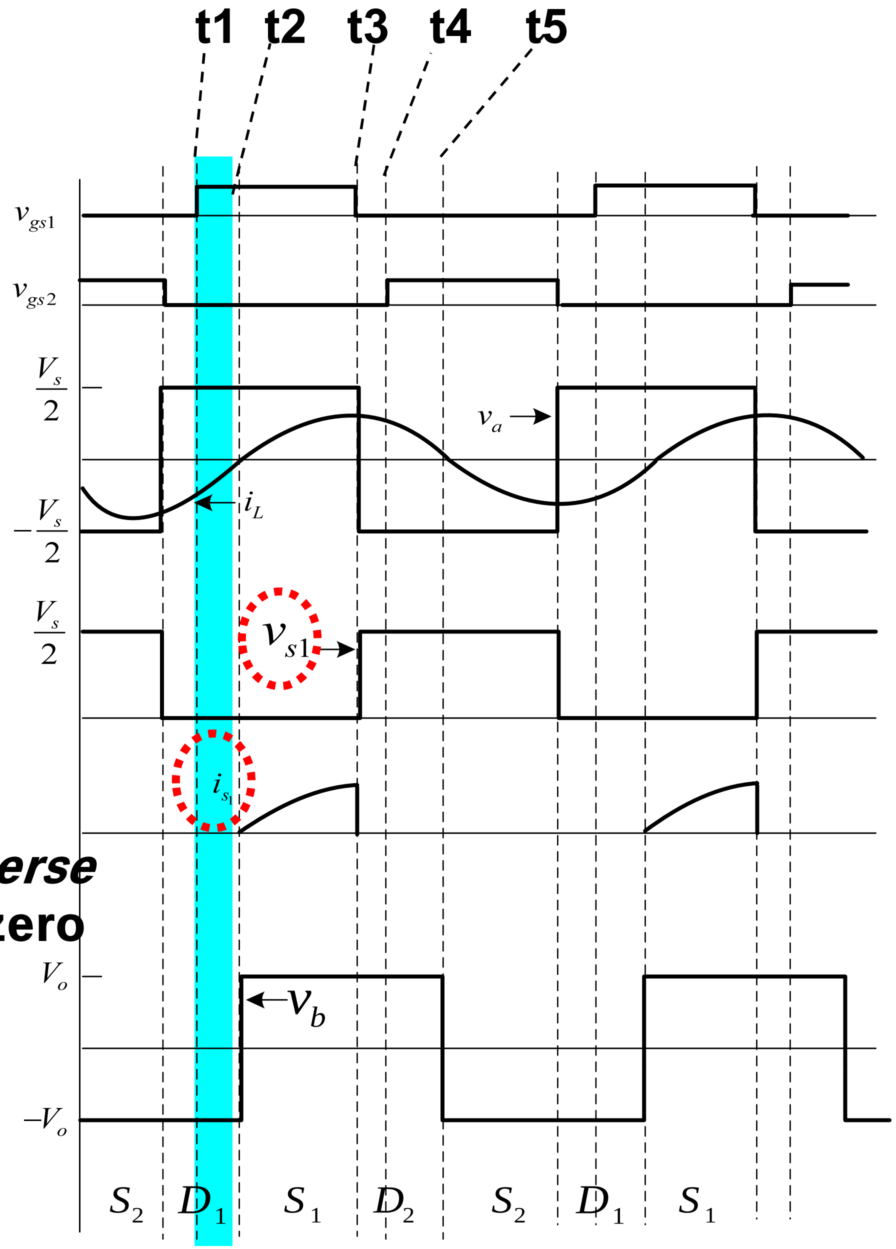




- **Resonant current is lagging**
- **S1 and S2: ZVS switching on**
- **S1 and S2 turn off loss reduction: Parallel capacitor on switches**

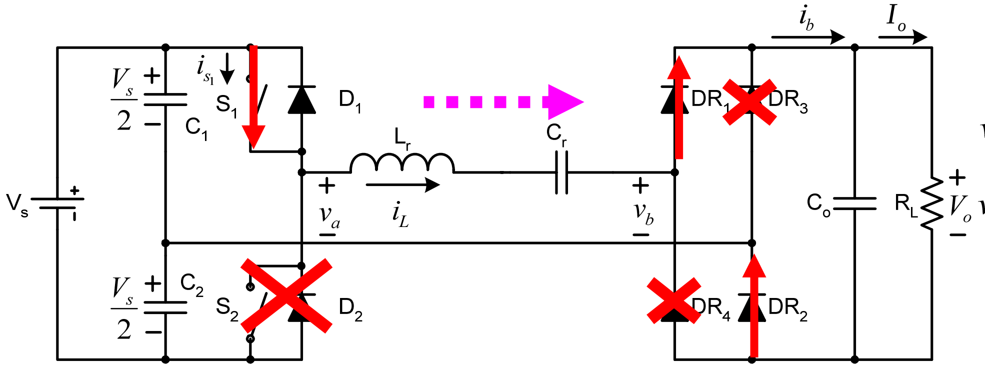
stage 1:[t1,t2] Reactive power flow stage

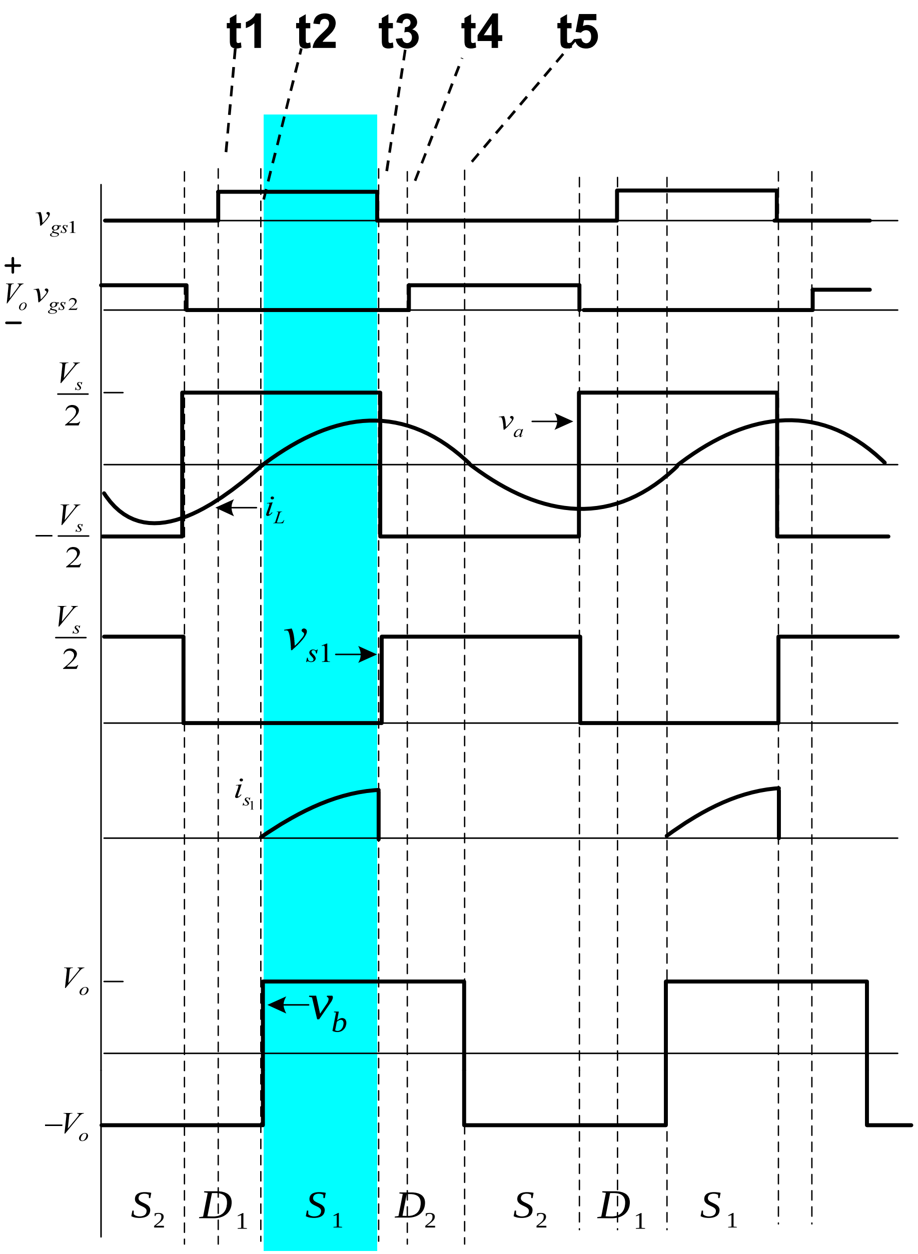




- **Half bridge:**
  - **D1 is on, S1 is ready to turn on**
  - **S2(D2) is off**
- **Rectifier:**
  - **DR3, DR4 are on**
  - **DR1,DR2 are off**
- ***Since v_a>0 & i_L<0, power flow is reverse***
- **Stage end condition: *i_L* increases to zero**
  - **D1 is conducting**
  - **S1 is ready to be turned on with ZVS**

stage 2:[t2,t3] Active power flow stage





Half bridge: S1 is on, D1 is off
S2(D2) is off

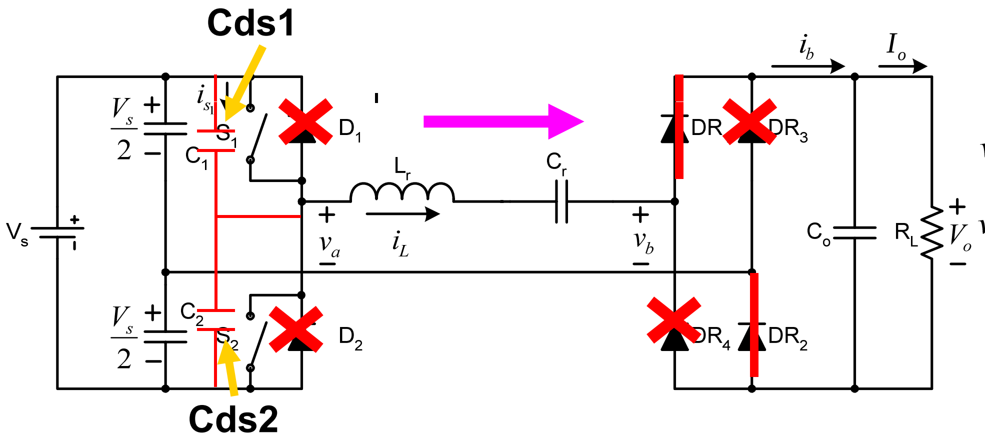
Rectifier: DR3, DR4 are off
DR1,DR2 are on

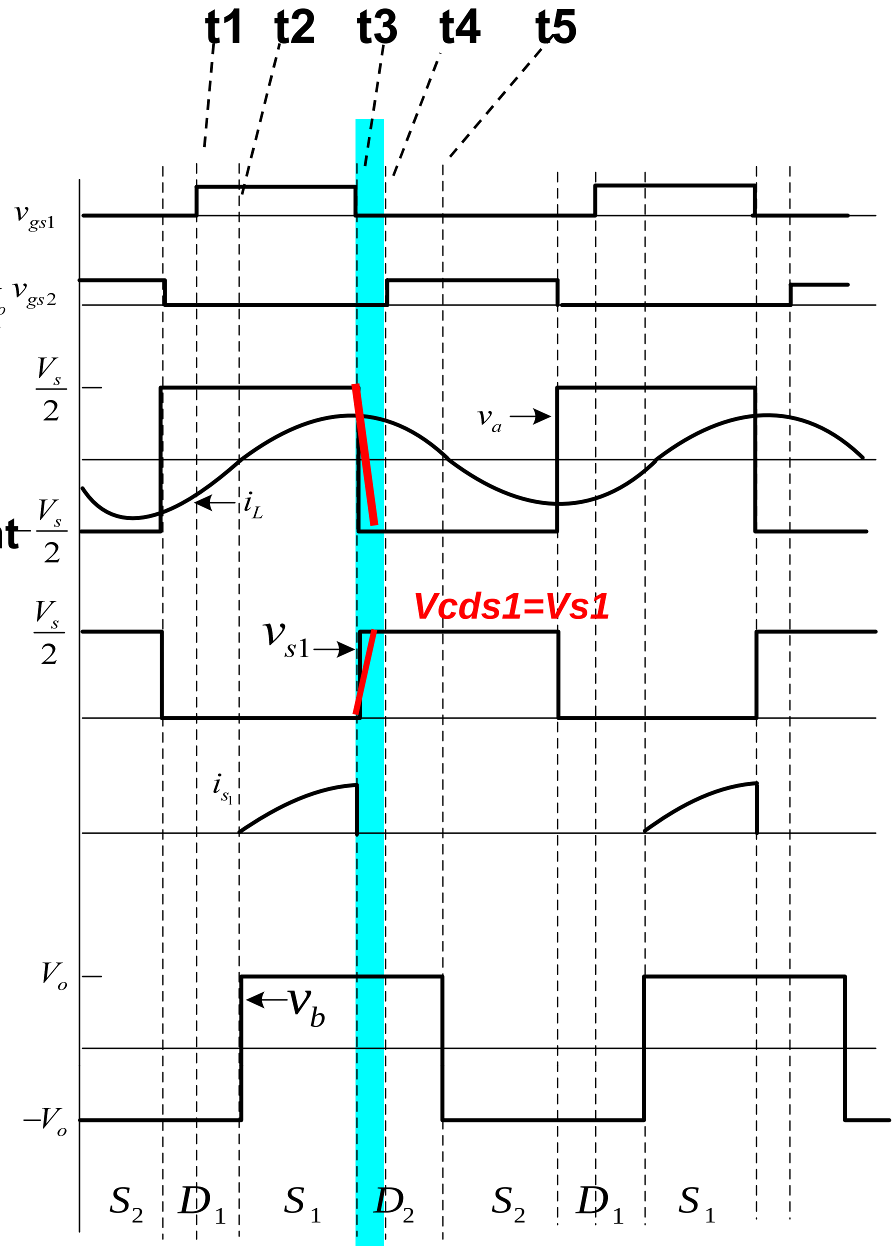
Since *Va>0 & IL>0,* power flow is forward

Stage end condition: *Vgs1* steps down

stage 3:[t3,t4]Resonant stage

Capacitance of MOSFETs





Since t3 to t4 is short, i_L is taken to be constant

$$v_{Cds1} + v_{Cds2} = V_S$$

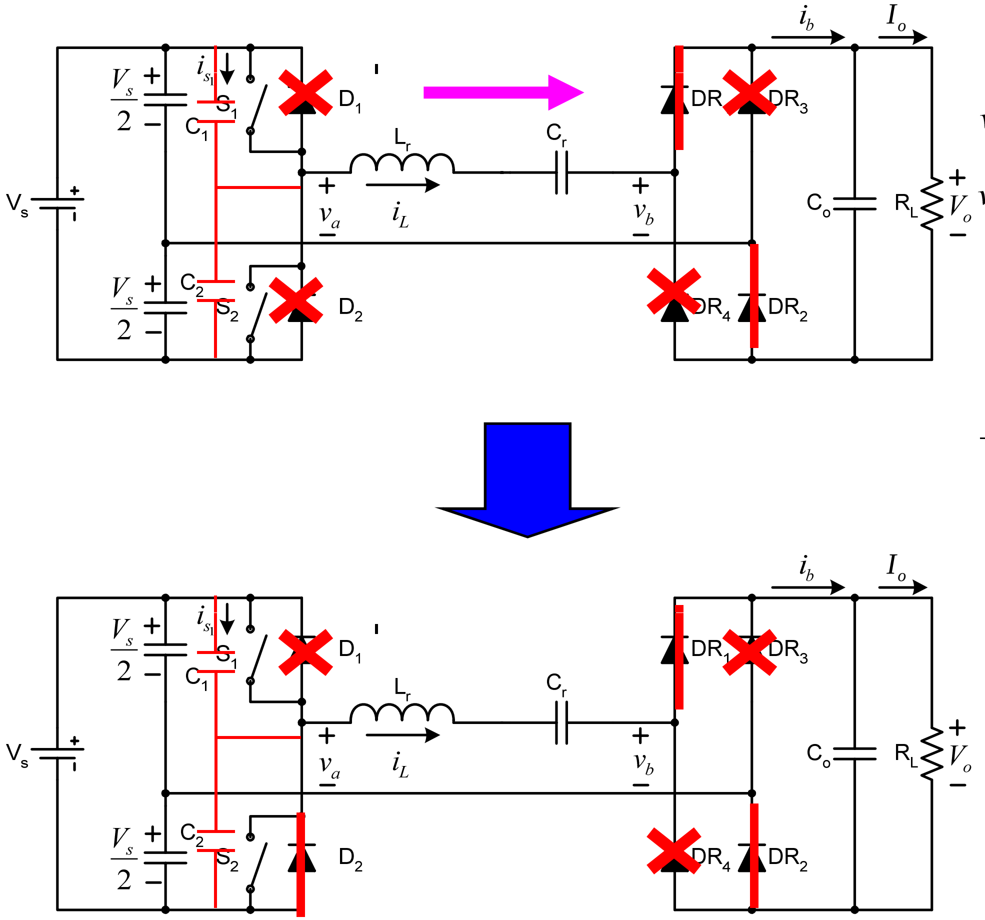
v_{Cds1} **Linearly increases from 0 to Vs**

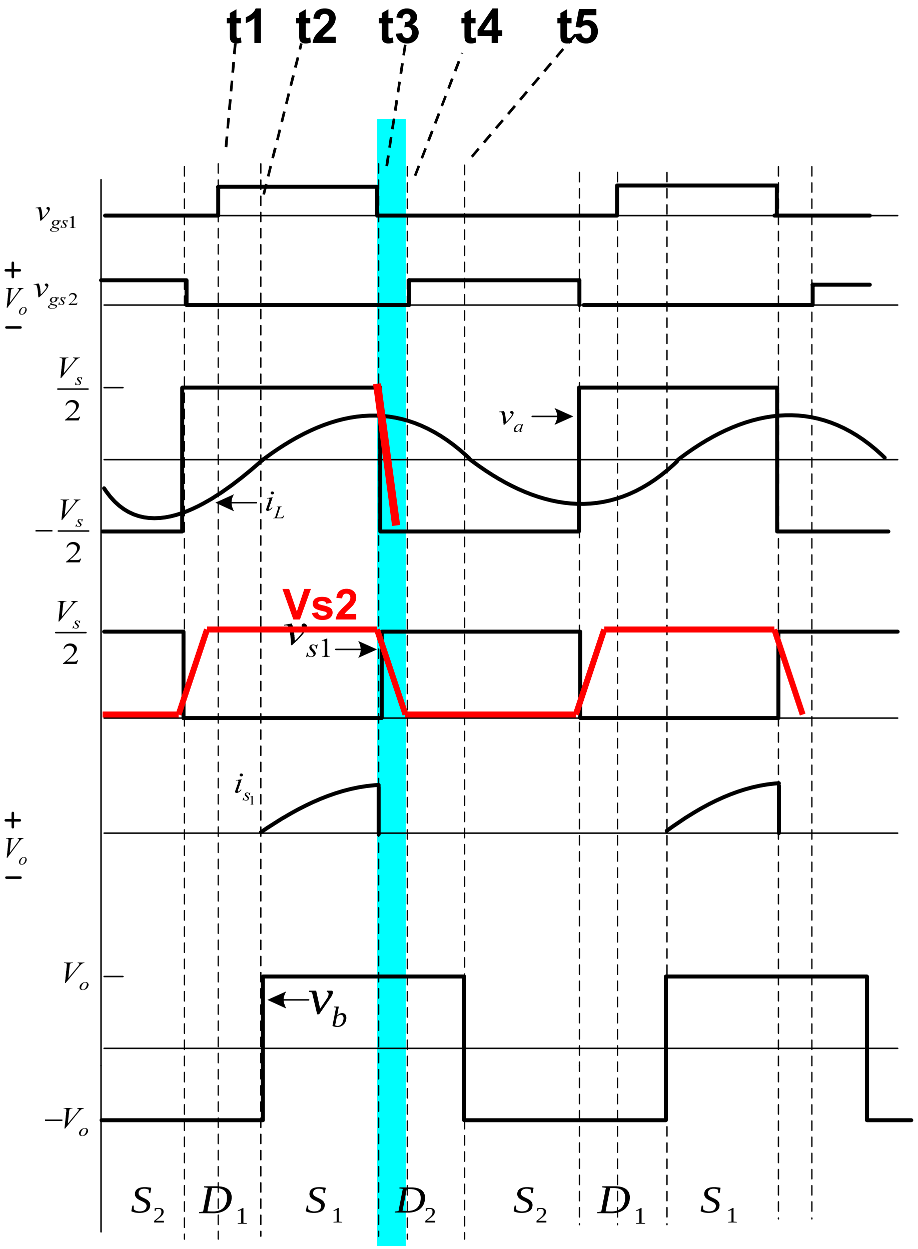
v_{Cds2} **Linearly decreases from *Vs*** to 0

Stage end condition:

***Vcds2*=0, then D2 is turned on**

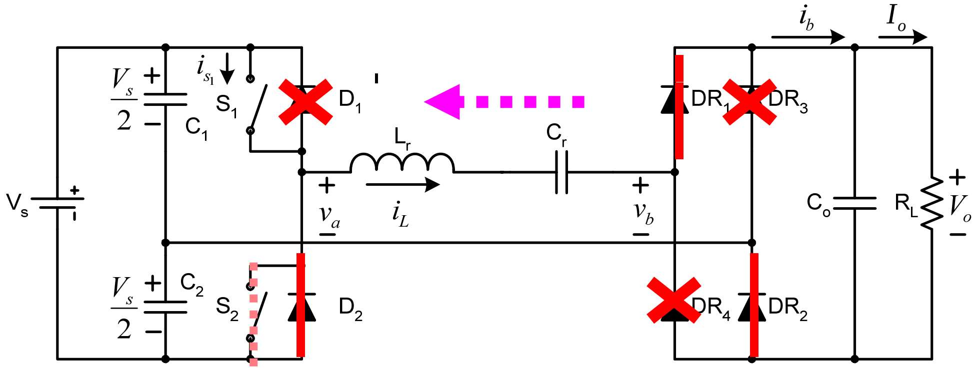
stage 3:[t3,t4]Resonant stage (continued)

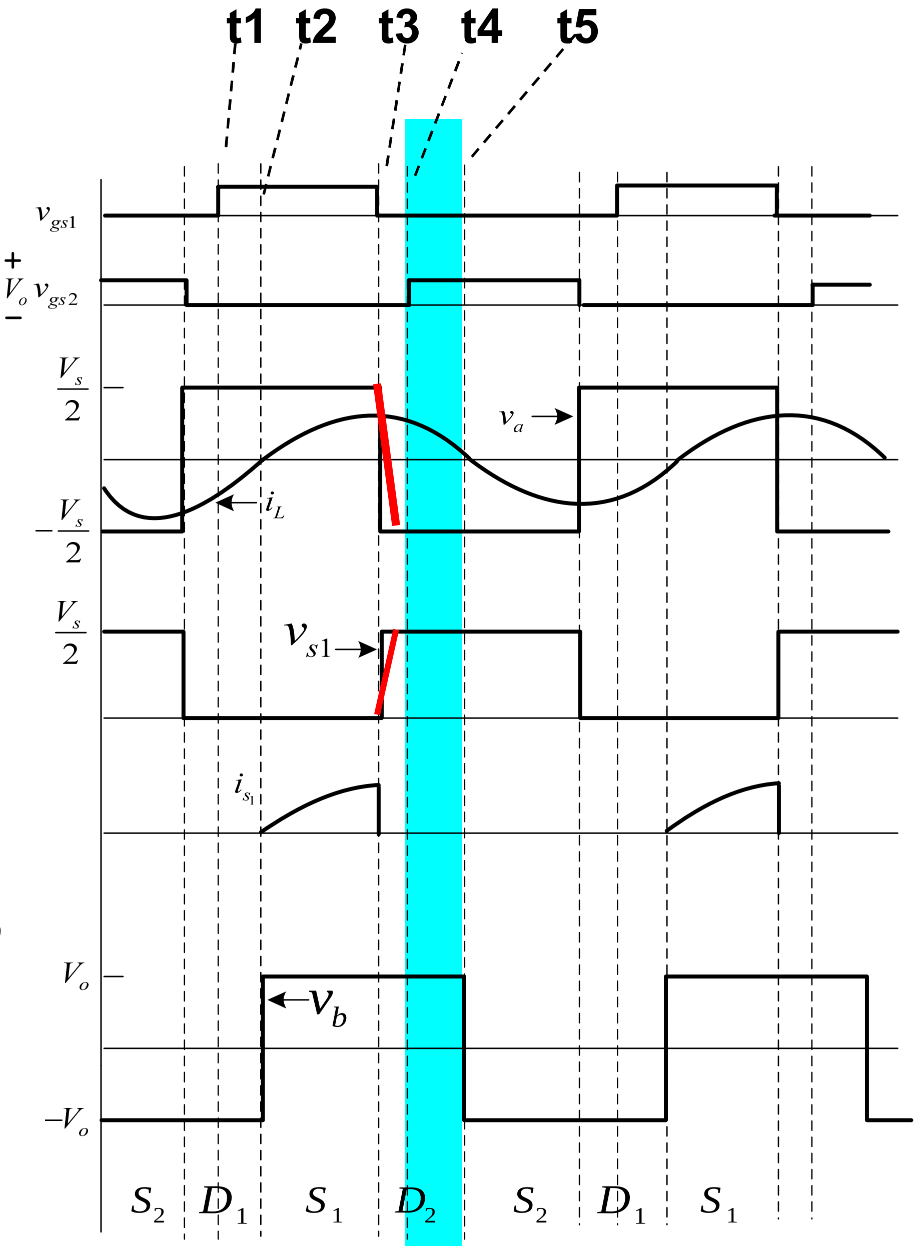




- D2 is conducting
- S2 is ready to be turned on with ZVS

stage 4:[t4,t5] reactive power flow stage





Half bridge:

S1(D1) is off

D2 is on, S2 ?

Rectifier:

DR3, DR4 are off

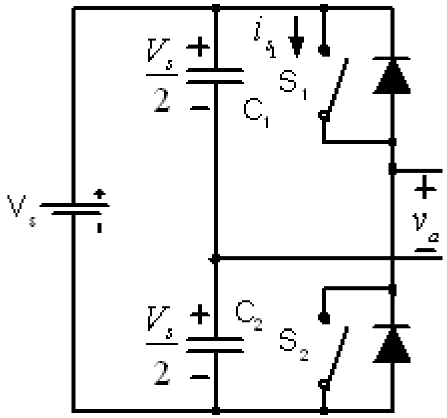
DR1,DR2 are on

Since Va<0 & IL>0, power flow is reverse

Stage end condition: I_L decreases to zero

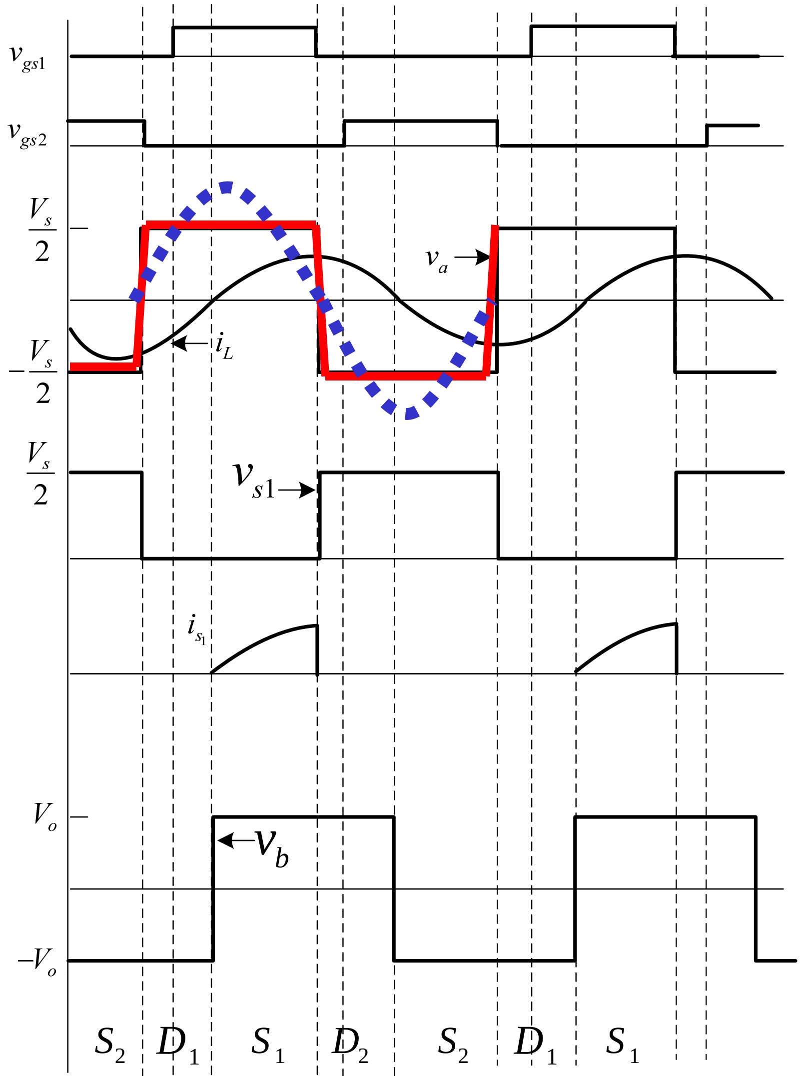
D2 is conducting and create the condition of zero voltage turn-on for S2

半桥逆变器的输出基波（Half bridge inverter）



- **va Square wave with amplitude vs/2**
- **Amplitude of the fundamental component**

$$V_{a1} = \frac{4(V_s/2)}{\pi} = \frac{2V_s}{\pi}$$



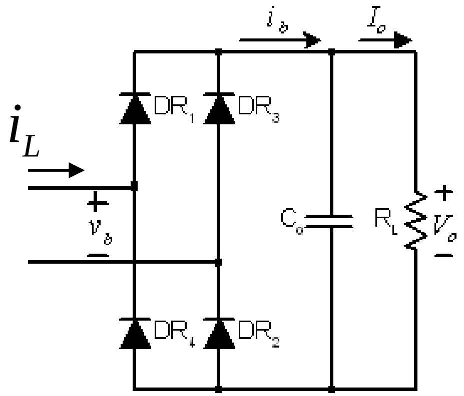
容性输出整流器（Capacitor filtered rectifier）

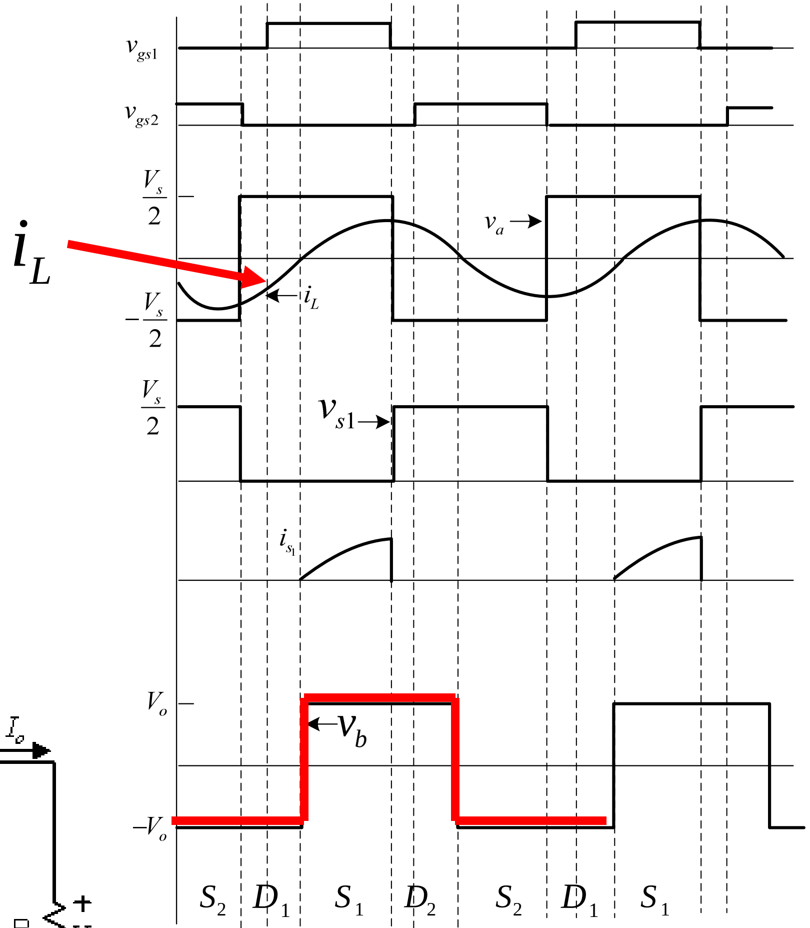
- Assumption: output V_o is constant
- Input voltage v_b is square wave. Amplitude of the fundamental component

$$V_{b1} = \frac{4V_o}{\pi}$$

- Since resonant circuit has filter property, its current can be seen as Sine wave.
- i_L Amplitude: I_{L1}
- I_b is rectified current of Averaged value of i_b

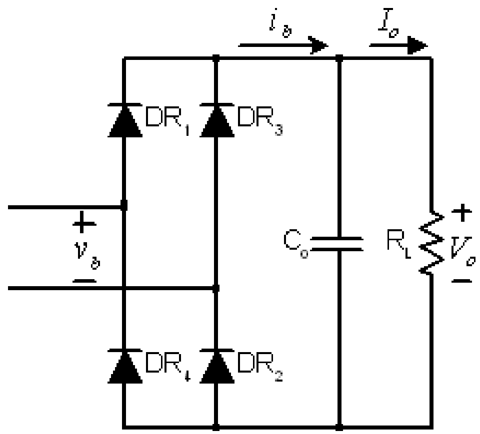
$$I_b = \frac{2I_{L1}}{\pi}$$





Capacitor filtered rectifier (continued)

$$I_b = I_o$$



- Output current

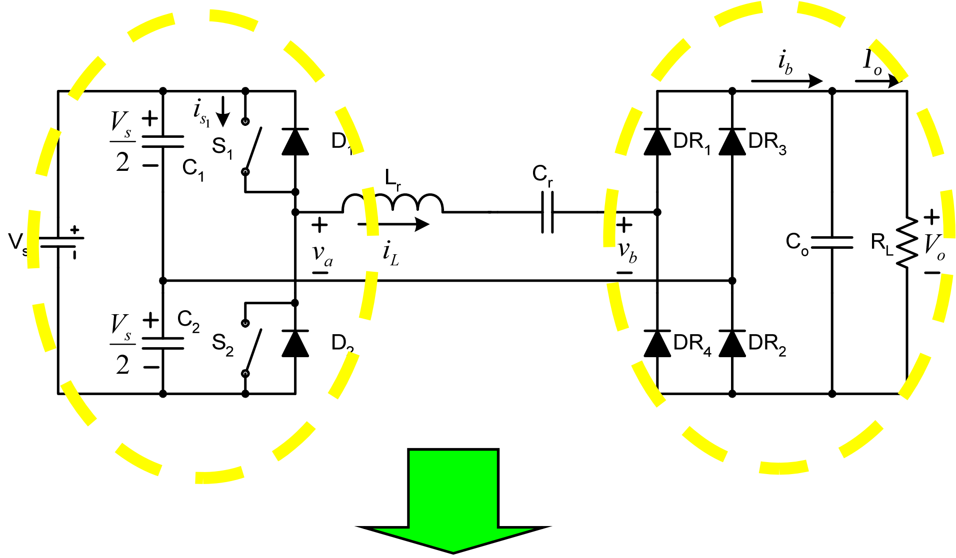
- Resonant circuit current amplitude

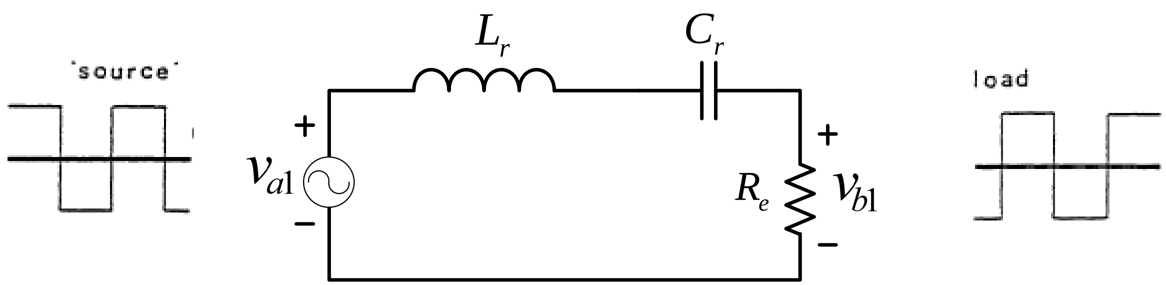
$$I_{L1} = \frac{\pi}{2} I_o$$

- Capacitor filtered rectifier can replaced by a equivalent resistor

$$R_e = \frac{V_{b1}}{I_{L1}} = \frac{\frac{4V_o}{\pi}}{\frac{\pi I_o}{2}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_L$$

基波等效电路（Fundamental equivalent circuit）



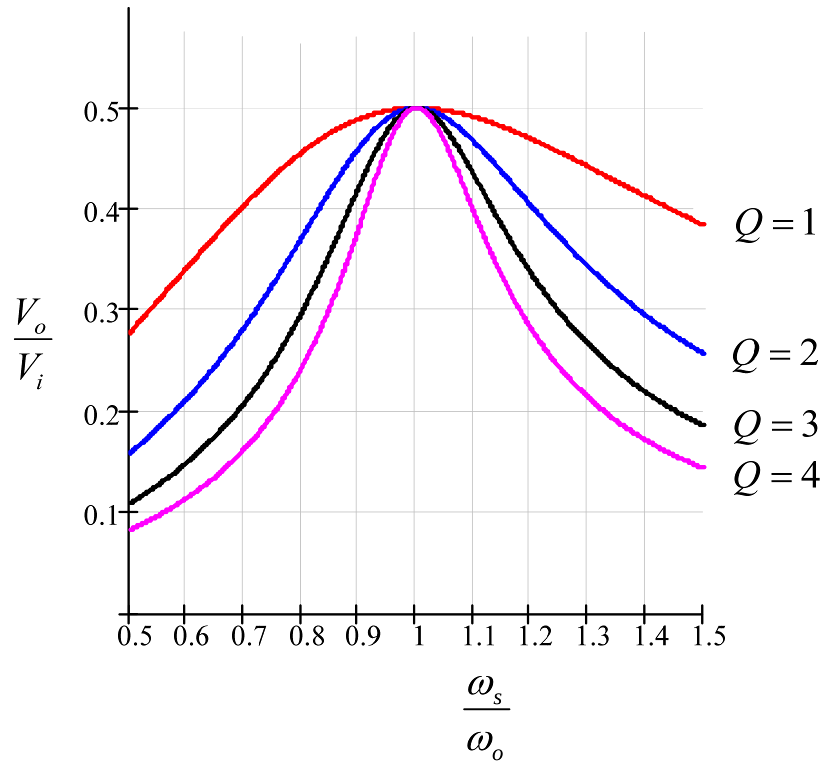


$$\frac{V_{b1}}{V_{a1}} = \frac{\frac{4V_o}{\pi}}{\frac{2V_s}{\pi}} = \left| \frac{R_e}{R_e + j(\omega_s L_r - \frac{1}{\omega_s C_r})} \right|$$

直流电压比（DC/DC conversion ratio）

$$\frac{V_o}{V_s} = \frac{1}{2\sqrt{1+Q^2\left(\frac{\omega_s}{\omega_o}-\frac{\omega_o}{\omega_s}\right)^2}}$$

$$Q = \frac{\omega_o L_r}{R_e}$$



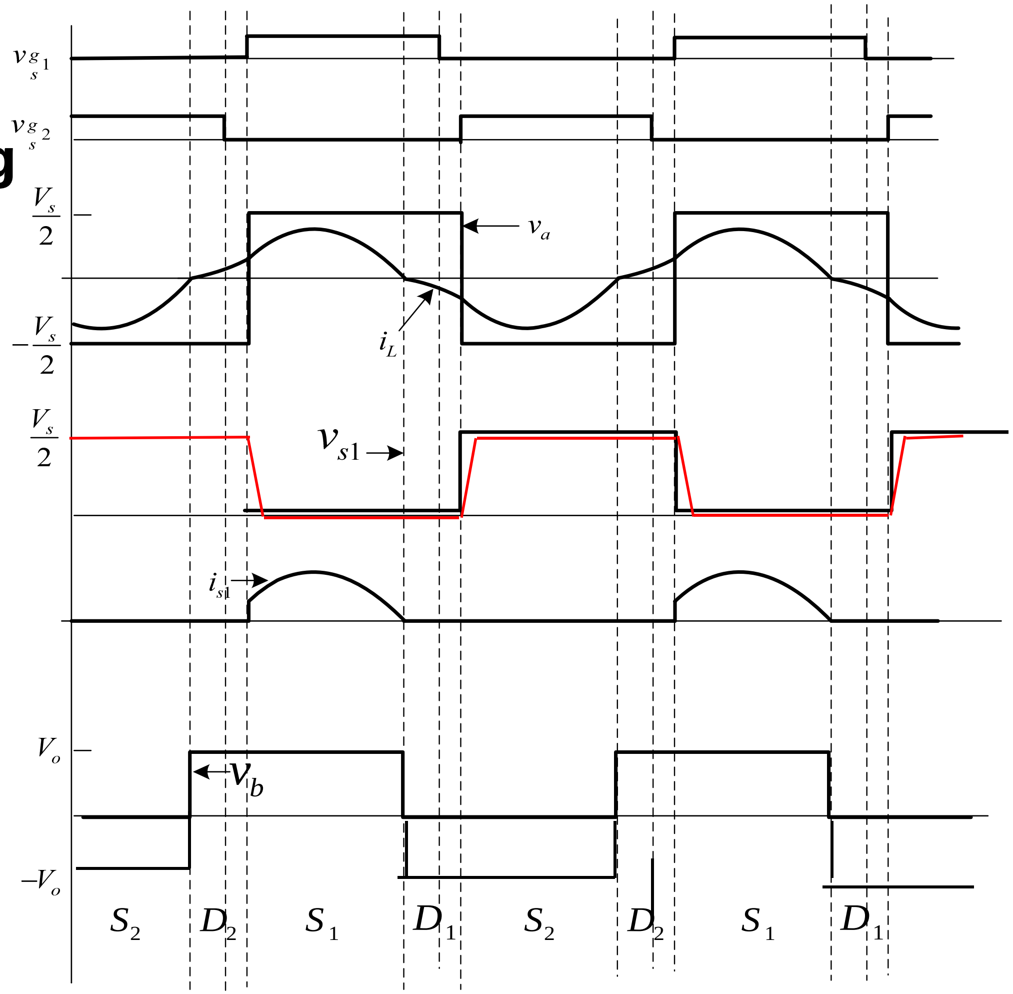
Output Vo can be controlled by changing switching frequency fs

Capacitive operation

$\frac{f_o}{2} < f_s < f_o$

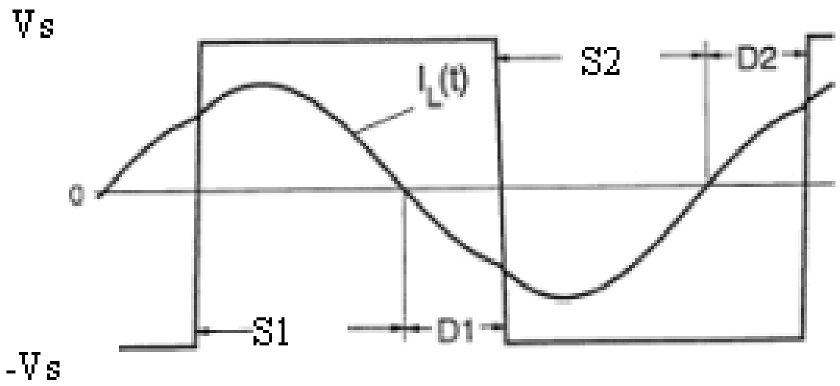
- Resonant current is leading
- S1 and S2: ZCS switching off
- Suited to thyristor converter

- Larger turn-on loss:
- Body diode reverse recovery
- There is larger distortion in resonant current



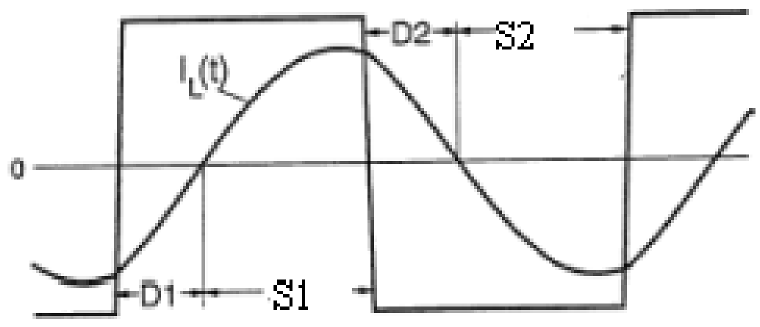
零电流关断与零电压开通（ZCS and ZVS switching）

Zero Current Switching



$f_s<f_0$, **Capacitive load**

Zero Voltage Switching

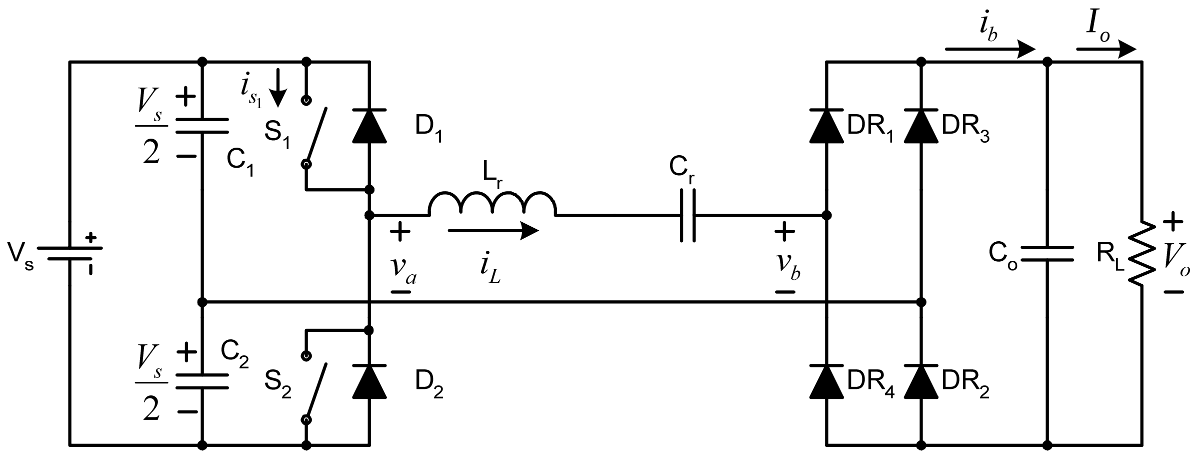


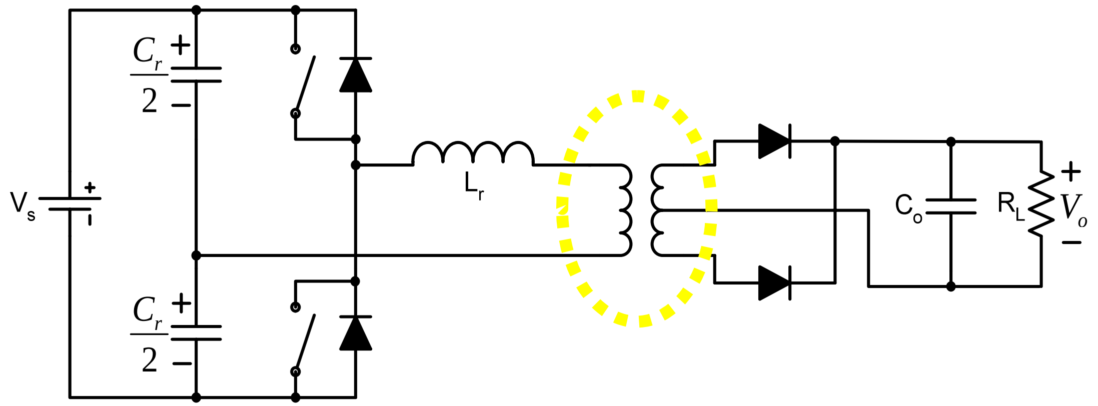
$f_s>f_0$, **Inductive load**

感性方式的优势（Advantages of inductive mode)

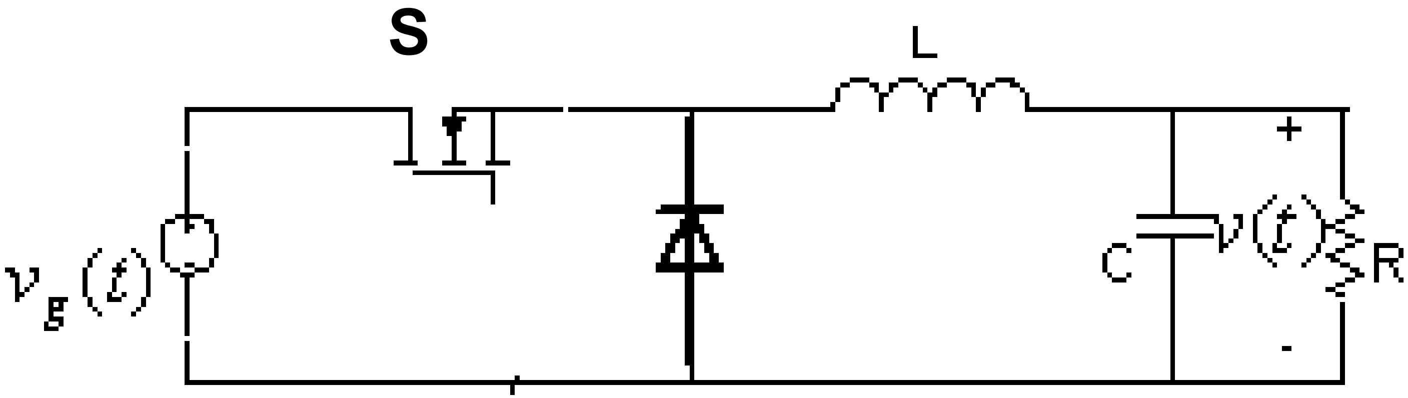
- **No turn-on loss in the power switches due to ZVS turn-on**
- **Lossless snubber during turn-off due to ZVS turn-off**
- **High speed anti-parallel diodes are not necessary, body diode of MOSFETs are ok**
- **Smaller transformer due to higher frequency operation**
- **Smaller output filter**

Topology variations



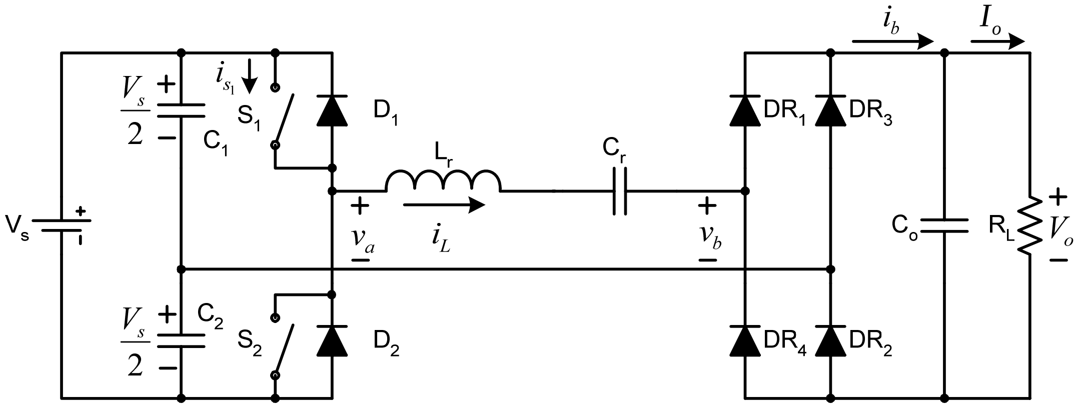


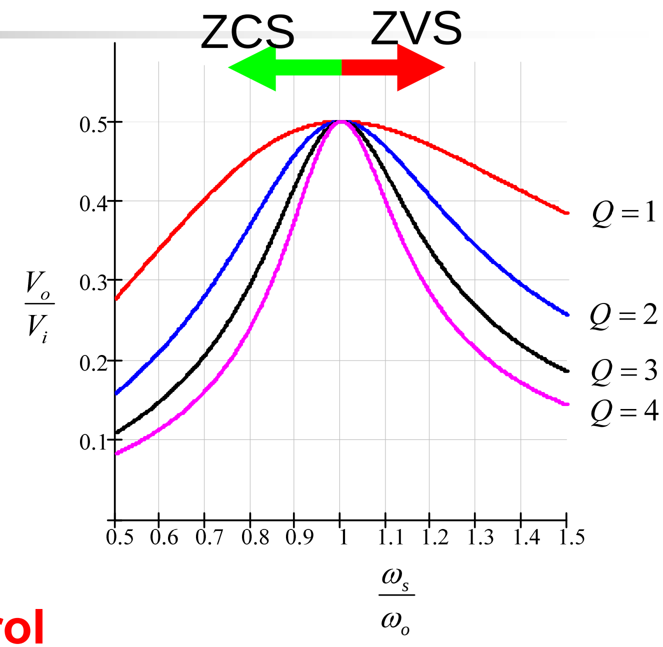
Zero Current quasi resonant converter



ZCS: How can the current through the switch naturally decrease to zero ?

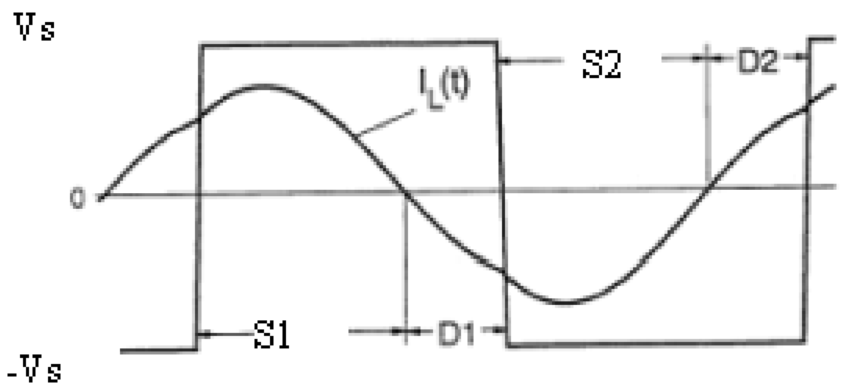
Resonant switching concept



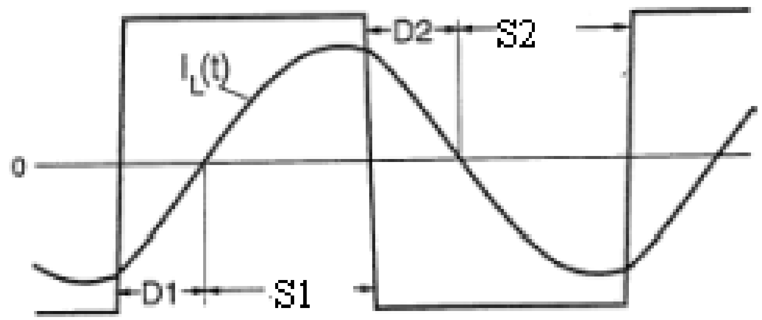


Switch frequency control

Zero Current Switching

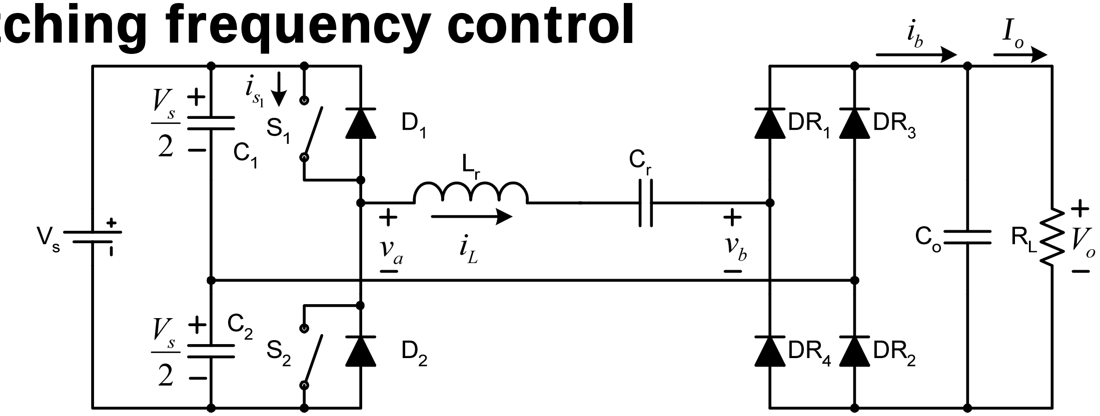


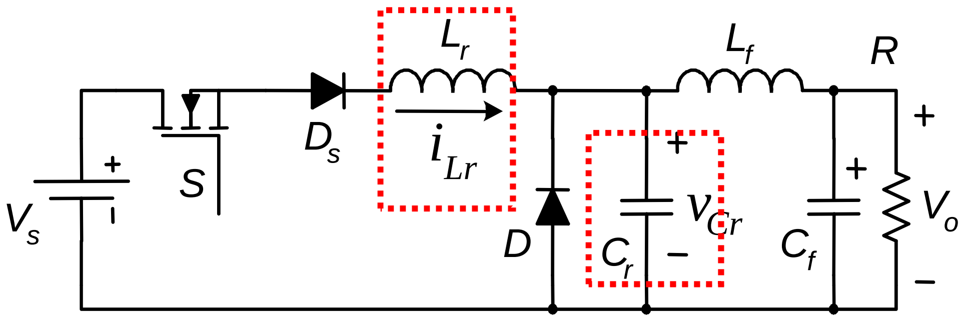
Zero Voltage Switching



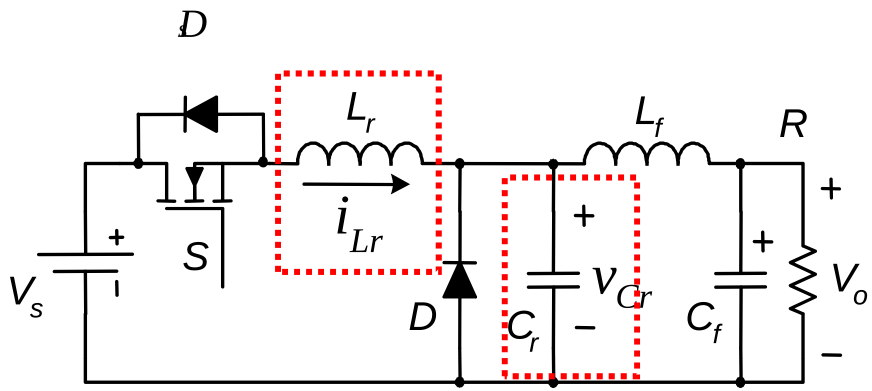
Introduce resonant switching concept to DC/DC converters

- **There is a LC resonant circuit, and the current is able to resonance to zero**
- **Switching frequency control**



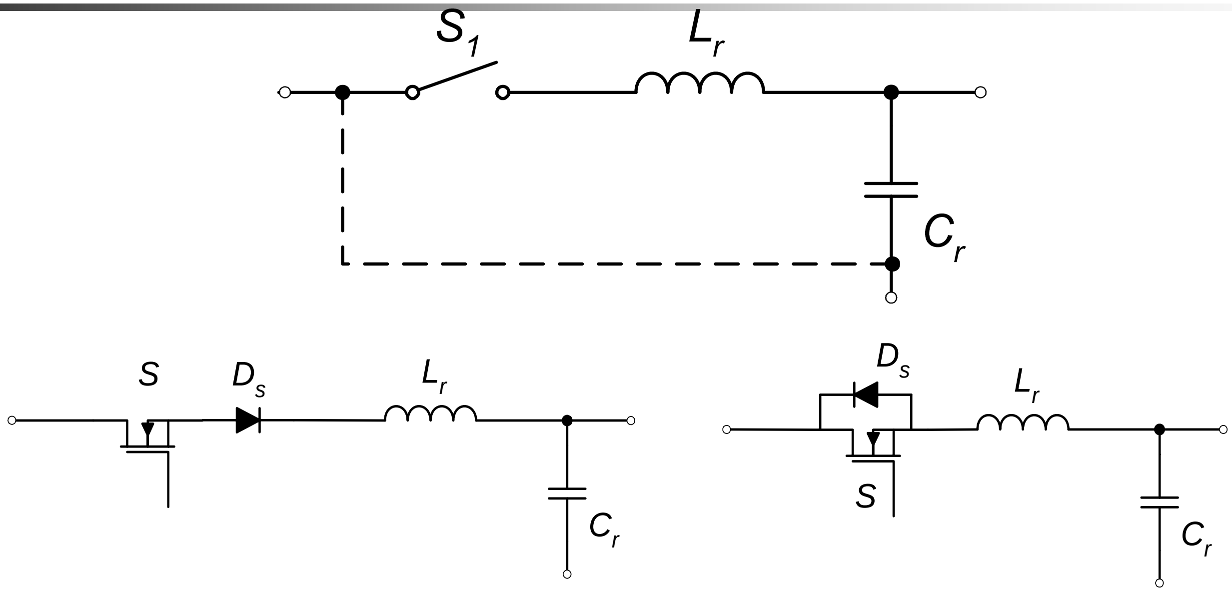


（a）半波模式



（b）全波模式

ZCS resonant switch

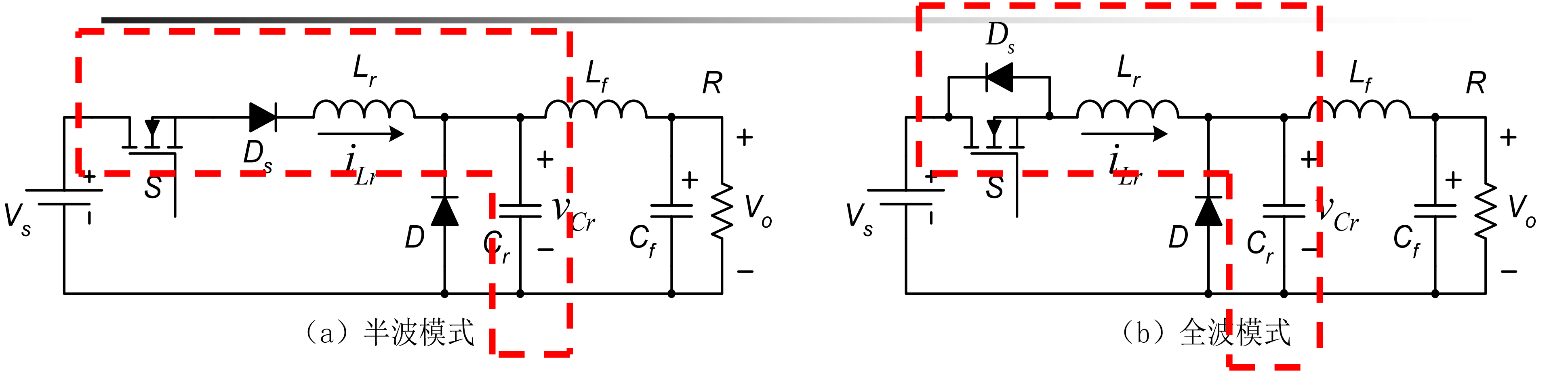


(a) 半波模式　　(b) 全波模式

Half wave: Resonant inductor current is one directional

Full wave: Resonant inductor current is bi-directional

ZCS quasi-resonant Buck converter



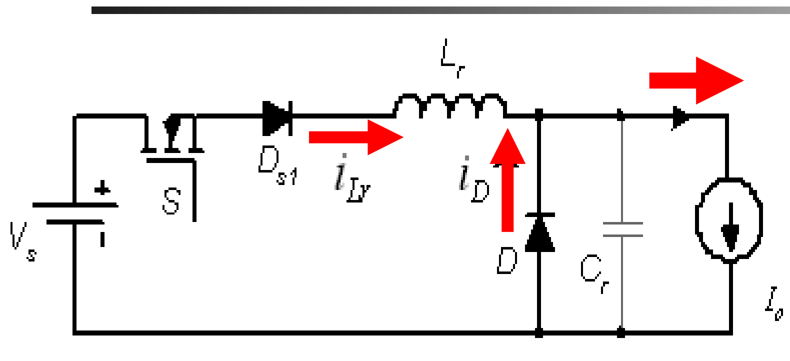
Half wave

Full wave

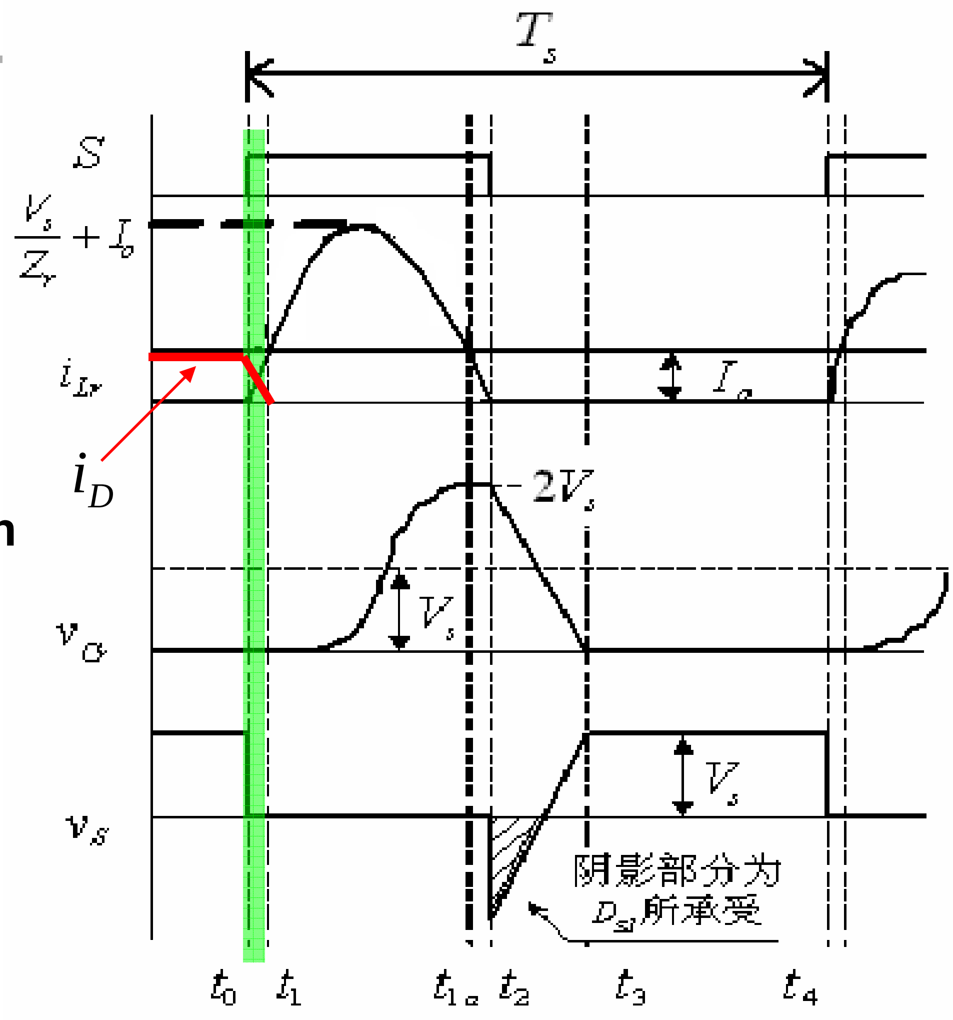
Assumption:

- All switches and diodes are ideal
- L and C are ideal
- Lf is larger enough and its current to be seen as current source

Stage 1:inductor charging (t0,t1)



（a）$[t_0, t_1]$电感充磁阶段



（a）半波模式

Current in diode is transfer to the switch

$$i_{Lr}(t_0) = 0$$

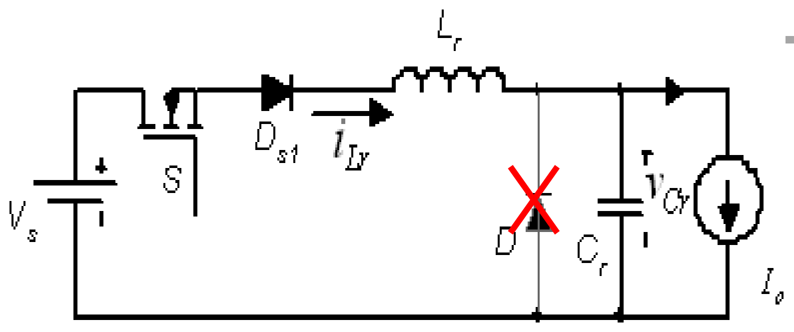
$$i_{Lr}(t) = \frac{1}{L_r}\int_0^t V_s dt = \frac{V_s}{L_r}t$$

Duration:

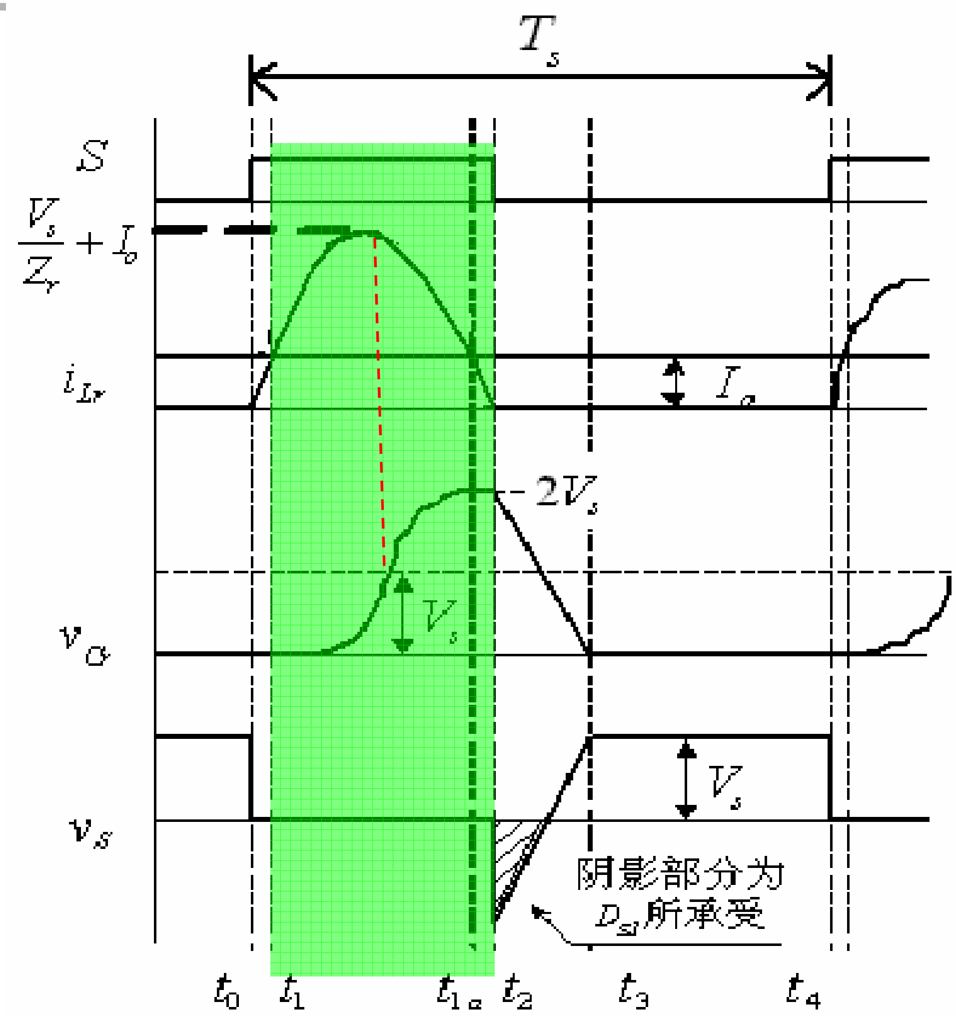
$$T_1 = t_1 - t_0 = \frac{L_r I_o}{V_s}$$

Stage 1 ends when i_D reduced to zero

Stage 2:resonant stage (t1,t2)



（b）$[t_1, t_2]$谐振阶段



（a）半波模式

Lr and Cr is in resonance

$$\begin{cases} C_r \dfrac{dv_{Cr}}{dt} = i_{Lr} - I_o & \textbf{KCL law} \\ L_r \dfrac{di_{Lr}}{dt} = V_s - v_{Cr} & \textbf{KVL law} \end{cases}$$

$$i_{Lr}(t) = I_o + \frac{V_s}{Z_r}\sin\omega_r(t - t_1)$$

$$v_{Cr}(t) = V_s[1 - \cos\omega_r(t - t_1)]$$

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \qquad Z_r = \sqrt{\frac{L_r}{C_r}}$$

Stage 2:resonant stage (cont'd)

$$\omega_r(t-t_1)=\frac{\pi}{2}$$

Resonant inductor peak current $i_{Lr\max}=i_{Lr}[\omega_r(t-t_1)=\frac{\pi}{2}]=\frac{V_s}{Z_r}+I_o$

Resonant cap voltage $v_{Cr}[\omega_r(t-t_1)=\frac{\pi}{2}]=V_s$

$$\omega_r(t-t_1)=\pi$$

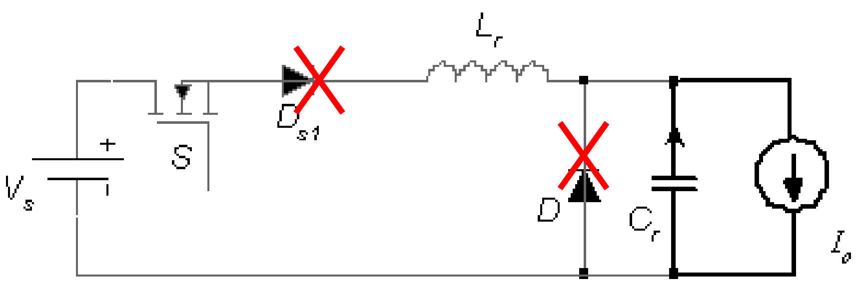
Resonant cap peak voltage: $v_{Cr\max}=v_{Cr}[\omega_r(t-t_1)=\pi]=2V_s$

Resonant inductor current $i_{Lr}[\omega_r(t-t_1)=\pi]=I_o$

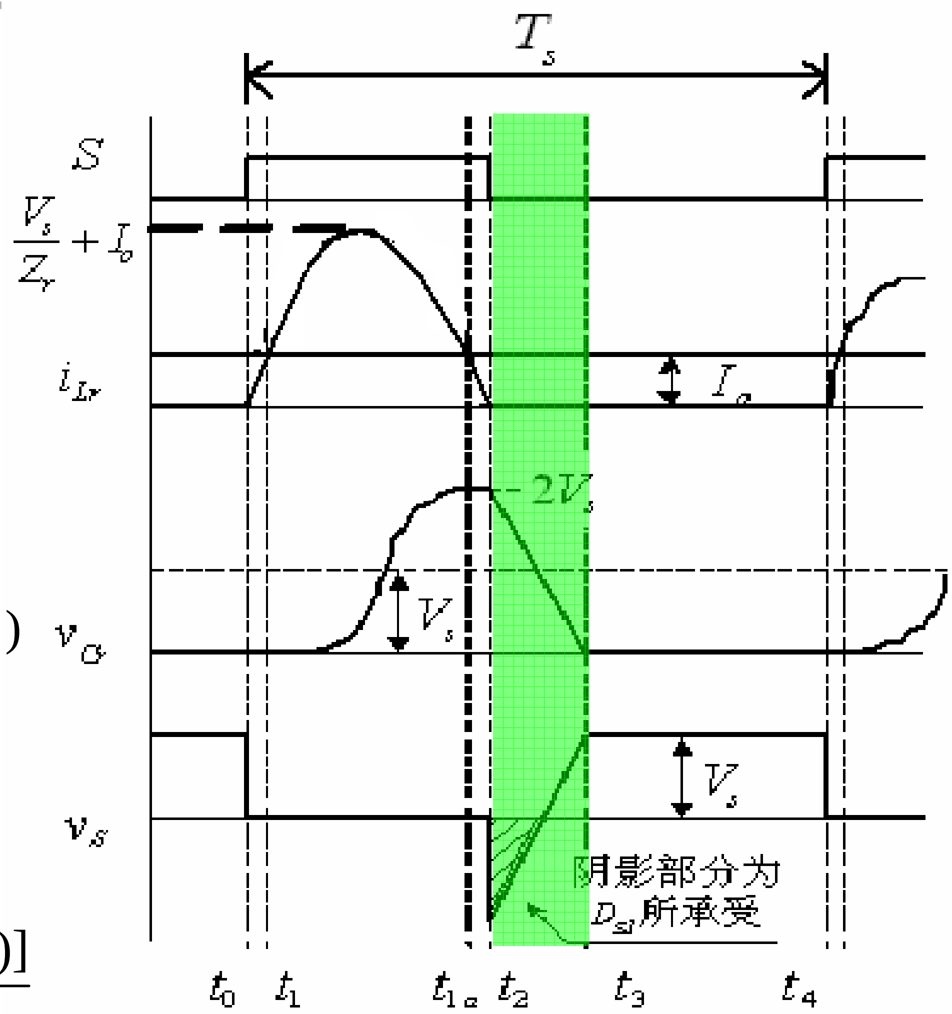
At time t2, switch naturally turns off when switch current resonant to *0* ZCS is realized

Stage 2 ends when S is turned off with ZCS

Stage 3: capacitor discharge (t2,t3)



（c）$[t_2, t_3]$电容放电阶段



（a）半波模式

Cap. voltage linearly is decreasing

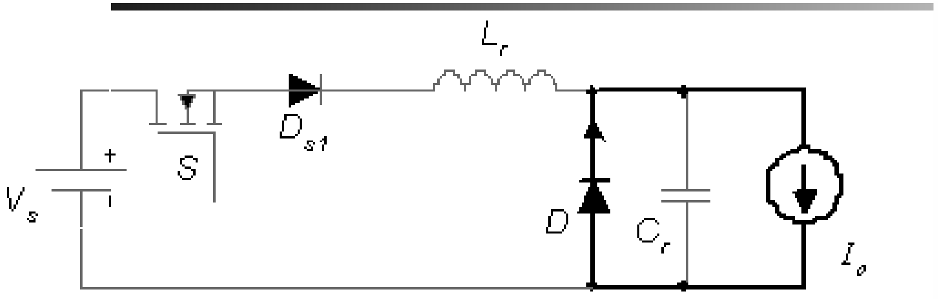
$$v_{Cr}(t)=\frac{1}{C_r}\int_{t_2}^{t}(-I_o)dt+V_{Cr}(t_2)=V_{Cr}(t_2)-\frac{I_o}{C_r}(t-t_2)$$

Duration:

$$T_3=t_3-t_2=\frac{C_rV_{Cr}(t_2)}{I_o}=\frac{C_rV_s[1-\cos\omega_r(t_2-t_1)]}{I_o}$$

Stage 3 ends when *D* starts to conduct

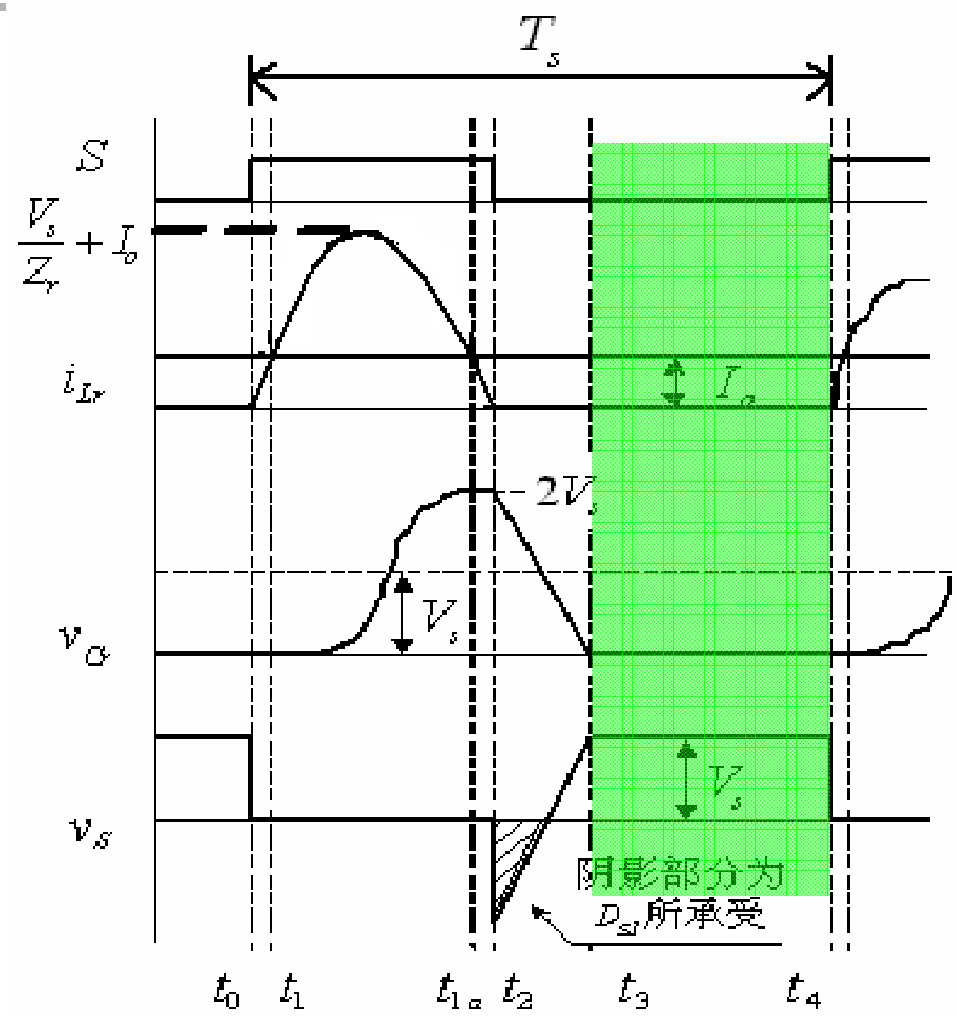
Stage 4: freewheel (t3,t4)



（d）$[t_3,t_4]$续流阶段

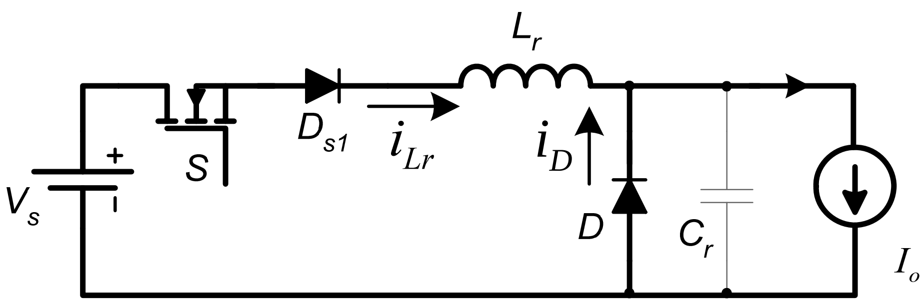
$$T_4 = t_4 - t_3 = T_s - (T_1 + T_2 + T_3)$$

Duration is decided by switching frequency

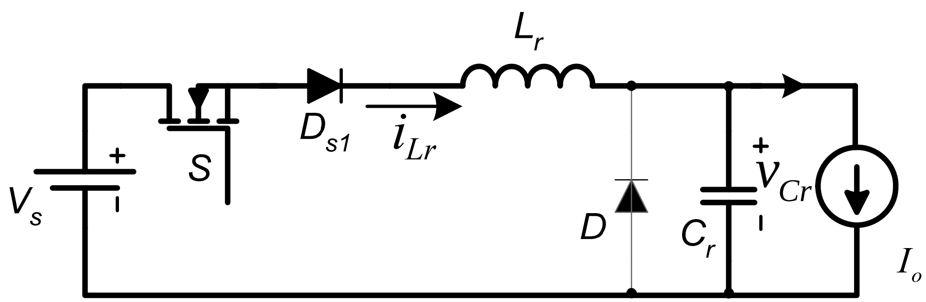


（a）半波模式

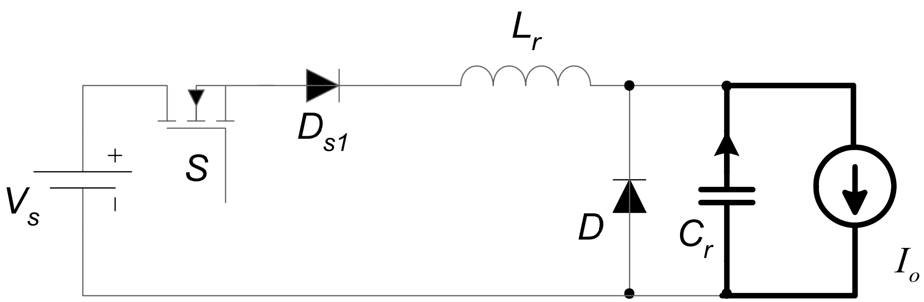
Summary of the half-wave operation



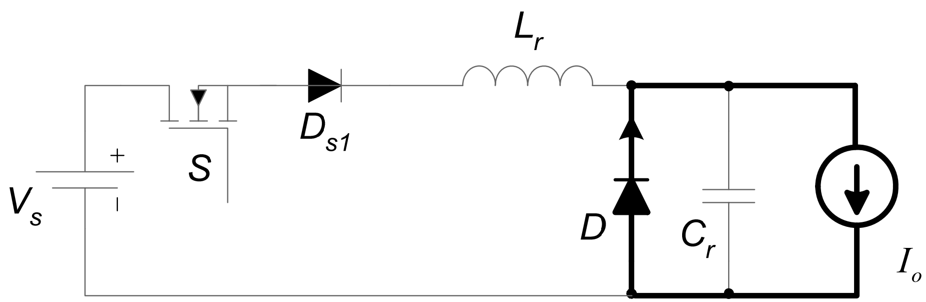
（a） Inductor charging



（b） [resonance

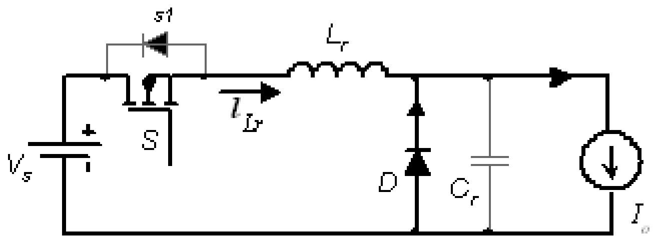


（c） Cap discharging

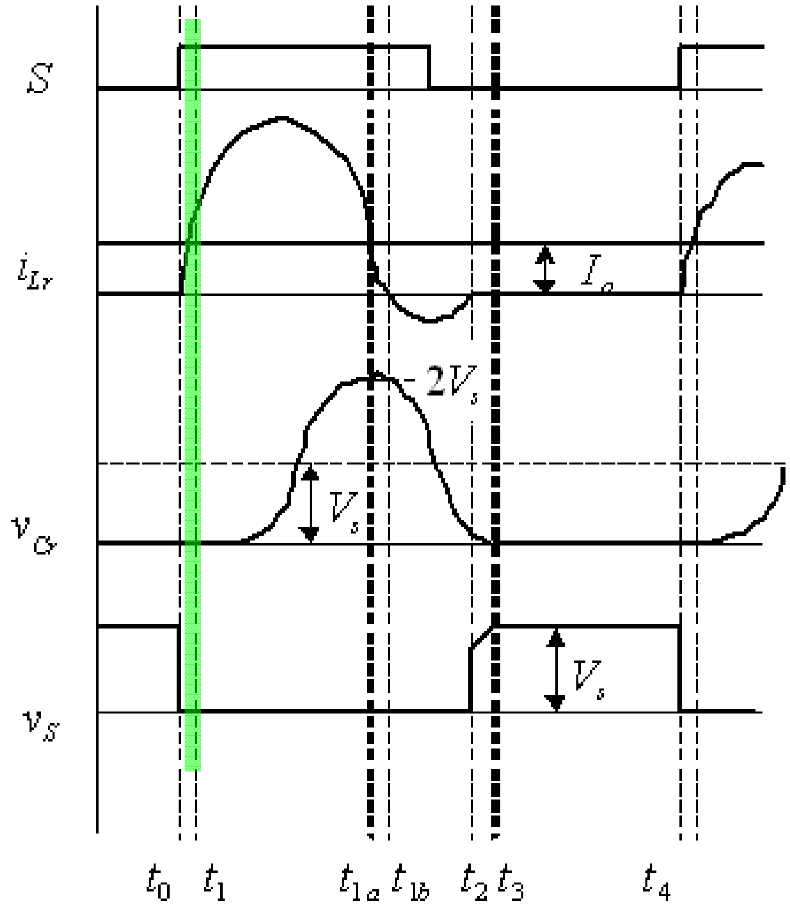


（d） Flywheel

Full wave mode:
Stage 1:inductor charge

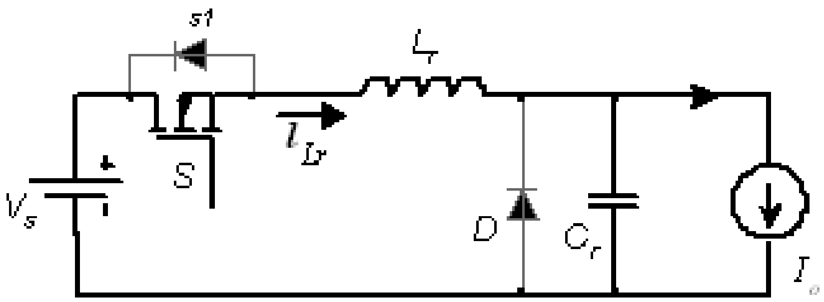


（a）[t_0，t_1]电感充磁阶段

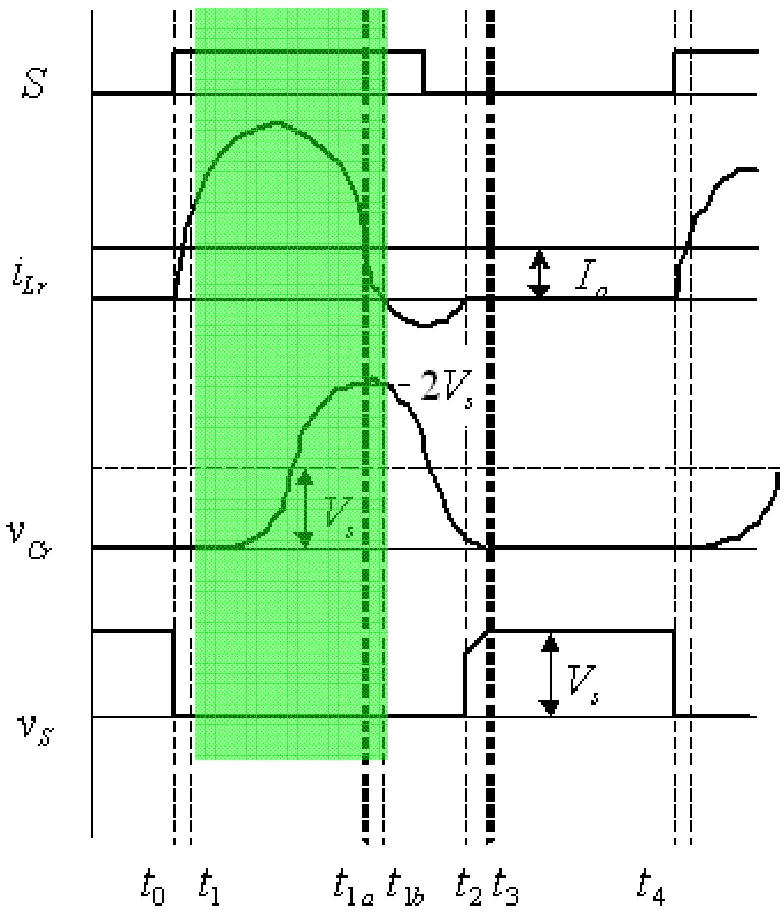


（b）全波模式

Full wave mode:
Stage 2(section 1):resonance

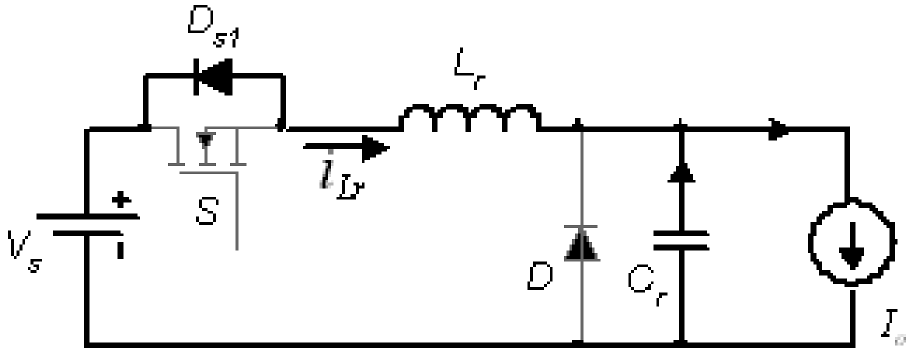


（b）[t_1，t_{1a}]谐振阶段之一



（b）全波模式

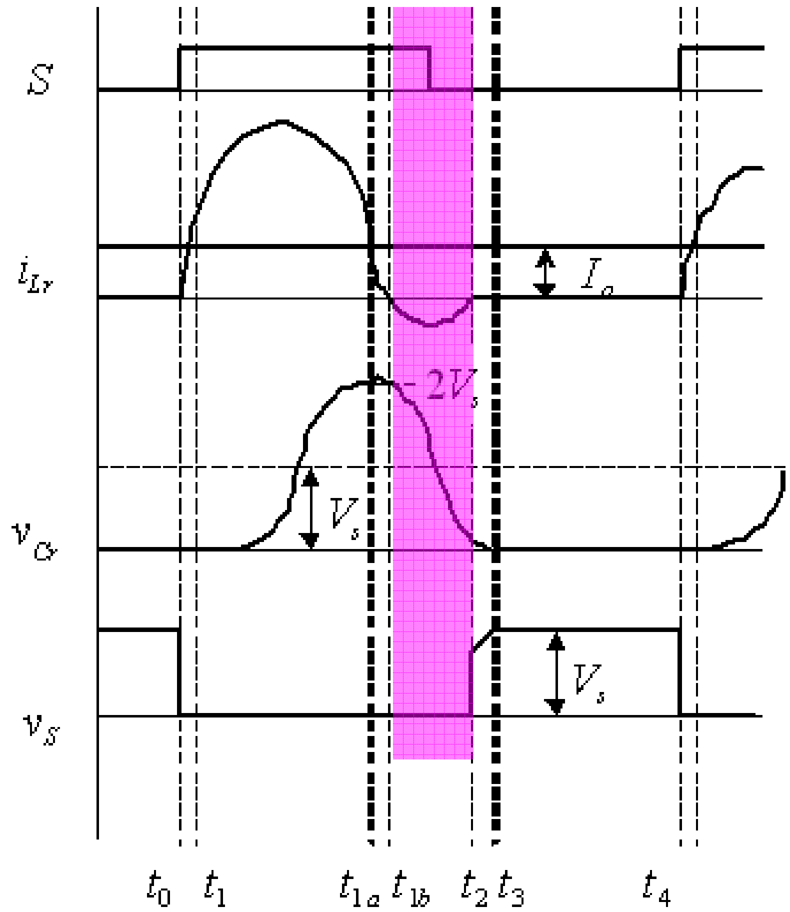
Full wave mode:
Stage 2(section 2):resonance



（b'） [t_{1b}，t_2]谐振阶段之二

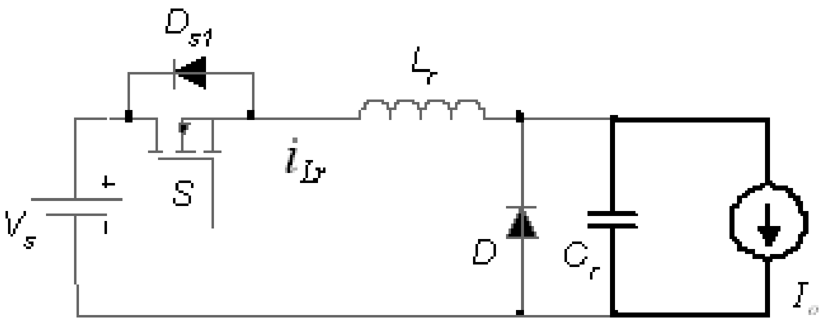
At time t_{1b} i_{Lr} is reversed and resonant through negative half cycle

During [t_{1b},t_2], switch S current is zero
It can be turned off with ZCS.

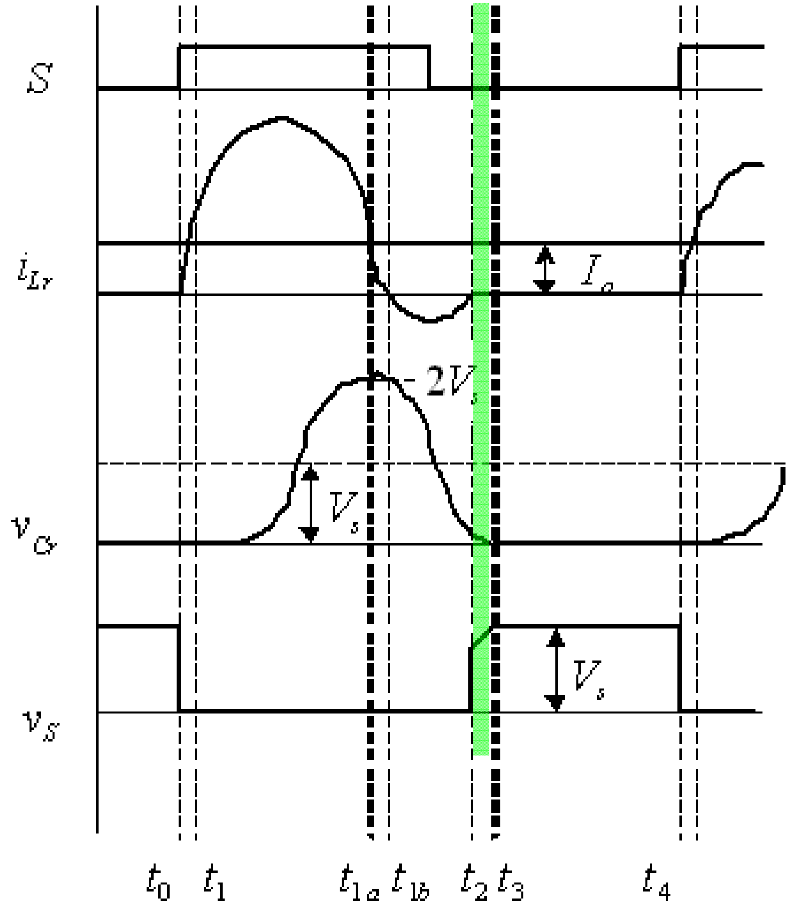


（b）全波模式

Full wave mode:
Stage 3: capacitor discharge

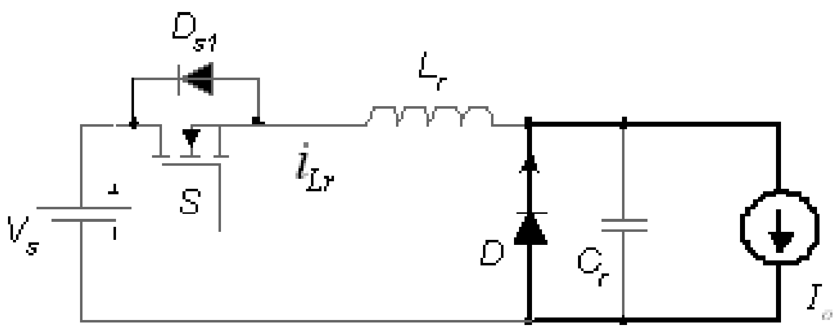


（c）［t_2，t_3］电容放电阶段

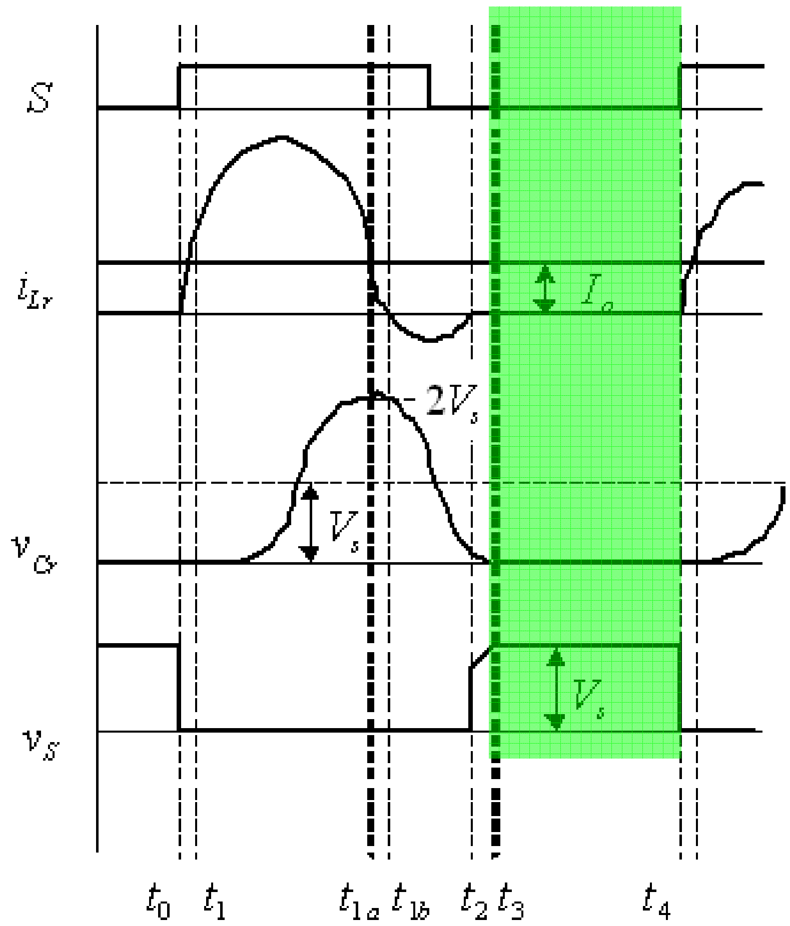


（b）全波模式

Full wave mode:
Stage 4: freewheel

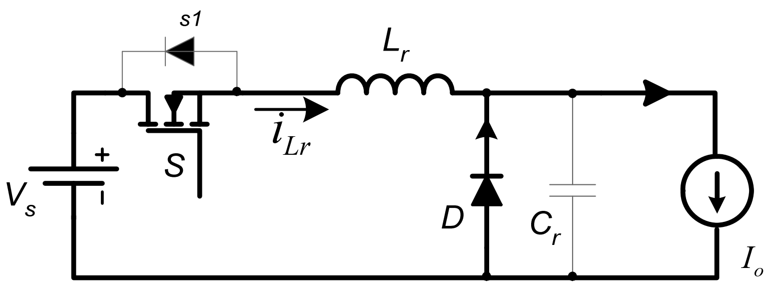


（d）[t_3，t_4]续流阶段

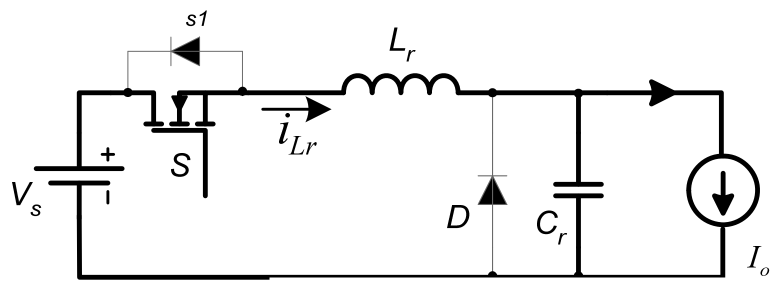


（b）全波模式

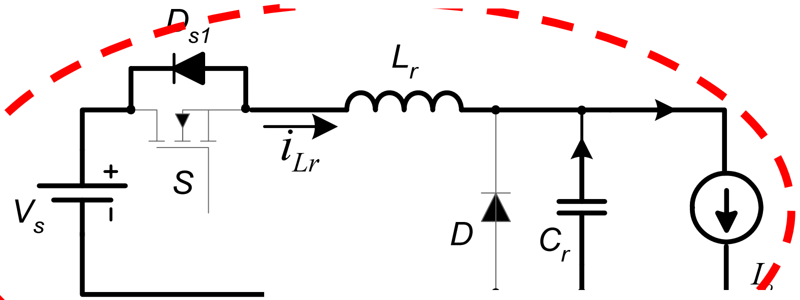
Full-wave operation stages



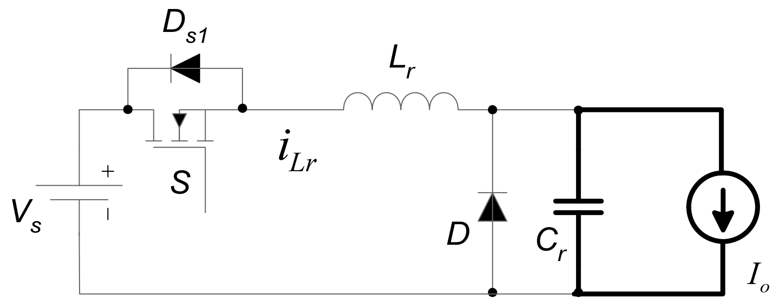
(a) Inductor charging



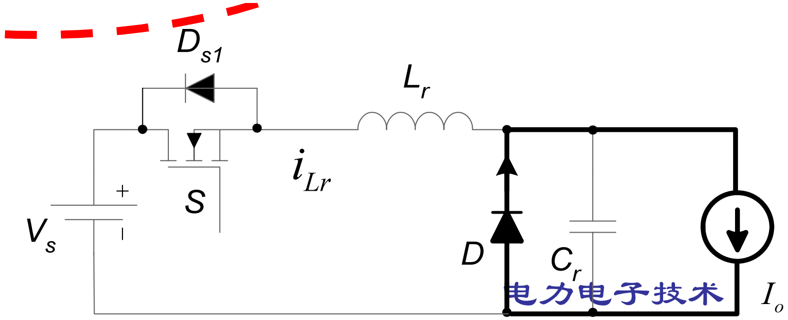
(b) Resonance duration 1



(b') Resonance duration 2



(c) Cap discharging



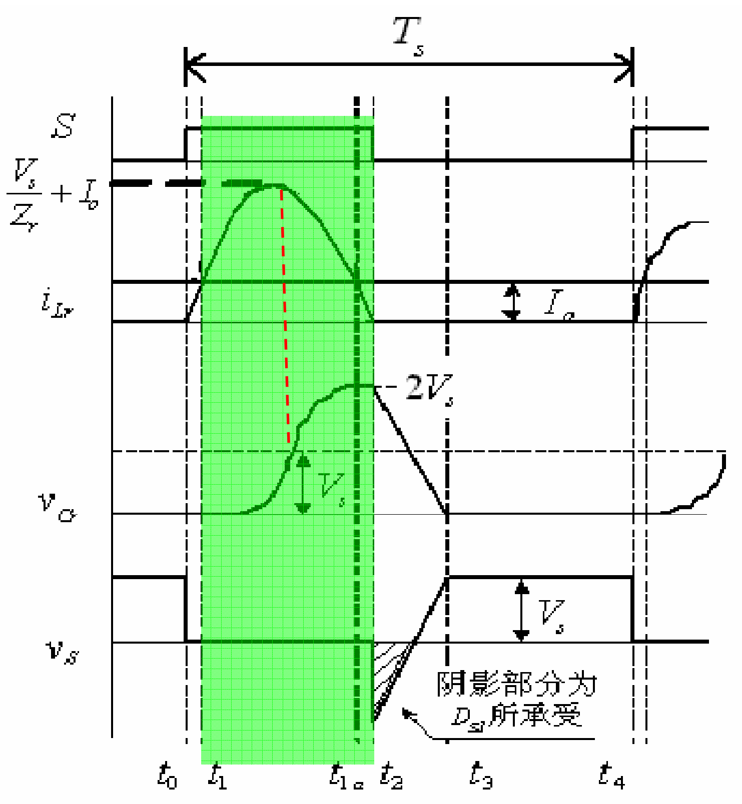
Flywheel

ZCS condition

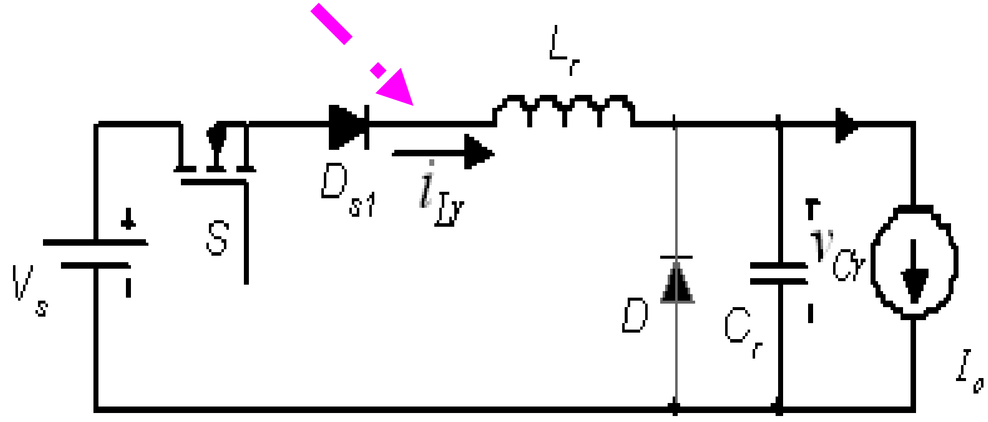
In stage 2, Inductor current must resonance to zero to realize ZCS.

$$i_{Lr}(t) = I_o + \frac{V_s}{Z_r}\sin\omega_r(t - t_1) \quad \Rightarrow \quad \frac{V_s}{Z_r} > I_{o\max}$$

$I_{o\max}$ Maximum load current



（a）半波模式



（b）[t_1, t_2]谐振阶段

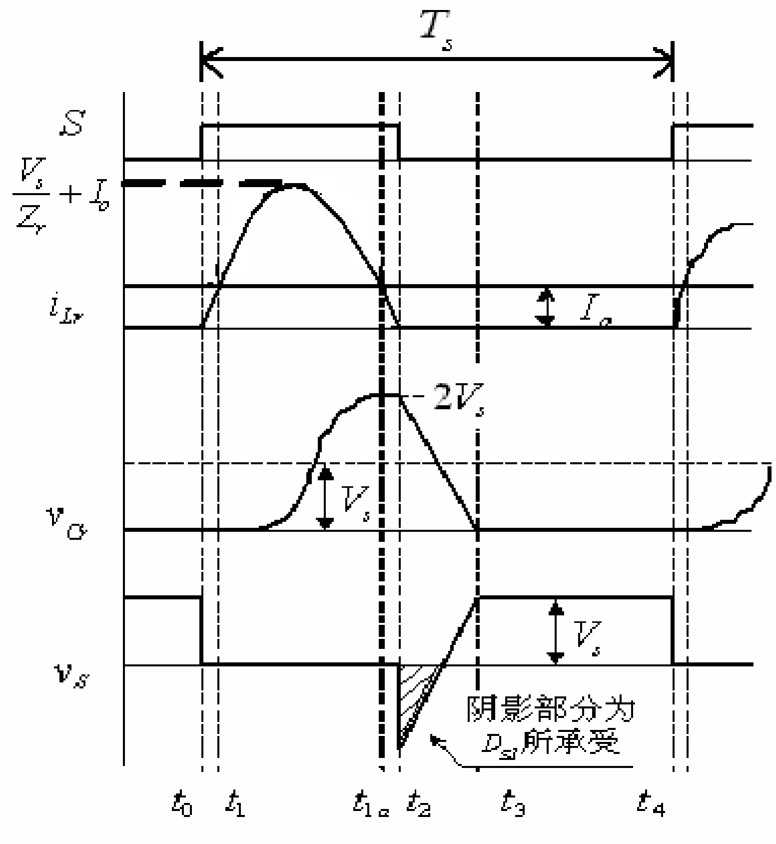
DC conversion ratio

Energy drawn from the DC source in every switching cycle:

$$W_s = V_s \int_0^T i_{Lr}(t)dt$$

Energy output to the load

$$W_o = V_o I_o T_s = \frac{V_o I_o}{f_s}$$



（a）半波模式

$$\int_0^T i_{Lr}(t)dt = \int_0^{t_1} \frac{V_s t}{L_r}dt + \int_{t_1}^{t_2} [I_o + \frac{V_s}{Z_o}\sin\omega_r(t-t_1)]dt$$

$$= \frac{I_o}{2}t_1 + I_o(t_2 - t_1) + V_s C_r[1-\cos(\omega_r(t_2 - t_1))]$$

DC conversion ratio

According to energy conservation law $W_s = W_o$

$$V_o = V_s f_s \left\{ \frac{t_1}{2} + (t_2 - t_1) + \frac{C_r V_s}{I_o} [1 - \cos\omega_r (t_2 - t_1)] \right\}$$

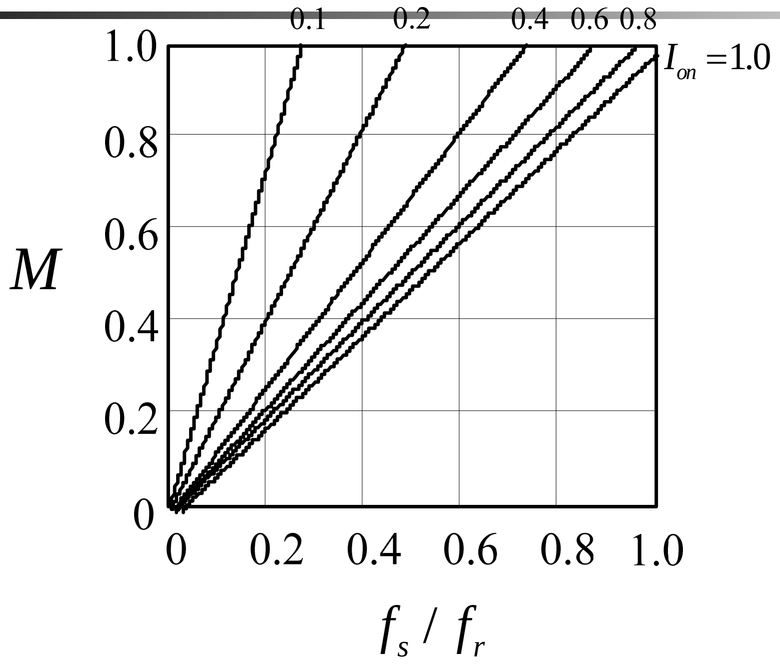
$$V_o = V_s f_s [\frac{t_1}{2} + (t_2 - t_1) + (t_3 - t_2)]$$

DC conversion ratio $M = \frac{V_o}{V_s} = \frac{f_s}{f_r} f(I_{on})$ where $I_{on} = \frac{Z_r I_o}{V_s}$

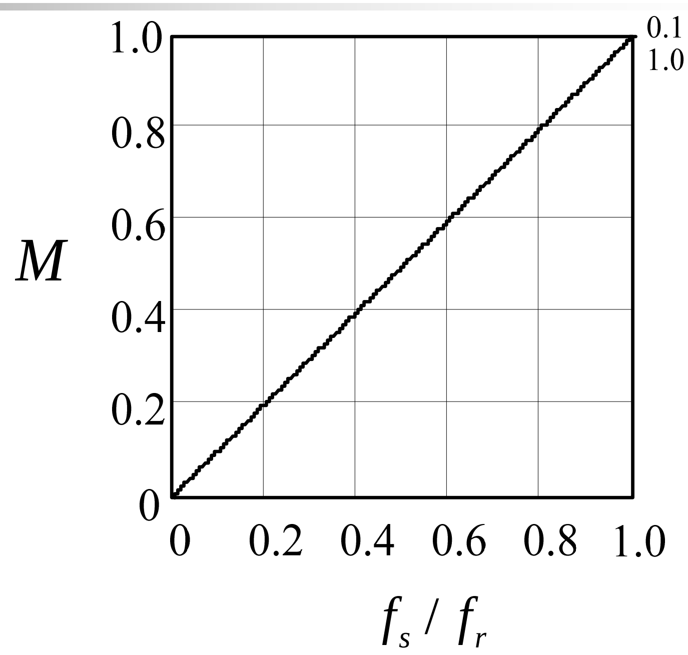
Half-wave: $f(I_{on}) = \frac{1}{2\pi}[\frac{1}{2} I_{on} + \pi + \sin^{-1}(I_{on}) + \frac{1}{I_{on}}(1 + sign\sqrt{1 - I_{on}^2})]$

Full-wave: $f(I_{on}) = \frac{1}{2\pi}[\frac{1}{2} I_{on} + 2\pi - \sin^{-1}(I_{on}) + \frac{1}{I_{on}}(1 - sign\sqrt{1 - I_{on}^2})]$

Conversion ratio curves



Half wave



Full wave

Half: $$f(I_{on}) = \frac{1}{2\pi}[\frac{1}{2}I_{on} + \pi + \sin^{-1}(I_{on}) + \frac{1}{I_{on}}(1 + sign\sqrt{1 - I_{on}^2})]$$

Full: $$f(I_{on}) = \frac{1}{2\pi}[\frac{1}{2}I_{on} + 2\pi - \sin^{-1}(I_{on}) + \frac{1}{I_{on}}(1 - sign\sqrt{1 - I_{on}^2})]$$

Summary of the ZCS QRC converter

•Current Resonant switch :full wave and half wave

•ZCS is realized for the switch

•ZCS condition is derived. The lighter the load, the better the ZCS condition

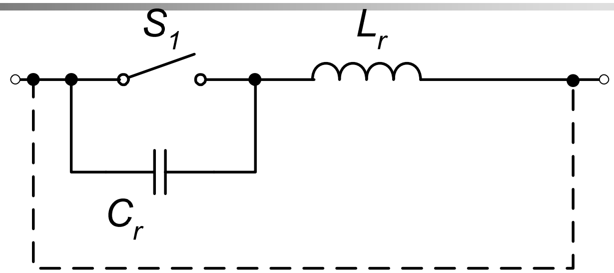
•DC conversion ratio is the function of switching frequency

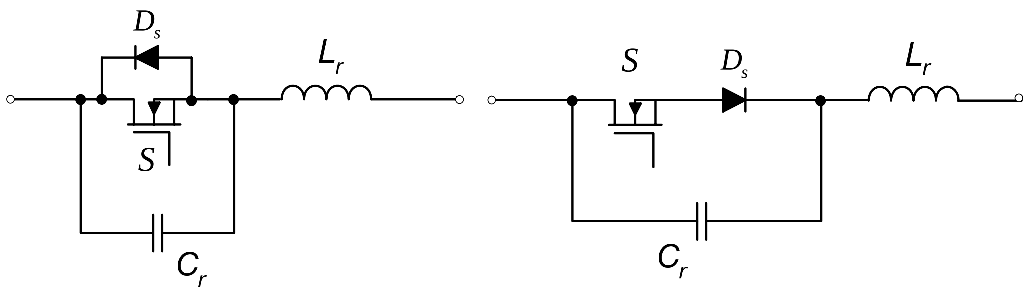
•DC conversion ratio: linear for full wave, and nonlinear for half wave

•The concept can be extended to all DC/DC converters

Zero Voltage quasi resonant converter

ZVS resonant switch





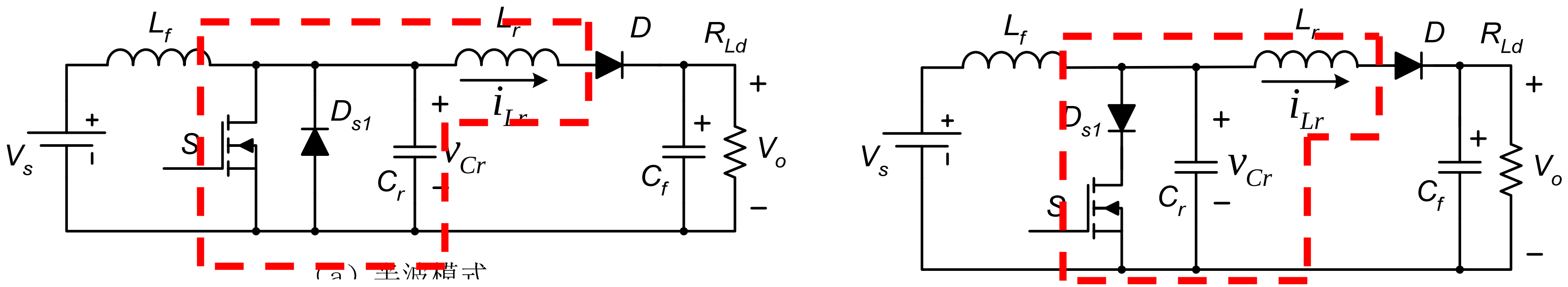
(a) 半波模式　　(b) 全波模式

Half wave:Resonant capacitor voltage is one directional

Full wave:Resonant capacitor voltage is bi-directional

Extra diode is inserted in full wave. Conduction loss increased.

Quasi ZVS Boost converter



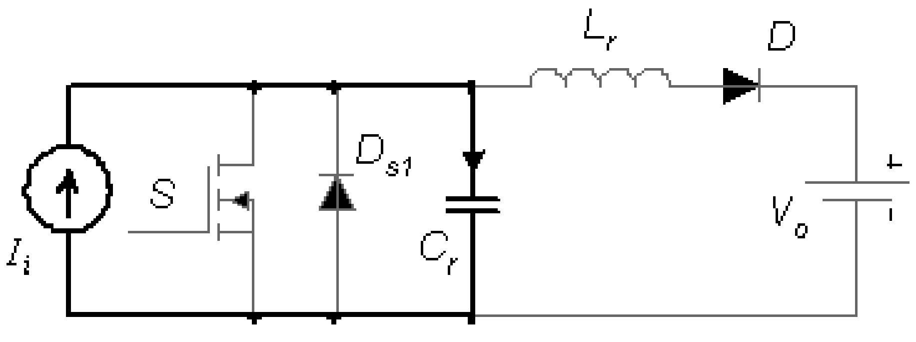
Half wave

Full wave

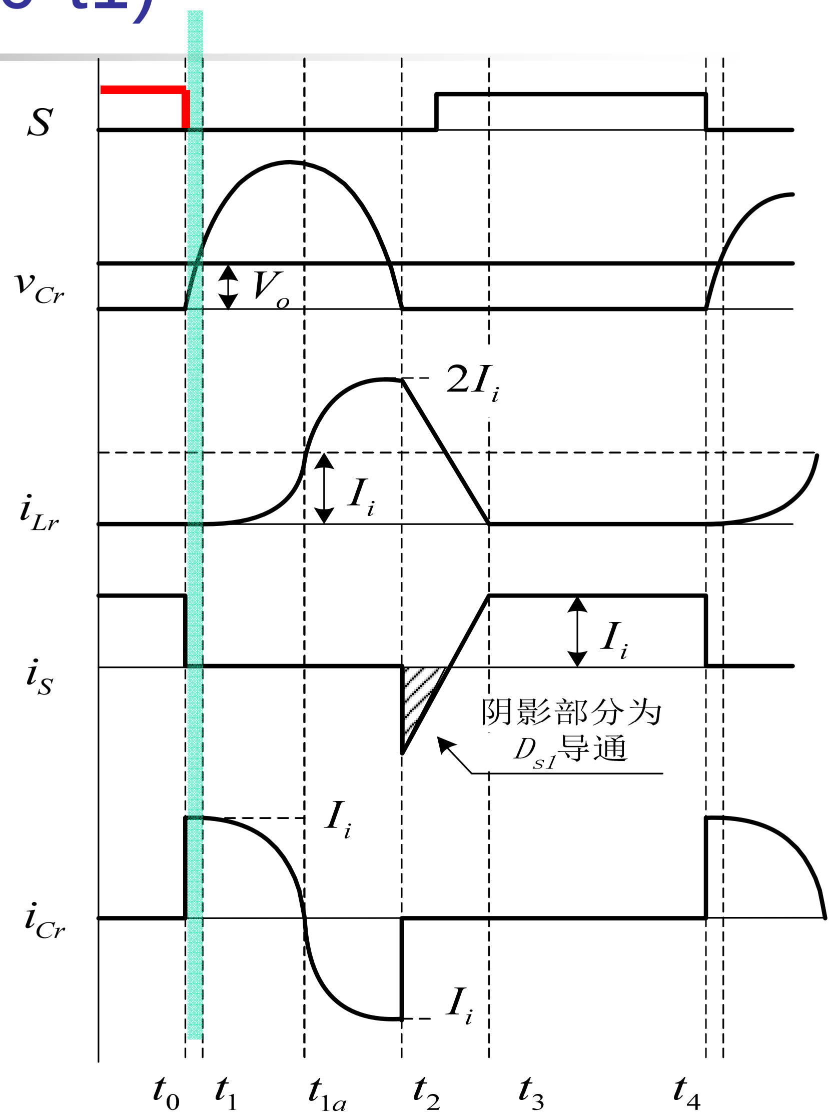
Assumption:

- All switches and diodes are ideal
- *L* and *C* are ideal
- *Lf* is larger enough and its current to be seen as the current source
- *Cf* is larger enough and can be seen as voltage sink

Stage 1:Capacitor Charge (t0-t1)



(a) 阶段1(t_0, t_1)电容充电阶段



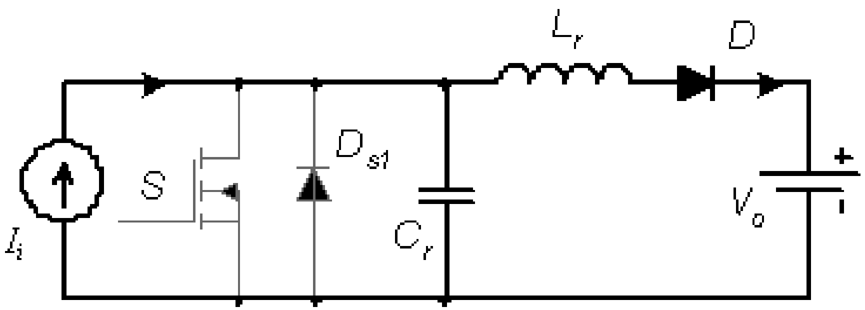
Voltage on resonant capacitor

$$v_{Cr}(t) = \frac{1}{C_r}\int_0^t I_i dt = \frac{I_i}{C_r} t$$

Duration: $$T_1 = t_1 - t_0 = \frac{C_r V_o}{I_i}$$

Stage 1 ends when resonant Cap. Voltage equal to *Vo*

Stage 2:Resonance (t1-t2)



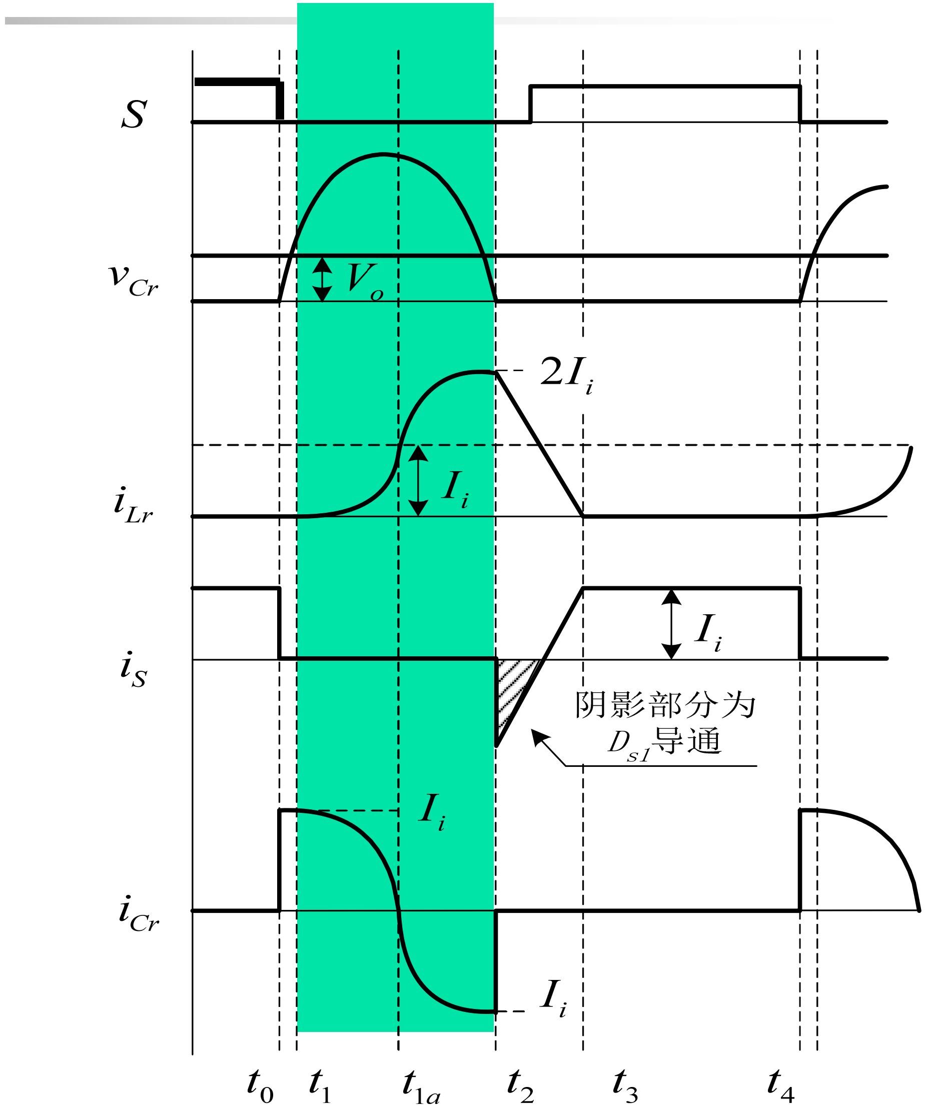
（b）阶段2（t_1，t_2）谐振阶段

$$\begin{cases} L_r \dfrac{di_{Lr}}{dt} = v_{Cr} - V_o & \textbf{KVL law} \\ C_r \dfrac{dv_{Cr}}{dt} = I_i - i_{Lr} & \textbf{KCL law} \end{cases}$$

$$i_{Lr}(t) = I_i[1 - \cos\omega_r(t - t_1)]$$

$$v_{Cr}(t) = V_o + I_i Z_r \sin\omega_r(t - t_1)$$

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \qquad Z_r = \sqrt{\frac{L_r}{C_r}}$$



Stage 2:Resonance (cont'd)

$$\omega_r(t_{1a}-t_1)=\frac{\pi}{2}$$

Cap peak voltage $V_{Cr\max}=V_o+I_iZ_r$

$$i_{Lr}(t_{1a})=I_i$$

$$\omega_r(t-t_1)=\pi$$

Cap voltage resonant to *Vo*

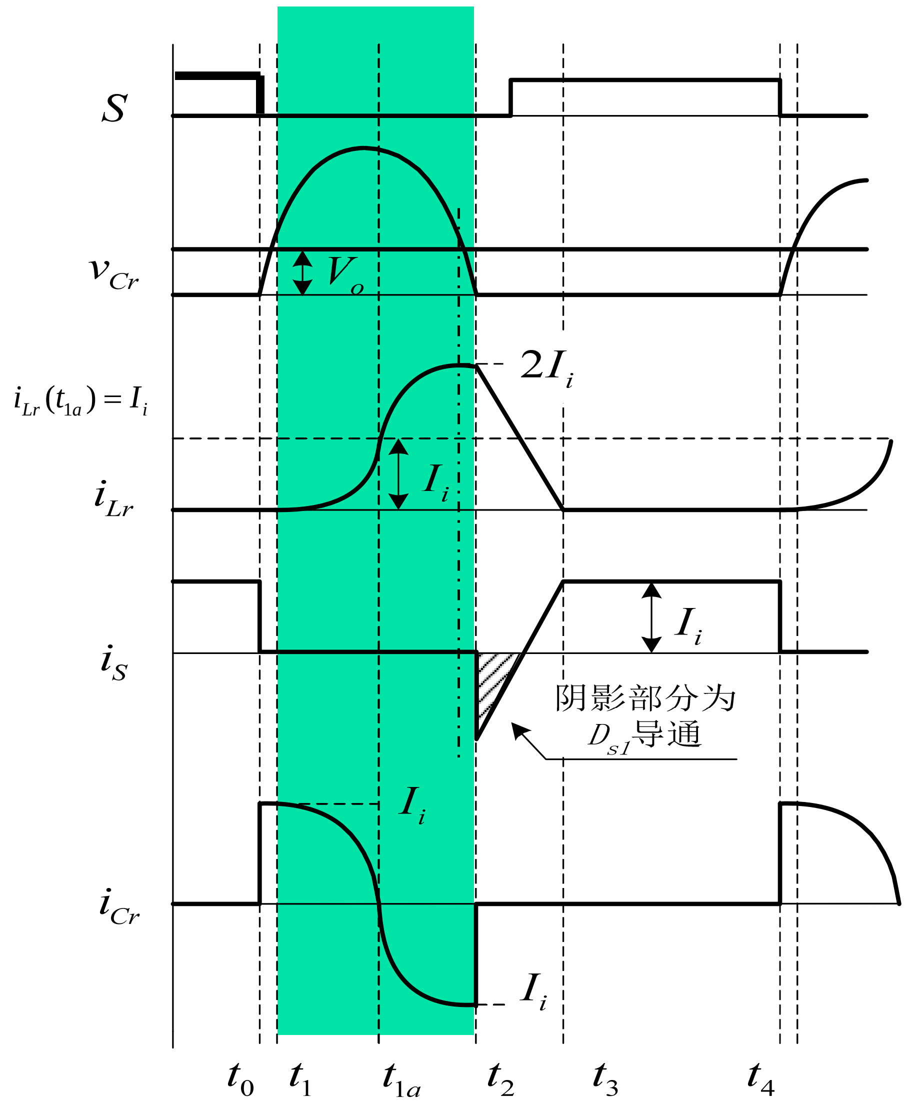
Ind. Current resonant to ***2Ii***

Duration:

$$T_2=t_2-t_1=\frac{1}{\omega_r}[\pi+\sin^{-1}(\frac{V_o}{I_iZ_r})]=\frac{\theta}{\omega_r}$$

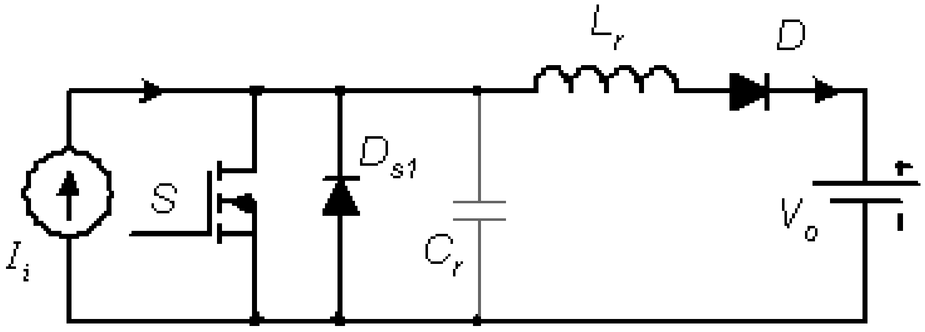
$$\pi<\theta<\frac{3}{2}\pi$$

$$I_{Lr2}=i_{L_r}(t_2)=I_i[1-\cos\omega_r(t_2-t_1)]=I_i[1+\sqrt{1-(\frac{V_o}{I_iZ_r})^2}]$$

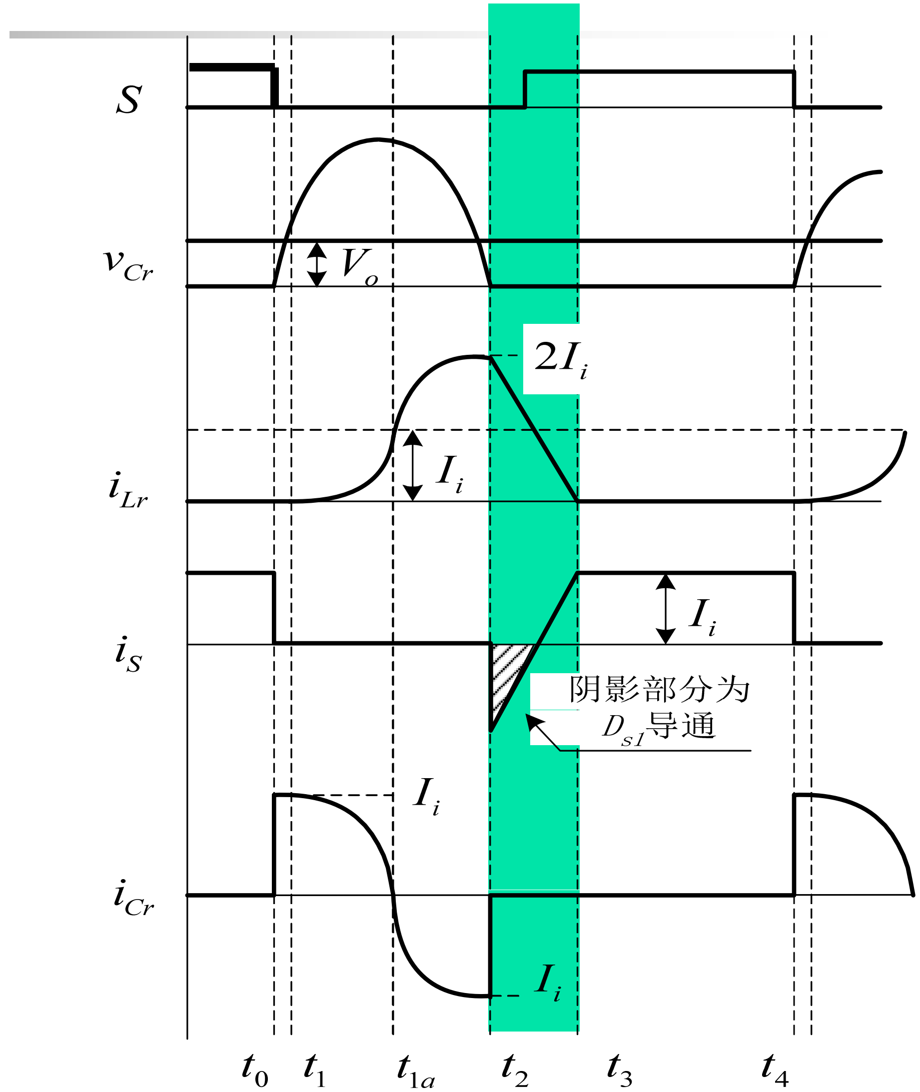


Stage 2 ends when cap. voltage resonant to zero

Stage 3: Inductor discharge (t2-t3)



(c) 阶段3(t_2, t_3)电感放磁阶段



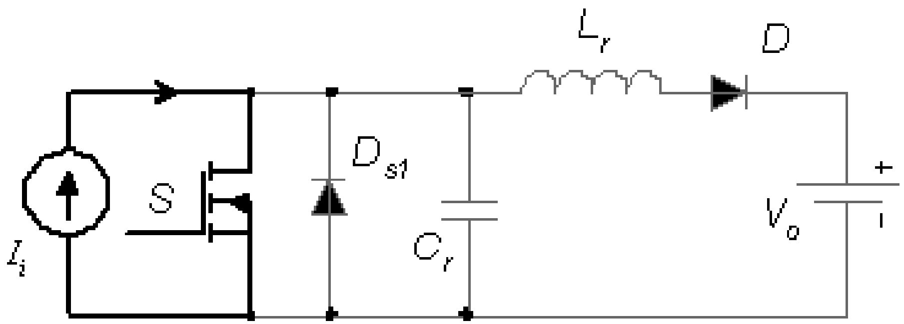
Inductor current is linearly decreasing

$$i_{Lr}(t) = I_{Lr2} - \int_{t_2}^{t} \frac{V_o}{L_r} dt = I_{Lr2} - \frac{V_o}{L_r}(t - t_2)$$

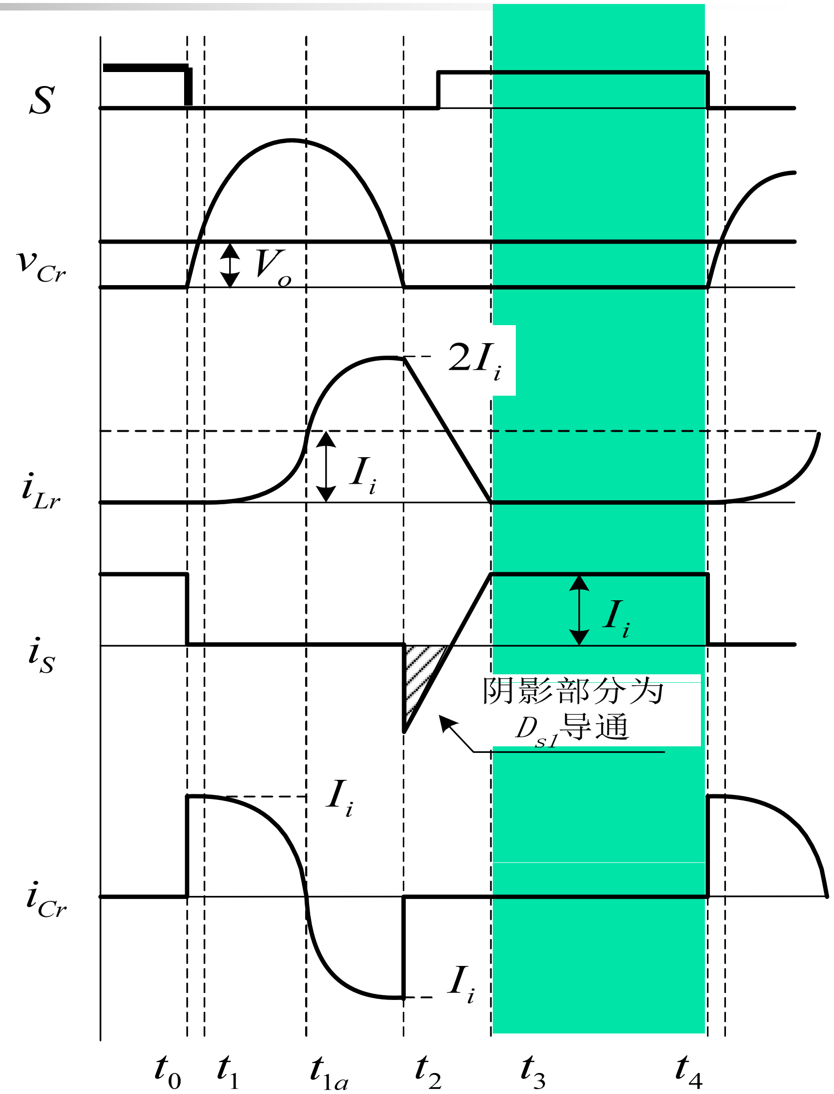
Duration: $$T_3 = t_3 - t_2 = \frac{L_r I_{Lr}(t_2)}{V_o}$$

Switch S may be turned on with ZVS when *Ds1* is conducting

Stage 4: freewheel (t3-t4)



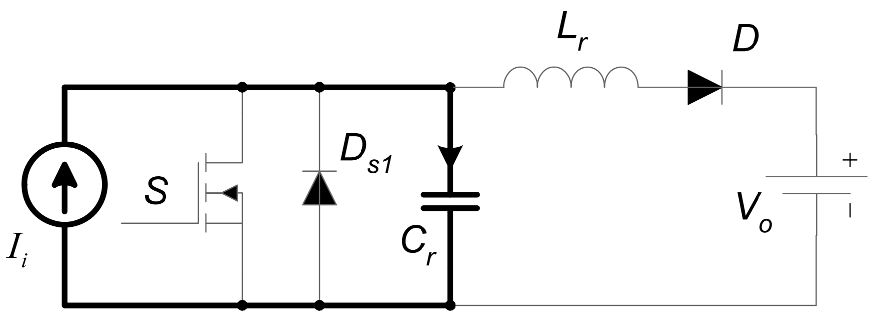
(d) 阶段4(t_3, t_4)续流阶段



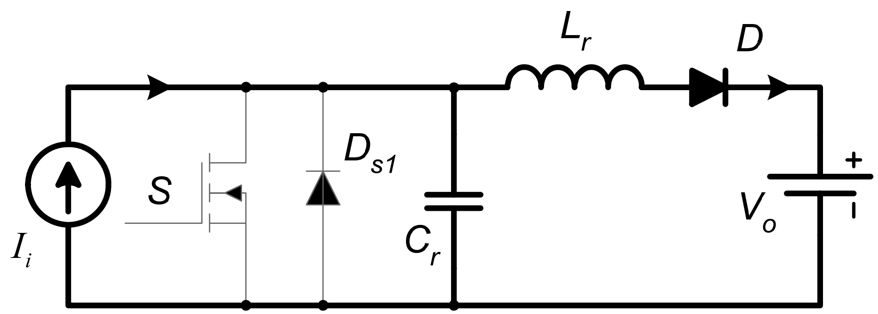
Duration decided by switching freq.

$$T_4 = T_s - T_1 - T_2 - T_3$$

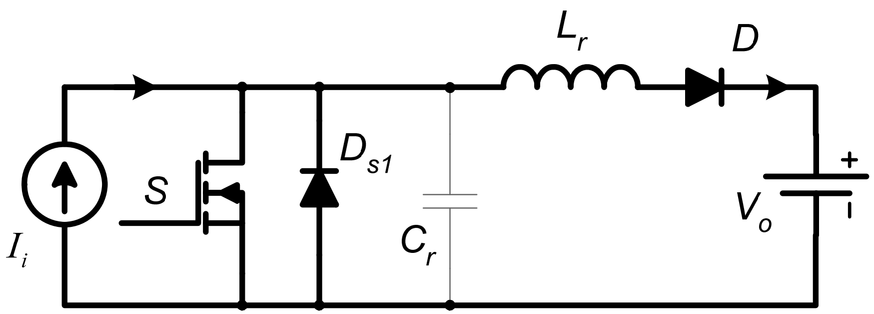
Stages in a cycle



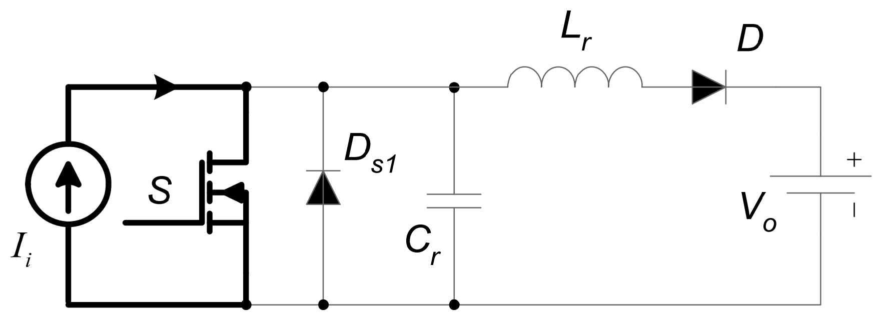
（a）阶段1（t_0 ，t_1）电容充电阶段



（b）阶段2（t_1 ，t_2）谐振阶段



（c）阶段3（t_2 ，t_3）电感放磁阶段



（d）阶段4（t_3 ，t_4）续流阶段

ZVS condition

Resonant cap voltage v_{Cr} must resonance to zero in stage 2

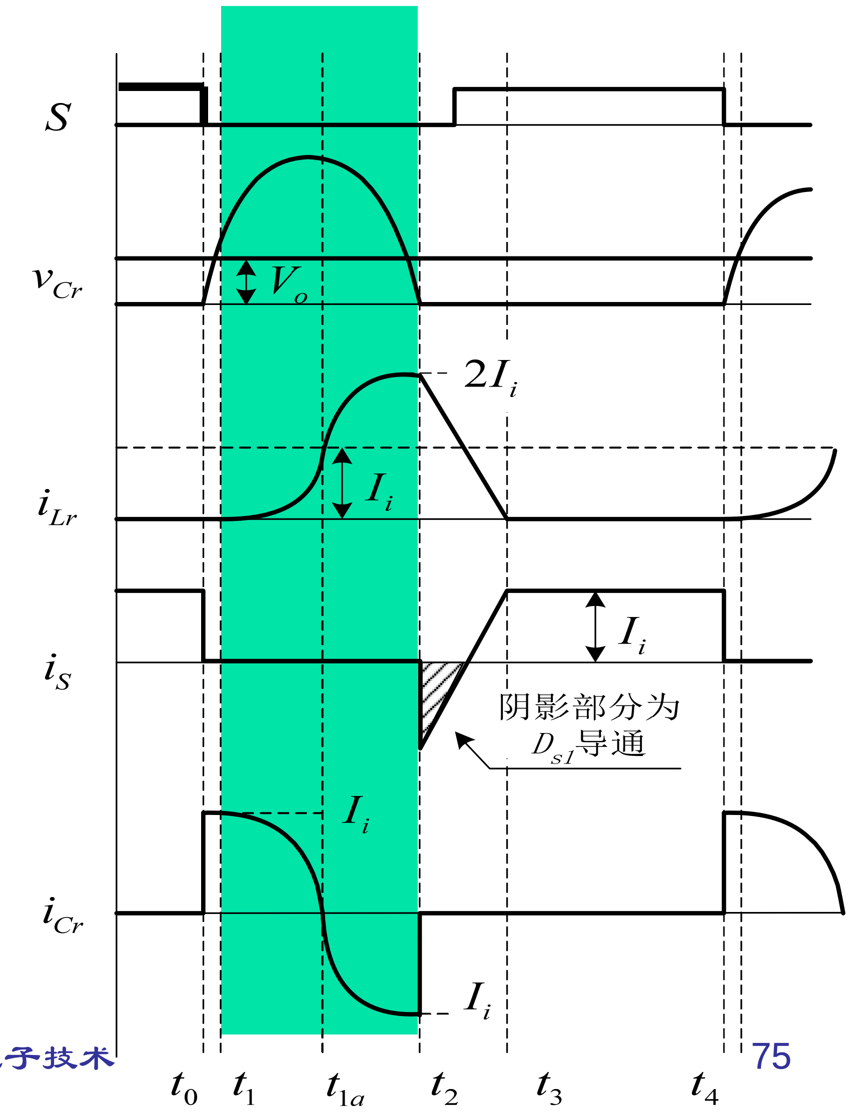
$$v_{Cr}(t) = V_o + I_i Z_r \sin\omega_r (t - t_1)$$

$$I_{i\min} Z_r > V_o \quad \Rightarrow \quad Z_r > \frac{V_o}{I_{i\min}}$$

$I_{i\min}$ Minimum input current

Cap peak voltage $V_{Cr\max} = V_o + I_{i\max} Z_r$

Therefore $V_{Cr\max} > V_o \left(1 + \frac{I_{i\max}}{I_{i\min}}\right)$



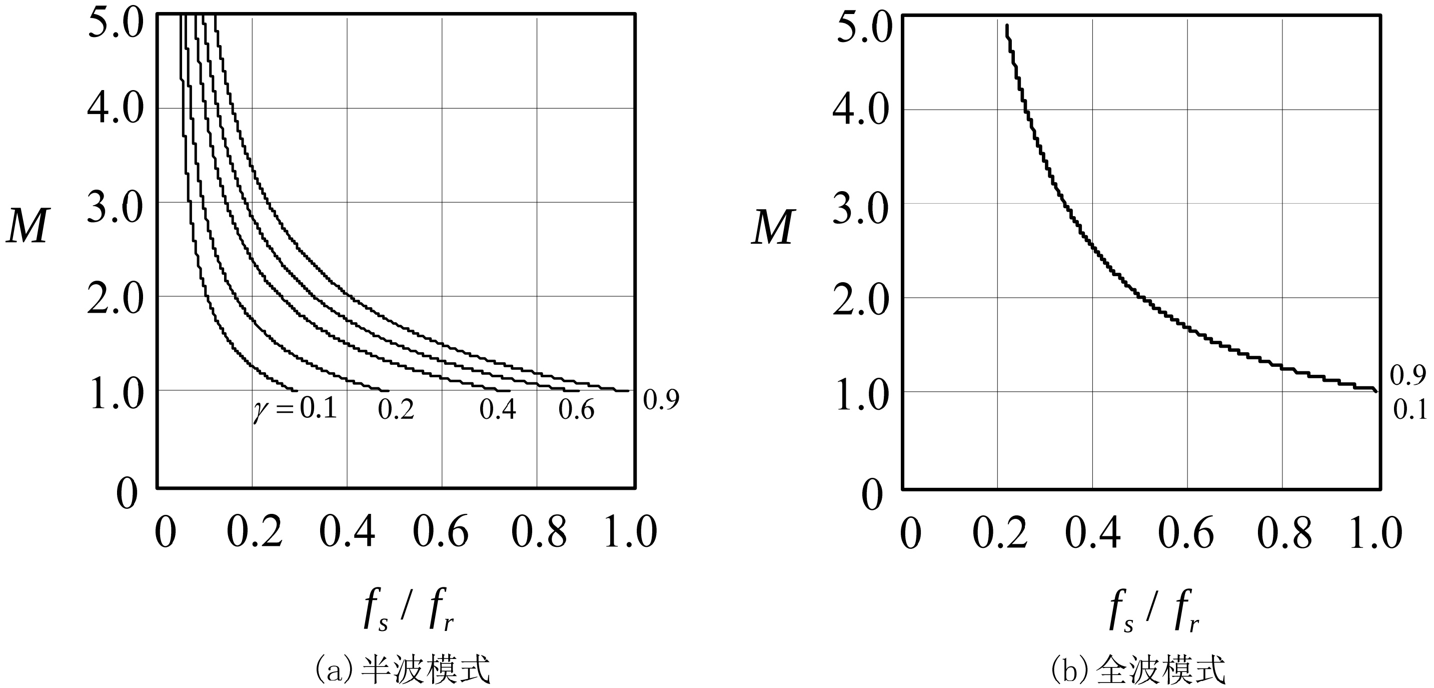
DC/DC conversion ratio

By energy conservation law, conversion ratio derived

$$M = \frac{V_o}{V_s} = \frac{1}{\dfrac{f_s}{2\pi f_r}[\pi + \sin^{-1}(\dfrac{\gamma}{M}) + \dfrac{\gamma}{2M} + \dfrac{M}{\gamma}(1 + \sqrt{1 - \dfrac{\gamma^2}{M^2}})]}$$

Where $\gamma = \dfrac{R_0}{Z_r}$

DC/DC conversion ratio



Half wave case: conversion ratio also affected by load
Full wave case: conversion ratio not related to load

Full wave: $$M \approx \frac{f_r}{f_s}$$

ZCS vs. ZVS

ZCS QRC:

- Switch is ZCS turn-off
- diode D is zero voltage off, reverse recovery reduced
- Switch turn-on loss and EMI noise

ZVS QRC:

- Switch is ZVS turn-on
- Parasitic resonance between D junction cap and resonant inductor
- Higher voltage stress on switch

$$V_{Cr\max} > V_o\left(1+\frac{I_{i\max}}{I_{i\min}}\right)$$

QRC vs. PWM converter

QRC:

- switching loss is reduced
- Circuit is simple
- Higher current or voltage stress
- Conduction loss is higher
- Variable frq control cause filter larger ???