Changes to MOSS Memory Management Simulator

The MOSS memory management simulator emulates the case where all physical frames have been allocated to virtual memory pages. The "memset" lines in the configuration file provide the initial picture of page allocation scheme, in effect providing the initial state of the Page table. From this initial setting the simulator extracts the following:
1. The number of physical pages used by the process that reflects the resident set of the process and thus emulating the fixed allocation replacement policy.
2. The initial clock value by selecting the maximum time from the "in memory time" and "last touched time" values in the table.

The simulator code has been modified and provides the following features:

1. The clock is now incremented with a random value between 1 and 10 ns at each step.
2. The trace log records have the following format:
   <clock> <operation> <address> Virt Addr <Pg #> <offset> Phys Addr <Fr #> <offset>
   where, <clock> is value of clock, <operation> is either READ or WRITE, <address> is the referenced address using the address radix specified in the configuration file (binary, hex, decimal, etc). Two other addresses are provided in a form to show the components of the Virtual and Physical addresses.
3. Two bit have been added to the PageTableEntry class, the "p" bit (present) and the "u" bit.
4. Must specify a configuration file with an initial page table using memset lines.
5. Have added to following commands to simulate execution of programs:
   a. WRITESEQ <num> <codeAdr> <dataAdr> <inc>
   b. READSEQ <num> <codeAdr> <dataAdr> <inc>
      These two commands run <num> loops in which <codeAdr> is read, followed by a write (WRITESEQ) or read (READSEQ) of the <dataAdr>. At each iteration of the loop, dataAdr is incremented by <inc>.
   c. LOOP <num> <codeAdr> <dataAdr1> [<dataAdr2>…. <dataAdr5>]
      Creates a loop (run <num> iterations) where each of <codeAdr> and up to 5 <dataAdr> are read. The data addresses (dataAdrX) can be spread through the virtual address space to create page faults (depending on the number pages in the resident set).