

System Table Registers

	47(79)	16 15	0
GDTR	32(64)-bit Linear Base Address	16-Bit Table Limit	
IDTR	32(64)-bit Linear Base Address	16-Bit Table Limit	

System Segment Registers

Segment Descriptor Registers (Automatically Loaded)

	15	0			Attributes
Task Register	Seg. Sel.	32(64)-bit Linear Base Address	Segment Limit		
LDTR	Seg. Sel.	32(64)-bit Linear Base Address	Segment Limit		

Figure 2-5. Memory Management Registers