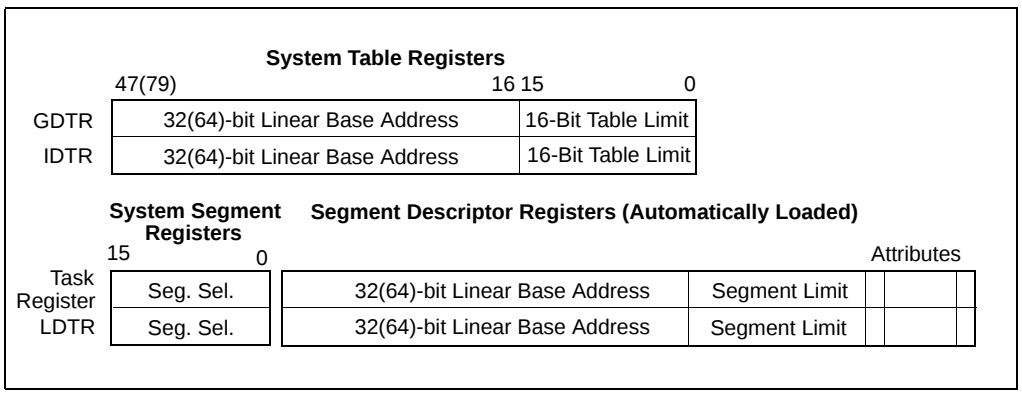

Figure 2-5. Memory Management Registers