

## 1K × 8-BIT STATIC RAM MK4801A(P/J/N)-1/2/3/4

## **FEATURES**

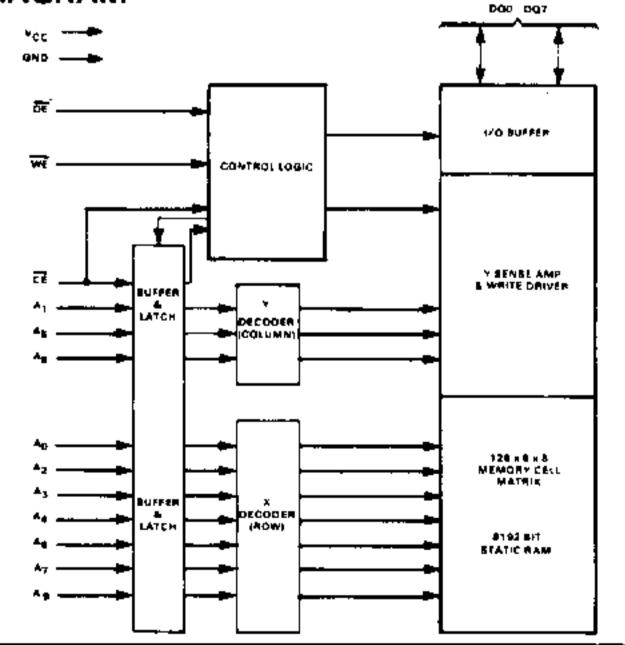
- Static operation
- □ Organization: 1K x 8 bit RAM JEDEC pinout
- ☐ High performance
- □ Pin compatible with Mostek's BYTEWYDE™ memory family
- □ 24/28 pin ROM/PROM compatible pin configuration
- ☐ CE and OE functions facilitate bus control

#### DESCRIPTION

The MK4801A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated<sup>TM</sup> circuit design techniques.

## **BLOCK DIAGRAM**

Figure 1



#### **TRUTH TABLE**

	IADEL			
CE	ŌĒ	WE	Mode	DQ
V <sub>IH</sub>	×	×	Deselect	H <del>i</del> gh Z
$V_{\rm IL}$	×	V <sub>IL</sub>	Write	D <sub>iN</sub>
V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Read	D <sub>OUT</sub>
$V_{\mid L}$	VIH	V <sub>IH</sub>	Read	High Z
X = Don	't Care			

## □ MKB version screened to MIL-STD-883

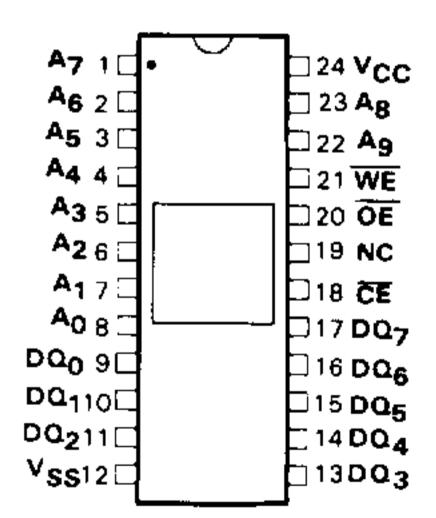
Part No.	R/W Access Time	R/W Cycle Time
MK4801A-1	120 nsec	120 nsec
MK4801A-2	150 nsec	150 nsec
MK4801A-3	200 nsec	200 nsec
MK4801A-4	250 nsec	250 nsec

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

## **PIN CONNECTIONS**

Figure 2

DATA INPUTS OUTPUTS



PIN NAMES
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A <sub>O</sub> -A <sub>9</sub>	Address Inputs	WE	Write Enable Output Enable No Connection Data In/Data Out
CE	Chip Enable	OE	
V <sub>SS</sub>	Ground	NC	
V <sub>CC</sub>	Power (+5V)	DQ <sub>0</sub> -DQ <sub>7</sub>	
100		07	

### **ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to V <sub>SS</sub>	5 V to +7.0 V
Operating Temperature T <sub>A</sub> (Ambient)	0°C to +70°C
Storage Temperature (Ambient)(Ceramic)	
Storage Temperature (Ambient)(Plastic)	55°C to +125°C
Power Dissipation	1 Watt
Output Current	20 mA

<sup>\*</sup>Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS7

 $(0^{\circ}C \le T_{A} \le +70^{\circ}C)$ 

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	NOTES
V <sub>cc</sub>	Supply Voltage	4.75	5.0	5.25	V	1
V <sub>SS</sub>	Supply Voltage	0	0	0	V	1
V <sub>IH</sub>	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V <sub>IL</sub>	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 9

## DC ELECTRICAL CHARACTERISTICS',7

 $(0^{\circ}C \le T_{A} \le +70^{\circ}C) (V_{CC} = 5.0 \text{ V} \pm 5\%)$ 

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I <sub>CC1</sub>	Average V <sub>CC</sub> Power Supply Current		50	80	mA	8
ارر	Input Leakage Current (Any Input)	-10		10	μΑ	2
l <sub>OL</sub>	Output Leakage Current	-10		10	μΑ	2
V <sub>OH</sub>	Output Logic "1" Voltage	2.4			V	
V <sub>OL</sub>	Output Logic "O" Voltage			0.4	٧	

## CAPACITANCE<sup>1</sup>,<sup>7</sup>

 $(0^{\circ}C \le T_{A} \le +70^{\circ}C) (V_{CC} = +5.0 V \pm 5\%)$ 

SYM	PARAMETER	TYP	MAX	NOTES
CI	All pins (except D/Q)	4 pF	6 pF	
C <sub>D/Q</sub>	D/Q pins	10 pF	12 pF	6

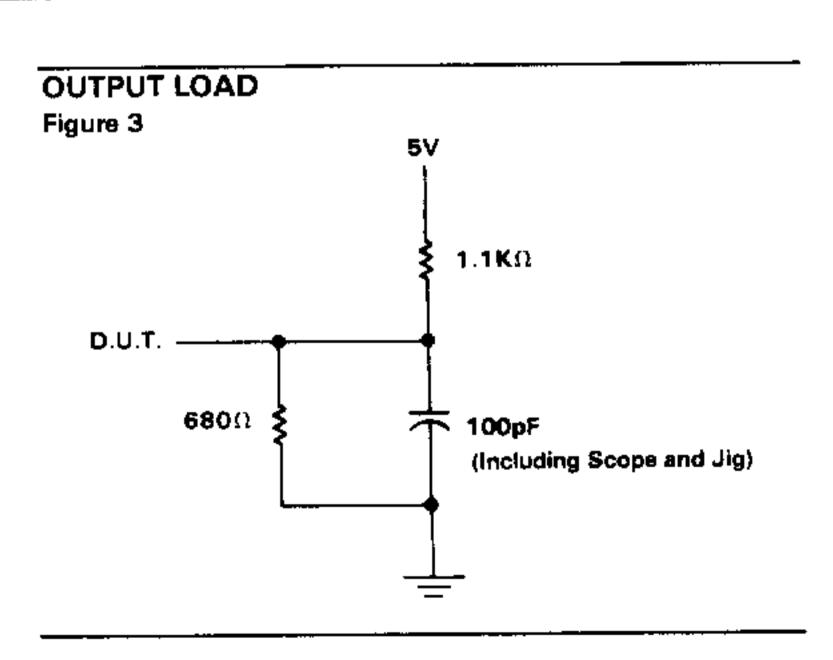
## AC ELECTRICAL CHARACTERISTICS 3,4

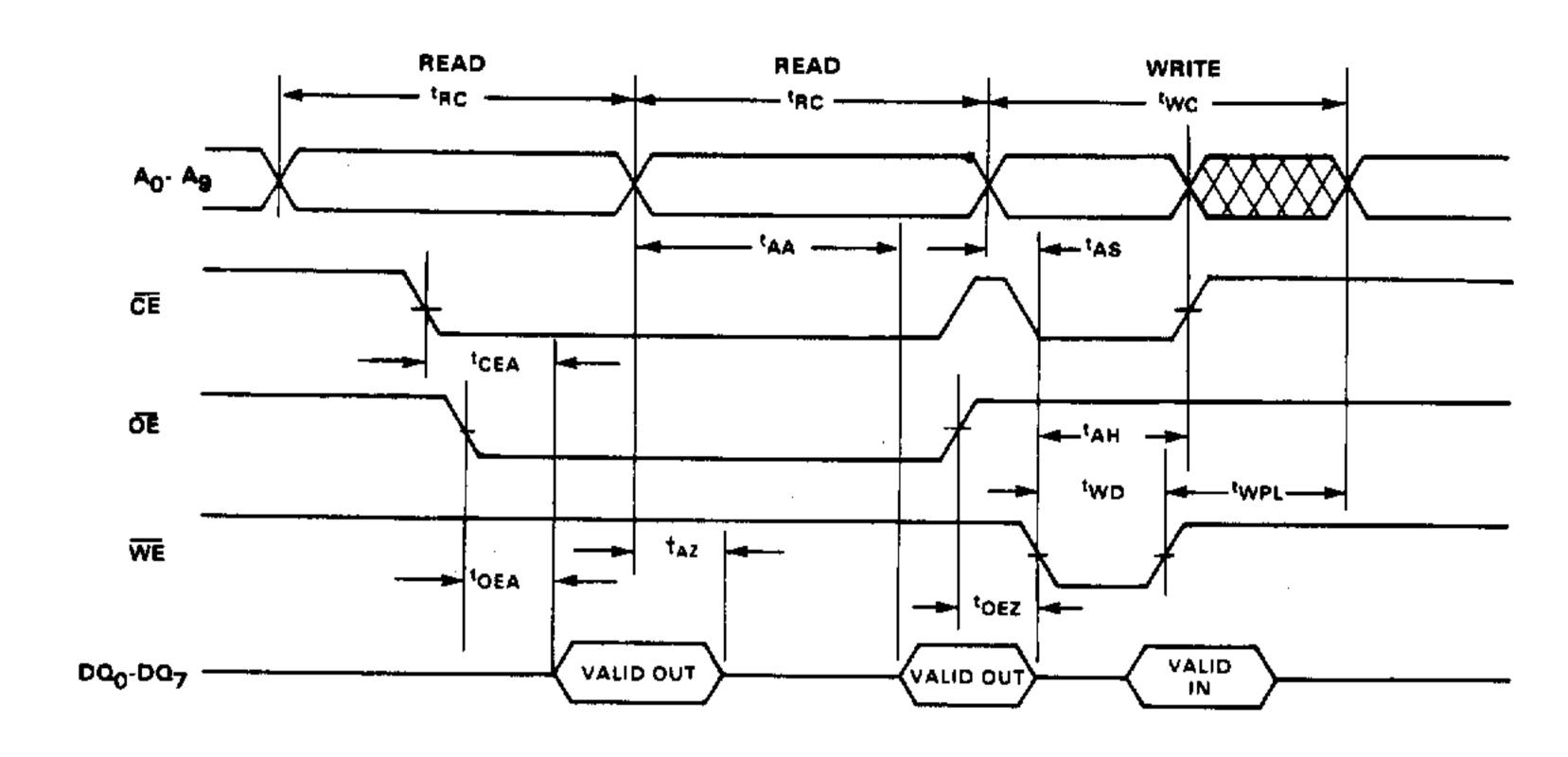
 $(0^{\circ}\text{C} \le \text{T}_{A} \le 70^{\circ}) (\text{V}_{CC} = 5.0 \text{ V} \pm 5\%)$ 

		-1		.2		·- <b>3</b>		-4			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
RC	Read Cycle Time	120		150		200		250		ns	
ĀA	Address Access Time	-	120		150		200		250	ns	5
CEA	Chip Enable Access Time		60		75		100		125	ns	5
CEZ	Chip Enable Data Off Time	5	30	5	35	.5	40	5	45	ns	·
OEA	Output Enable Access Time		60		75		100		125	ns	5
OEZ	Output Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
AZ	Address Data Off Time	10		10		10		10		ns	
wc	Write Cycle Time	120		150		200		250		ns	
AS	Address Setup Time	0		0		0		0		ns	see text
АН	Address Hold Time	40		50		65	-	80		ns	see text
bsw	Data To Write Setup Time	10		10		15		20		ns	
DHW	Data From Write Hold Time	10		10		10		10		ns	
WD	Write Pulse Duration	45		50		60		70		ns	see text
WEZ	Write Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
WPL	Write Pulse Lead Time	75		90		130		170		ns	

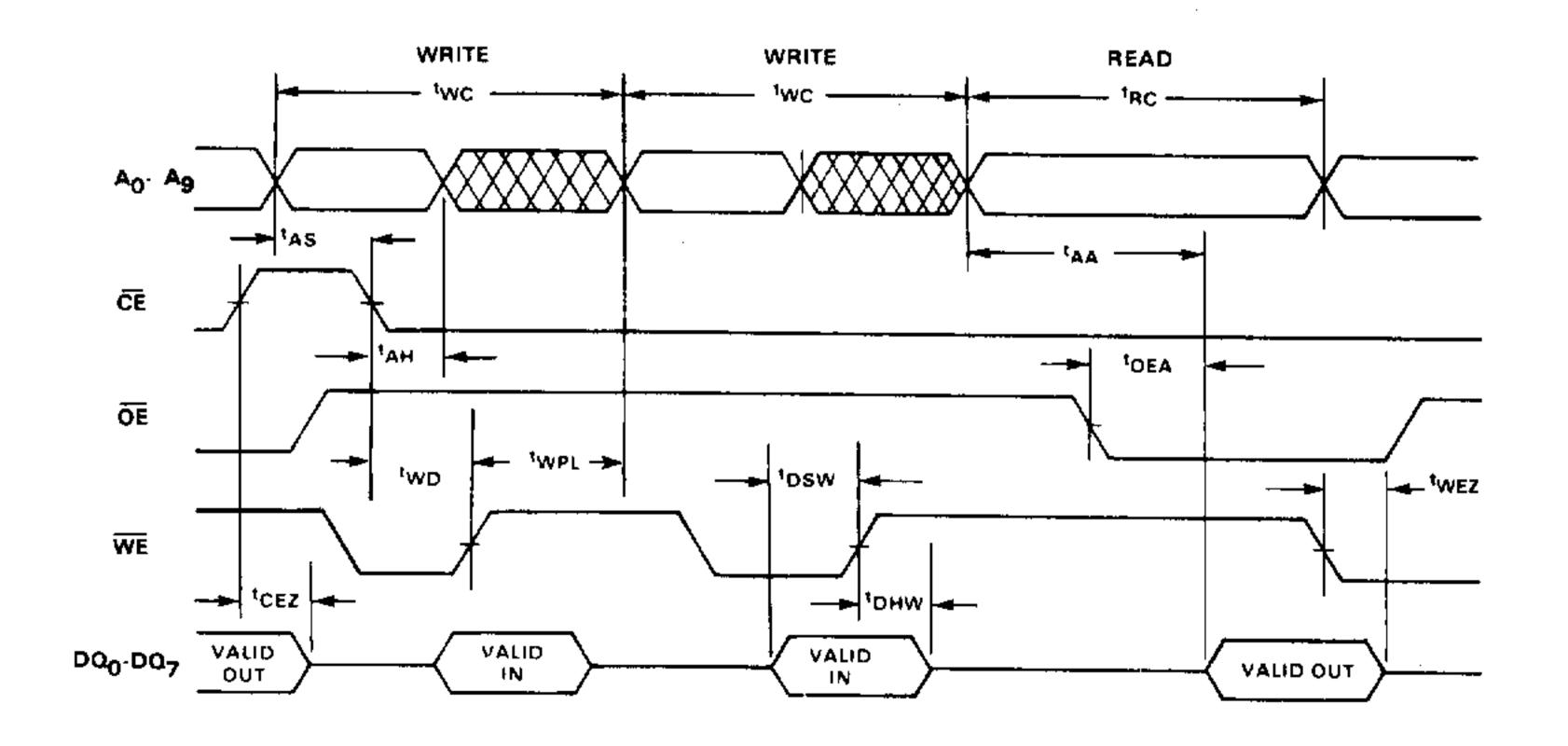
## NOTES:

- All voltages referenced to VSS Measured with .4  $\leq$  V $_{\parallel}$   $\leq$  5.0 V, outputs deselected and V $_{CC}$  = 5 V AC measurements assume Transition Time = 5 ns, levels VSS to 3.0 V
- Input and output timing reference levels are at 1.5 V
- Measured with a load as shown in Figure 3.
- Output buffer is deselected.
- A minimum of 2ms time delay is required after application of  $V_{CC}$  (+5 V) before proper device operation can be achieved.
- I<sub>CC</sub> measured with outputs open.
- Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.





# TIMING DIAGRAM Figure 5



The MK4801A features a fast  $\overline{CE}$  (50% of Address Access) function to permit memory expansion without impacting system access time. A fast  $\overline{OE}$  (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs. Mostek also offers a higher performance version of the MK4801A designated the MK4801A.

#### **OPERATION**

#### Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input (WE) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t<sub>AZ</sub>. Valid Data will be available to the 8 Data Output Drivers within t<sub>AA</sub> after the last address input signal is stable, providing that the CE and OE access times are satisfied. If CE or OE access times are not met, data access will be measured from the limiting parameter

(t<sub>CEA</sub> or t<sub>OEA</sub>) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable (CE) and Output Enable (OE) control signals.

#### Write Mode

The MK4801A is in the Write Mode whenever the Write Enable (WE) and Chip Enable (CE) control inputs are in the low state.

The WRITE cycle is initiated by the WE pulse going low provided that CE is also low. The leading edge of the WE pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either WE or CE will determine the start of the write cycle. Therefore,  $t_{AS}$ ,  $t_{WD}$  and  $t_{AH}$  are referenced to the latter occurring edge of CE or WE. Addresses are latched at this time. All write cycles whether, initiated by CE or WE must be terminated by the rising edge of WE. If the output bus has been enabled (CE and OE low) then WE will cause the output to go to the high Z state in  $t_{WEZ}$ .

Data In must be valid t<sub>DSW</sub> prior to the low to high transition of WE. The Data In lines must remain stable for t<sub>DHW</sub> after WE goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, OE should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.