



Low-Power, 16-Bit, 500kSPS, 4-/8-Channel Unipolar Input ANALOG-TO-DIGITAL CONVERTERS with Serial Interface

Check for Samples: [ADS8331](#), [ADS8332](#)

FEATURES

- **Low-Power, Flexible Supply Range:**
 - 2.7V to 5.5V Analog Supply
 - 8.7mW (250kSPS in Auto-Nap Mode, $V_A = 2.7V$, $V_{BD} = 1.65V$)
 - 14.2mW (500kSPS, $V_A = 2.7V$, $V_{BD} = 1.65V$)
- **Up to 500kSPS Sampling Rate**
- **Excellent DC Performance:**
 - ± 1.2 LSB Typ, ± 2 LSB Max INL at 2.7V
 - ± 0.6 LSB Typ, $-1.0/1.5$ LSB Max DNL at 2.7V
 - 16-Bit NMC Over Temperature
- **Excellent AC Performance at 5V, $f_{IN} = 1kHz$:**
 - 91.5dB SNR, 101dB SFDR, $-100dB$ THD
- **Flexible Analog Input Arrangement:**
 - On-Chip 4-/8-Channel Mux with Breakout
 - Auto/Manual Channel Select and Trigger
- **Other Hardware Features:**
 - On-Chip Conversion Clock (CCLK)
 - Software/Hardware Reset
 - Programmable Status/Polarity EOC/ \overline{INT}
 - Daisy-Chain Mode
 - Global \overline{CONVST} (Independent of \overline{CS})
 - Deep, Nap, and Auto-Nap Powerdown Modes
 - SPI™/DSP Compatible Serial Interface
 - Separate I/O Supply: 1.65V to V_A
 - SCLK up to 40MHz ($V_A = V_{BD} = 5V$)
- **24-Pin 4x4 QFN and 24-Pin TSSOP Packages**

APPLICATIONS

- Communications
- Transducer Interfaces
- Medical Instruments
- Magnetometers
- Industrial Process Control
- Data Acquisition Systems
- Automatic Test Equipment

DESCRIPTION

The ADS8331 is a low-power, 16-bit, 500k samples-per-second (SPS) analog-to-digital converter (ADC) with a unipolar, 4-to-1 multiplexer (mux) input. The device includes a 16-bit capacitor-based successive approximation register (SAR) ADC with inherent sample and hold.

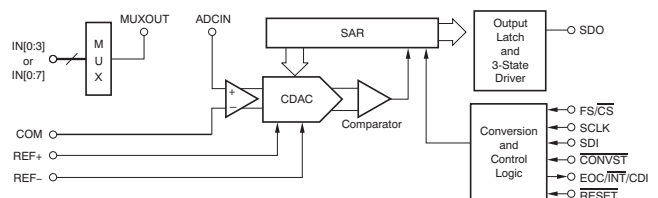
The ADS8332 is based on the same core and includes a unipolar 8-to-1 input mux. Both devices offer a high-speed, wide-voltage serial interface and are capable of daisy-chain operation when multiple converters are used.

These converters are available in 24-pin, 4x4 QFN and 24-pin TSSOP packages and are fully specified for operation over the industrial $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.

Low-Power, High-Speed, SAR Converter Family

RESOLUTION/TYPE	CHANNELS	500kSPS	1MSPS
16-Bit Pseudo-Diff	1	ADS8327	ADS8329
	2	ADS8328	ADS8330
	4	ADS8331	—
	8	ADS8332	—
14-Bit Pseudo-Diff	1	—	ADS7279
	2	—	ADS7280
12-Bit Pseudo-Diff	1	—	ADS7229
	2	—	ADS7230

Functional Block Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.⁽¹⁾

		ADS8331, ADS8332	UNIT
Voltage	IN _X , MUXOUT, ADCIN, REF+ to AGND	–0.3 to V _A + 0.3	V
	COM, REF– to AGND	–0.3 to 0.3	V
Voltage range	V _A to AGND	–0.3 to 7	V
	V _{BD} to DGND	–0.3 to 7	V
	AGND to DGND	–0.3 to 0.3	V
Digital input voltage to DGND		–0.3 to V _{BD} + 0.3	V
Digital output voltage to DGND		–0.3 to V _{BD} + 0.3	V
Operating free-air temperature range, (T _A)		–40 to +85	°C
Storage temperature range, (T _{STG})		–65 to +150	°C
Junction temperature (T _J Max)		+150	°C
4x4 QFN-24 Package	Power dissipation	(T _J Max – T _A)/θ _{JA}	W
	θ _{JA} thermal impedance	47	°C/W
TSSOP-24 Package	Power dissipation	(T _J Max – T _A)/θ _{JA}	W
	θ _{JA} thermal impedance	47	°C/W

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_A = 2.7V$

At $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_A = 2.7V$, $V_{BD} = 1.65V$ to $2.7V$, $V_{REF} = 2.5V$, and $f_{SAMPLE} = 500kSPS$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8331I, ADS8332I			ADS8331IB, ADS8332IB			UNIT		
			MIN	TYP	MAX	MIN	TYP	MAX			
ANALOG INPUT											
Full-scale input voltage ⁽¹⁾		IN _X – COM, ADCIN – COM	0		V _{REF}		0		V _{REF}	V	
Absolute input voltage		IN _X , ADCIN	AGND – 0.2		VA + 0.2		AGND – 0.2		VA + 0.2		V
		COM	AGND – 0.2		AGND + 0.2		AGND – 0.2		AGND + 0.2		V
Input capacitance		ADCIN	40		45		40		45		pF
Input leakage current		Unselected ADC input	±1				±1				nA
SYSTEM PERFORMANCE											
Resolution			16				16				Bits
No missing codes			16				16				Bits
INL	Integral linearity		–3	±2	3		–2	±1.2	2		LSB ⁽²⁾
DNL	Differential linearity		–1	±0.6	2		–1	±0.6	1.5		LSB ⁽²⁾
E _O	Offset error ⁽³⁾		–0.5	±0.15	0.5		–0.5	±0.15	0.5		mV
Offset error drift			±1				±1				PPM/°C
Offset error matching			–0.2		+0.2		–0.2		+0.2		mV
E _G	Gain error		–0.25	–0.06	0.25		–0.25	–0.06	0.25		%FSR
Gain error drift			±0.4				±0.4				PPM/°C
Gain error matching			–0.003		0.003		–0.003		0.003		%FSR
Transition noise			28				28				µV RMS
PSRR	Power-supply rejection ratio		74				74				dB
SAMPLING DYNAMICS											
t _{CONV}	Conversion time		18				18				CCLK
t _{SAMPLE1}	Acquisition time	Manual-Trigger mode	3				3				CCLK
t _{SAMPLE2}		Auto-Trigger mode	3				3				CCLK
Throughput rate			500				500				kSPS
DYNAMIC CHARACTERISTICS											
THD	Total harmonic distortion ⁽⁴⁾	V _{IN} = 2.5V _{PP} at 1kHz	–101				–101				dB
		V _{IN} = 2.5V _{PP} at 10kHz	–95				–95				dB
SNR	Signal-to-noise ratio	V _{IN} = 2.5V _{PP} at 1kHz	88				89				dB
		V _{IN} = 2.5V _{PP} at 10kHz	86.5				87.5				dB
SINAD	Signal-to-noise + distortion	V _{IN} = 2.5V _{PP} at 1kHz	87.5				88.5				dB
		V _{IN} = 2.5V _{PP} at 10kHz	86				87				dB
SFDR	Spurious-free dynamic range	V _{IN} = 2.5V _{PP} at 1kHz	103				103				dB
		V _{IN} = 2.5V _{PP} at 10kHz	98				98				dB
	Crosstalk	V _{IN} = 2.5V _{PP} at 1kHz	125				125				dB
		V _{IN} = 2.5V _{PP} at 100kHz	108				108				dB
	–3dB small-signal bandwidth	IN _X – COM with MUXOUT tied to ADCIN	17				17				MHz
		ADCIN – COM	30				30				MHz

(1) Ideal input span; does not include gain or offset error.

(2) LSB means least significant bit.

(3) Measured relative to an ideal full-scale input ($IN_X - COM$) of 2.5V when $V_A = 2.7V$.

(4) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: VA = 2.7V (continued)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_A = 2.7\text{V}$, $V_{BD} = 1.65\text{V}$ to 2.7V , $V_{REF} = 2.5\text{V}$, and $f_{\text{SAMPLE}} = 500\text{kSPS}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8331I, ADS8332I			ADS8331IB, ADS8332IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
CLOCK									
Internal conversion clock frequency			10.5	11	12.2	10.5	11	12.2	MHz
SCLK external serial clock		Used as I/O clock only	25			25			MHz
		Used as both I/O clock and conversion clock	1	21		1	21		MHz
EXTERNAL VOLTAGE REFERENCE INPUT									
V _{REF}	Input reference range ⁽⁵⁾	(REF+) – (REF–)	1.2	2.525		1.2	2.525		V
		(REF–) – AGND	–0.1	0.1		–0.1	0.1		V
Resistance ⁽⁶⁾		Reference input	20			20			kΩ
DIGITAL INPUT/OUTPUT									
Logic family			CMOS			CMOS			
V _{IH}	High-level input voltage	1.65V < V _{BD} < 2.5V	0.8 × V _{BD}	V _{BD} + 0.3		0.8 × V _{BD}	V _{BD} + 0.3		V
		2.5V ≤ V _{BD} ≤ V _A	0.65 × V _{BD}	V _{BD} + 0.3		0.65 × V _{BD}	V _{BD} + 0.3		V
V _{IL}	Low-level input voltage	1.65 < V _{BD} < 2.5V	–0.3	0.1 × V _{BD}		–0.3	0.1 × V _{BD}		V
		2.5V ≤ V _{BD} ≤ V _A	–0.3	0.25 × V _{BD}		–0.3	0.25 × V _{BD}		V
I _I	Input current	V _{IN} = V _{BD} or DGND	–1	1		–1	1		μA
C _I	Input capacitance		5			5			pF
V _{OH}	High-level output voltage	V _A ≥ V _{BD} ≥ 1.65V, I _O = 100μA	V _{BD} – 0.6		V _{BD}	V _{BD} – 0.6		V _{BD}	V
V _{OL}	Low-level output voltage	V _A ≥ V _{BD} ≥ 1.65V, I _O = –100μA	0	0.4		0	0.4		V
C _O	SDO pin capacitance	Hi-Z state	5			5			pF
C _L	Load capacitance		30			30			pF
Data format			Straight binary			Straight binary			
POWER-SUPPLY REQUIREMENTS									
V _A	Analog supply voltage ⁽⁵⁾		2.7	3.6		2.7	3.6		V
V _{BD}	Digital I/O supply voltage		1.65	V _A + 0.2		1.65	V _A + 0.2		V
I _A	Analog supply current	f _{SAMPLE} = 500kSPS	5.2		6.5	5.2		6.5	mA
		f _{SAMPLE} = 250kSPS in Auto-Nap mode	3.2			3.2			mA
		Nap mode, SCLK = V _{BD} or DGND	325		400	325		400	μA
		Deep PD mode, SCLK = V _{BD} or DGND	50		250	50		250	nA
I _{BD}	Digital I/O supply current	f _{SAMPLE} = 500kSPS	0.1		0.4	0.1		0.4	mA
		f _{SAMPLE} = 250kSPS in Auto-Nap mode	0.05			0.05			mA
	Power dissipation	V _A = 2.7V, V _{BD} = 1.65V, f _{SAMPLE} = 500kSPS	14.2		18.2	14.2		18.6	mW
		V _A = 2.7V, V _{BD} = 1.65V, f _{SAMPLE} = 250kSPS in Auto-Nap mode	8.72			8.72			mW
TEMPERATURE RANGE									
T _A	Operating free-air temperature		–40	+85		–40	+85		°C

(5) The ADS8331/32 operates with V_A between 2.7V and 5.5V, and V_{REF} between 1.2V and V_A . However, the device may not meet the specifications listed in the Electrical Characteristics when V_A is between 3.6V and 4.5V.

(6) Can vary $\pm 30\%$.

ELECTRICAL CHARACTERISTICS: VA = 5V

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_A = 5\text{V}$, $V_{BD} = 1.65\text{V}$ to 5V , $V_{REF} = 4.096\text{V}$, and $f_{SAMPLE} = 500\text{kSPS}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8331I, ADS8332I			ADS8331IB, ADS8332IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Full-scale input voltage ⁽¹⁾		IN _X – COM, ADCIN – COM	0		V _{REF}	0		V _{REF}	V
Absolute input voltage		IN _X , ADCIN	AGND – 0.2		VA + 0.2	AGND – 0.2		VA + 0.2	V
		COM	AGND – 0.2		AGND + 0.2	AGND – 0.2		AGND + 0.2	V
Input capacitance		ADCIN	40		45	40		45	pF
Input leakage current		Unselected ADC input	±1			±1			nA
SYSTEM PERFORMANCE									
Resolution			16			16			Bits
No missing codes			16			16			Bits
INL	Integral linearity		–3	±2	3	–2	±1	2	LSB ⁽²⁾
DNL	Differential linearity		–1	±1	2	–1	±0.5	1.5	LSB ⁽²⁾
E _O	Offset error ⁽³⁾		–1	±0.23	1	–1	±0.23	1	mV
Offset error drift			±1			±1			PPM/°C
Offset error matching			–0.125		0.125	–0.125		0.125	mV
E _G	Gain error		–0.25	–0.06	0.25	–0.25	–0.06	0.25	%FSR
Gain error drift			±0.02			±0.02			PPM/°C
Gain error matching			–0.003		0.003	–0.003		0.003	%FSR
Transition noise			30			30			μV RMS
PSRR	Power-supply rejection ratio		78			78			dB
SAMPLING DYNAMICS									
t _{CONV}	Conversion time		18			18			CCLK
t _{SAMPLE1}	Acquisition time	Manual-Trigger mode	3			3			CCLK
t _{SAMPLE2}		Auto-Trigger mode	3			3			CCLK
Throughput rate			500			500			kSPS
DYNAMIC CHARACTERISTICS									
THD	Total harmonic distortion ⁽⁴⁾	V _{IN} = 4.096V _{PP} at 1kHz	–100			–100			dB
		V _{IN} = 4.096V _{PP} at 10kHz	–94			–95			dB
SNR	Signal-to-noise ratio	V _{IN} = 4.096V _{PP} at 1kHz	90.5			91.5			dB
		V _{IN} = 4.096V _{PP} at 10kHz	88			88			dB
SINAD	Signal-to-noise + distortion	V _{IN} = 4.096V _{PP} at 1kHz	90			91			dB
		V _{IN} = 4.096V _{PP} at 10kHz	87			87			dB
SFDR	Spurious-free dynamic range	V _{IN} = 4.096V _{PP} at 1kHz	101			101			dB
		V _{IN} = 4.096V _{PP} at 10kHz	96			96			dB
	Crosstalk	V _{IN} = 4.096V _{PP} at 1kHz	119			119			dB
		V _{IN} = 4.096V _{PP} at 100kHz	107			107			dB
	–3dB small-signal bandwidth	IN _X – COM with MUXOUT tied to ADCIN	22			22			MHz
		ADCIN – COM	40			40			MHz

- (1) Ideal input span; does not include gain or offset error.
- (2) LSB means least significant bit.
- (3) Measured relative to an ideal full-scale input ($IN_X - \text{COM}$) of 4.096V when $V_A = 5\text{V}$.
- (4) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: VA = 5V (continued)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_A = 5\text{V}$, $V_{BD} = 1.65\text{V}$ to 5V , $V_{REF} = 4.096\text{V}$, and $f_{\text{SAMPLE}} = 500\text{kSPS}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8331I, ADS8332I			ADS8331IB, ADS8332IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
CLOCK									
Internal conversion clock frequency			10.9	11.5	12.6	10.9	11.5	12.6	MHz
SCLK external serial clock		Used as I/O clock only	40			40			MHz
		Used as both I/O clock and conversion clock	1			21			MHz
EXTERNAL VOLTAGE REFERENCE INPUT									
V _{REF}	Input reference range ⁽⁵⁾	(REF+) – (REF–)	1.2	4.096	4.2	1.2	4.096	4.2	V
		(REF–) – AGND	–0.1			0.1			V
Resistance ⁽⁶⁾		Reference input	20			20			kΩ
DIGITAL INPUT/OUTPUT									
Logic family			CMOS			CMOS			
V _{IH}	High-level input voltage	1.65 < V _{BD} < 2.5V	0.8 × V _{BD}		V _{BD} + 0.3	0.8 × V _{BD}		V _{BD} + 0.3	V
		2.5V ≤ V _{BD} ≤ V _A	0.65 × V _{BD}		V _{BD} + 0.3	0.65 × V _{BD}		V _{BD} + 0.3	V
V _{IL}	Low-level input voltage	1.65 < V _{BD} < 2.5V	–0.3		0.1 × V _{BD}	–0.3		0.1 × V _{BD}	V
		2.5V ≤ V _{BD} ≤ V _A	–0.3		0.25 × V _{BD}	–0.3		0.25 × V _{BD}	V
I _I	Input current	V _{IN} = V _{BD} or DGND	–1		1	–1		1	μA
C _I	Input capacitance		5			5			pF
V _{OH}	High-level output voltage	V _A ≥ V _{BD} ≥ 1.65V, I _O = 100μA	V _{BD} – 0.6		V _{BD}	V _{BD} – 0.6		V _{BD}	V
V _{OL}	Low-level output voltage	V _A ≥ V _{BD} ≥ 1.65V, I _O = –100μA	0		0.4	0		0.4	V
C _O	SDO pin capacitance	Hi-Z state	5			5			pF
C _L	Load capacitance		30			30			pF
Data format			Straight binary			Straight binary			
POWER-SUPPLY REQUIREMENTS									
V _A	Analog supply voltage ⁽⁵⁾		4.5	5	5.5	4.5	5	5.5	V
V _{BD}	Digital I/O supply voltage		1.65		V _A + 0.2	1.65		V _A + 0.2	V
I _A	Analog supply current	f _{SAMPLE} = 500kSPS	6.6		7.75	6.6		7.75	mA
		f _{SAMPLE} = 250kSPS in Auto-Nap mode	4.2			4.2			mA
		Nap mode, SCLK = V _{BD} or DGND	390		500	390		500	μA
		Deep PD mode, SCLK = V _{BD} or DGND	80		250	80		250	nA
I _{BD}	Digital I/O supply current	f _{SAMPLE} = 500kSPS	1.2		2.0	1.2		2.0	mA
		f _{SAMPLE} = 250kSPS in Auto-Nap mode	0.7			0.7			mA
	Power dissipation	V _A = 5.0V, V _{BD} = 5.0V, f _{SAMPLE} = 500kSPS	39		48.75	39		48.75	mW
		V _A = 5.0V, V _{BD} = 5.0V, f _{SAMPLE} = 250kSPS in Auto-Nap mode	24.5			24.5			mW
TEMPERATURE RANGE									
T _A	Operating free-air temperature		–40		+85	–40		+85	°C

(5) The ADS8331/32 operates with V_A between 2.7V and 5.5V, and V_{REF} between 1.2V and V_A . However, the device may not meet the specifications listed in the Electrical Characteristics when V_A is between 3.6V and 4.5V.

(6) Can vary $\pm 30\%$.

TIMING CHARACTERISTICS: VA = 2.7V

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_A = 2.7\text{V}$, and $V_{BD} = 1.65\text{V}$, unless otherwise noted. ⁽¹⁾ ⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, $f_{\text{CCLK}} = 1/2 f_{\text{SCLK}}$	0.5		10.5	MHz
		Internal	10.5	11	12.2	MHz
t_{SU1}	Setup time, rising edge of $\overline{\text{CS}}$ to EOC ⁽³⁾	Read while converting	1			CCLK
t_{H1}	$\overline{\text{CS}}$ hold time with respect to EOC ⁽³⁾	Read while sampling	25			ns
t_{WL1}	Pulse duration, $\overline{\text{CONVST}}$ low		40			ns
t_{WH1}	Pulse duration, $\overline{\text{CS}}$ high		40			ns
t_{SU2}	Setup time, rising edge of $\overline{\text{CS}}$ to EOS	Read while sampling	25			ns
t_{H2}	$\overline{\text{CS}}$ hold time with respect to EOS	Read while converting	25			ns
t_{SU3}	Setup time, falling edge of $\overline{\text{CS}}$ to first falling edge of SCLK		14			ns
t_{WL2}	Pulse duration, SCLK low		17	$t_{\text{SCLK}} - t_{\text{WH2}}$		ns
t_{WH2}	Pulse duration, SCLK high		12	$t_{\text{SCLK}} - t_{\text{WL2}}$		ns
t_{SCLK}	Cycle time, SCLK	I/O clock only	40			ns
		I/O and conversion clocks	47.6		1000	ns
		I/O clock, daisy-chain mode	40			ns
		I/O and conversion clocks, daisy-chain mode	47.6		1000	ns
t_{D1}	Delay time, falling edge of SCLK to SDO invalid	10pF load	8			ns
t_{D2}	Delay time, falling edge of SCLK to SDO valid	10pF load			35	ns
t_{D3}	Delay time, falling edge of $\overline{\text{CS}}$ to SDO valid, SDO MSB output	10pF load			35	ns
t_{SU4}	Setup time, SDI to falling edge of SCLK		8			ns
t_{H3}	Hold time, SDI to falling edge of SCLK		8			ns
t_{D4}	Delay time, rising edge of $\overline{\text{CS}}$ to SDO 3-state	10pF load			15	ns
t_{SU5}	Setup time, last falling edge of SCLK before rising edge of $\overline{\text{CS}}$		15			ns
t_{H4}	Hold time, last falling edge of SCLK before rising edge of $\overline{\text{CS}}$		2			ns
$t_{\text{SU6}}^{(4)}$	Setup time, rising edge of SCLK to rising edge of $\overline{\text{CS}}$		10			ns
$t_{\text{H5}}^{(4)}$	Hold time, rising edge of SCLK to rising edge of $\overline{\text{CS}}$		2			ns
t_{D5}	Delay time, falling edge of $\overline{\text{CS}}$ to deactivation of $\overline{\text{INT}}$	10pF load			40	ns

(1) All input signals are specified with $t_r = t_f = 1.5\text{ns}$ (10% to 90% of V_{BD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

(2) See the [Timing Diagrams](#) section.

(3) The EOC and EOS signals are the inverse of each other.

(4) Applies to the 5th or 17th rising SCLK when sending 4-bit or 16-bit commands, respectively, to the ADS8331/32.

TIMING CHARACTERISTICS: VA = 5V

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, and $V_A = V_{BD} = 5\text{V}$, unless otherwise noted. ⁽¹⁾ ⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, $f_{\text{CCLK}} = 1/2 f_{\text{SCLK}}$	0.5		10.5	MHz
		Internal	10.9	11.5	12.6	MHz
t_{SU1}	Setup time, rising edge of $\overline{\text{CS}}$ to EOC ⁽³⁾	Read while converting	1			CCLK
t_{H1}	$\overline{\text{CS}}$ hold time with respect to EOC ⁽³⁾	Read while sampling	20			ns
t_{WL1}	Pulse duration, $\overline{\text{CONVST}}$ low		40			ns
t_{WH1}	Pulse duration, $\overline{\text{CS}}$ high		40			ns
t_{SU2}	Setup time, rising edge of $\overline{\text{CS}}$ to EOS	Read while sampling	20			ns
t_{H2}	$\overline{\text{CS}}$ hold time with respect to EOS	Read while converting	20			ns
t_{SU3}	Setup time, falling edge of $\overline{\text{CS}}$ to first falling edge of SCLK		8			ns
t_{WL2}	Pulse duration, SCLK low		12	$t_{\text{SCLK}} - t_{\text{WH2}}$		ns
t_{WH2}	Pulse duration, SCLK high		11	$t_{\text{SCLK}} - t_{\text{WL2}}$		ns
t_{SCLK}	Cycle time, SCLK	I/O clock only	25			ns
		I/O and conversion clocks	47.6		1000	ns
		I/O clock, daisy-chain mode	25			ns
		I/O and conversion clocks, daisy-chain mode	47.6		1000	ns
t_{D1}	Delay time, falling edge of SCLK to SDO invalid	10pF load	5			ns
t_{D2}	Delay time, falling edge of SCLK to SDO valid	10pF load			20	ns
t_{D3}	Delay time, falling edge of $\overline{\text{CS}}$ to SDO valid, SDO MSB output	10pF load			20	ns
t_{SU4}	Setup time, SDI to falling edge of SCLK		8			ns
t_{H3}	Hold time, SDI to falling edge of SCLK		8			ns
t_{D4}	Delay time, rising edge of $\overline{\text{CS}}$ to SDO 3-state	10pF load			10	ns
t_{SU5}	Setup time, last falling edge of SCLK before rising edge of $\overline{\text{CS}}$		10			ns
t_{H4}	Hold time, last falling edge of SCLK before rising edge of $\overline{\text{CS}}$		2			ns
$t_{\text{SU6}}^{(4)}$	Setup time, rising edge of SCLK to rising edge of $\overline{\text{CS}}$		10			ns
$t_{\text{H5}}^{(4)}$	Hold time, rising edge of SCLK to rising edge of $\overline{\text{CS}}$		2			ns
t_{D5}	Delay time, falling edge of $\overline{\text{CS}}$ to deactivation of $\overline{\text{INT}}$	10pF load			20	ns

(1) All input signals are specified with $t_r = t_f = 1.5\text{ns}$ (10% to 90% of V_{BD}) and timed from a voltage level of $(V_{\text{IL}} + V_{\text{IH}})/2$.

(2) See the [Timing Diagrams](#) section.

(3) The EOC and EOS signals are the inverse of each other.

(4) Applies to the 5th or 17th rising SCLK when sending 4-bit or 16-bit commands, respectively, to the ADS8331/32.

TIMING DIAGRAMS

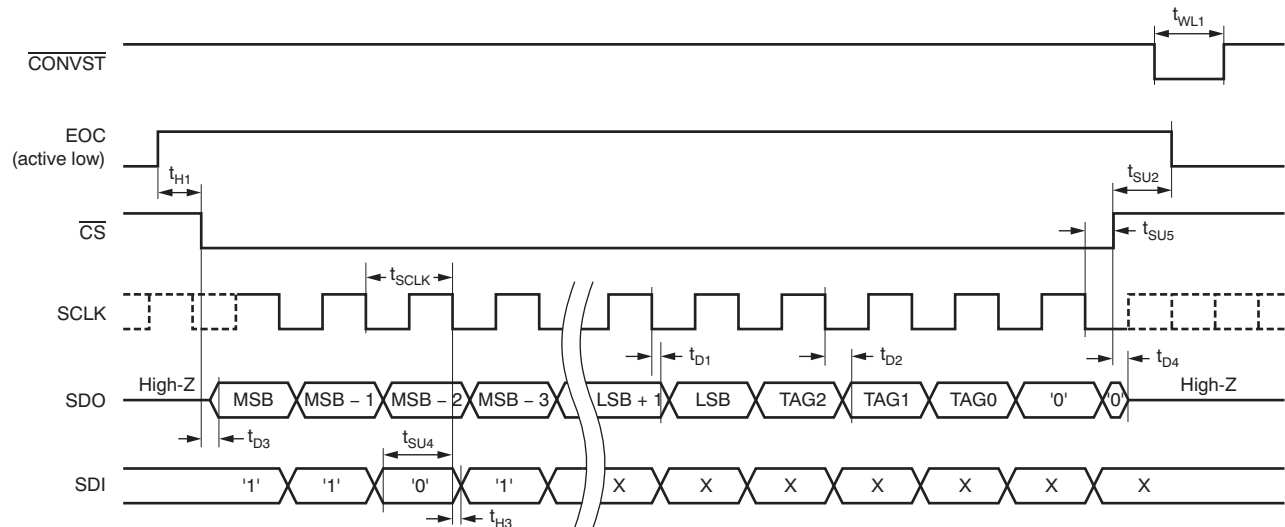


Figure 1. Read While Sampling (Shown with Manual-Trigger Mode)

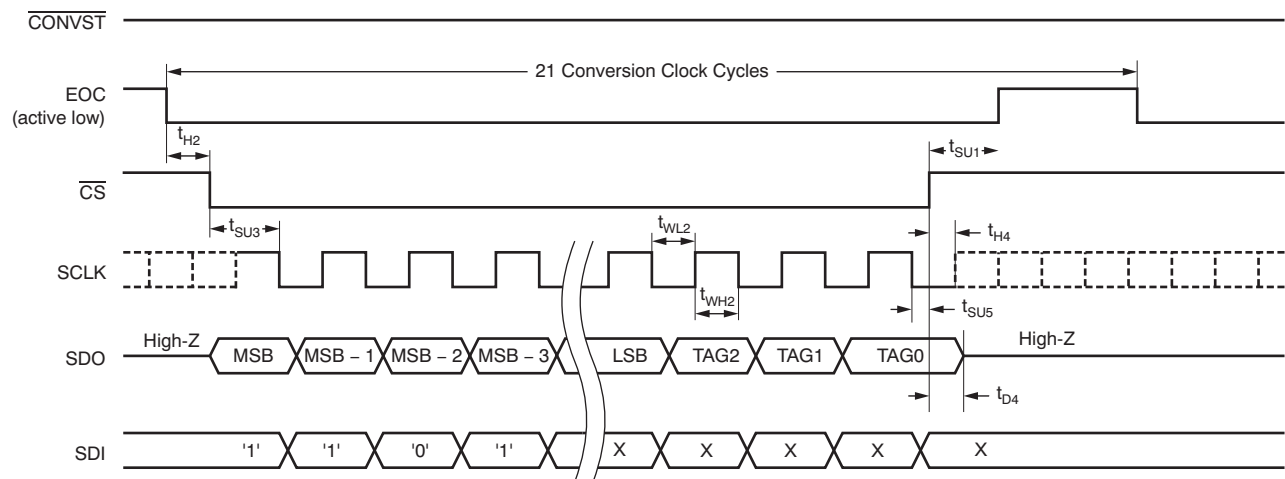


Figure 2. Read While Converting (Shown with Auto-Trigger Mode at 500 kSPS)

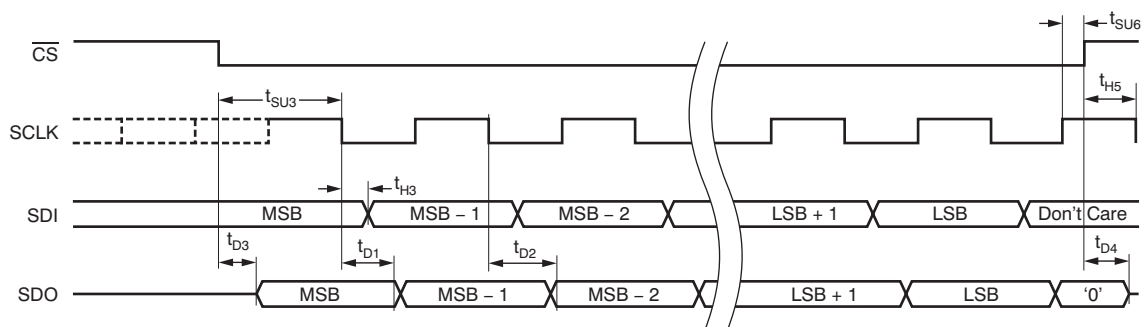


Figure 3. SPI I/O

TIMING DIAGRAMS (continued)

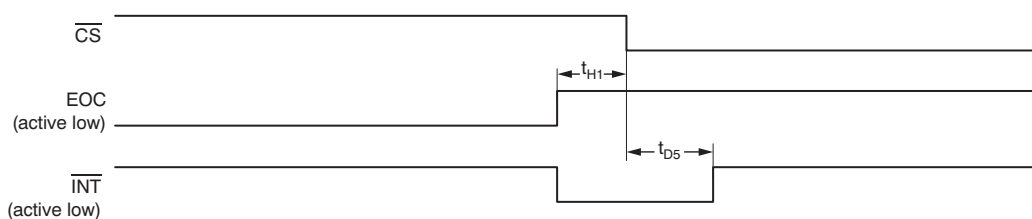
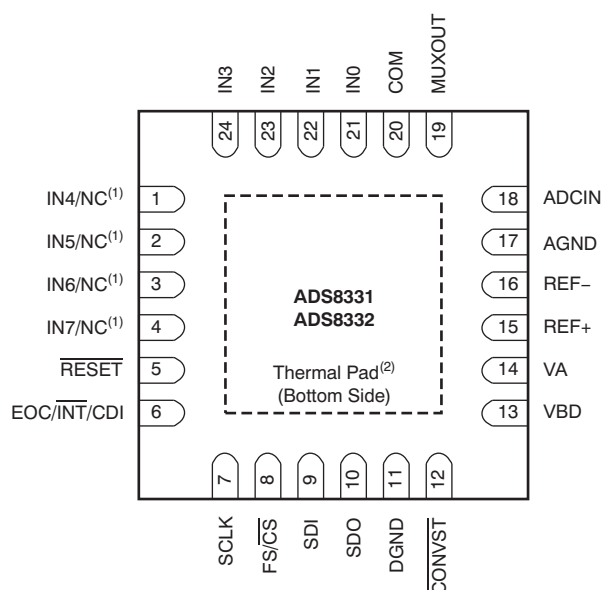


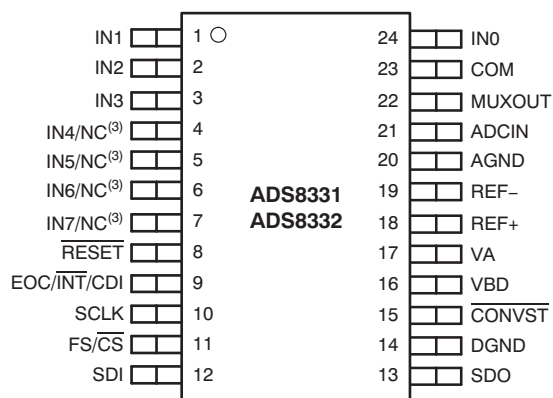
Figure 4. Relationship among \overline{CS} , EOC, and \overline{INT}

PIN ASSIGNMENTS

RGE PACKAGE 4x4 QFN-24 (TOP VIEW)



PW PACKAGE TSSOP-24 (TOP VIEW)



(1) NC = No internal connection (ADS8331 only).

(2) Connect thermal pad to analog ground.

(3) NC = No internal connection (ADS8331 only).

ADS8331 PIN DESCRIPTIONS

NAME	PIN NO.		I/O	DESCRIPTION
	TSSOP	QFN		
ADCIN	21	18	I	ADC input
AGND	20	17	–	Analog ground
DGND	14	11	–	Digital interface ground
COM	23	20	I	Common ADC input (usually connected to AGND)
CONVST	15	12	I	Conversion start. Freezes sample and hold, starts conversion.
EOC/INT/CDI	9	6	O/O/I	Status output. If programmed as end-of-conversion (EOC), this pin is low (default) when a conversion is in progress. If programmed as an interrupt (INT), this pin is low (default) after the end of conversion and returns high after FS/CS goes low. The polarity of EOC or INT is programmable. This pin can also be used as a chain data input (CDI) when operated in daisy-chain mode.
FS/CS	11	8	I	Frame sync signal for DSP (such as TMS320™ DSP) or chip select input for SPI.
IN _[0:3]	1-3, 24	21-24	I	Mux inputs
NC	4-7	1-4	–	No connection
MUXOUT	22	19	O	Mux output
REF+	18	15	I	External reference input
REF–	19	16	–	External reference ground (connect to AGND through an individual via on the printed circuit board)
RESET	8	5	I	External reset (active low)
SCLK	10	7	I	SPI clock for serial interface
SDI	12	9	I	SPI serial data in
SDO	13	10	O	SPI serial data out
VA	17	14	–	Analog supply, +2.7V to +5.5V
VBD	16	13	–	Digital interface supply

ADS8332 PIN DESCRIPTIONS

NAME	PIN NO.		I/O	DESCRIPTION
	TSSOP	QFN		
ADCIN	21	18	I	ADC input
AGND	20	17	–	Analog ground
DGND	14	11	–	Digital interface ground
COM	23	20	I	Common ADC input (usually connected to AGND)
CONVST	15	12	I	Conversion start. Freezes sample and hold, starts conversion.
EOC/INT/CDI	9	6	O/O/I	Status output. If programmed as end-of-conversion (EOC), this pin is low (default) when a conversion is in progress. If programmed as an interrupt (INT), this pin is low (default) after the end of conversion and returns high after FS/CS goes low. The polarity of EOC or INT is programmable. This pin can also be used as a chain data input (CDI) when operated in daisy-chain mode.
FS/CS	11	8	I	Frame sync signal for DSP (such as TMS320™ DSP) or chip select input for SPI.
IN _[0:7]	1-7, 24	1-4, 21-24	I	Mux inputs
MUXOUT	22	19	O	Mux output
REF+	18	15	I	External reference input
REF–	19	16	–	External reference ground (connect to AGND through an individual via on the printed circuit board)
RESET	8	5	I	External reset (active low)
SCLK	10	7	I	SPI clock for serial interface
SDI	12	9	I	SPI serial data in
SDO	13	10	O	SPI serial data out
VA	17	14	–	Analog supply, +2.7 V to +5.5 V
VBD	16	13	–	Digital interface supply

TYPICAL CHARACTERISTICS: DC Performance

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 2.500\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{CLK}} = 21\text{MHz}$, and $f_{\text{SAMPLE}} = 500\text{kSPS}$, unless otherwise noted.

**INTEGRAL LINEARITY ERROR
vs CODE**

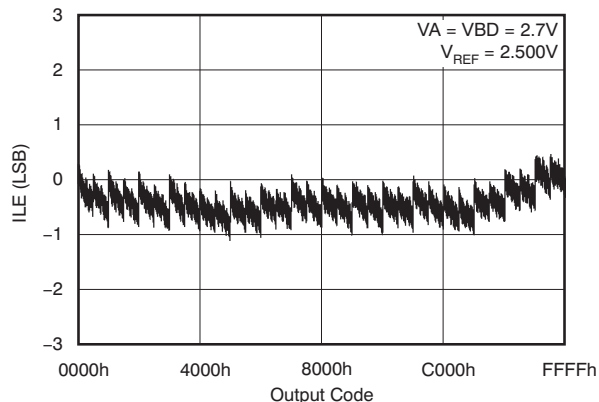


Figure 5.

**INTEGRAL LINEARITY ERROR
vs CODE**

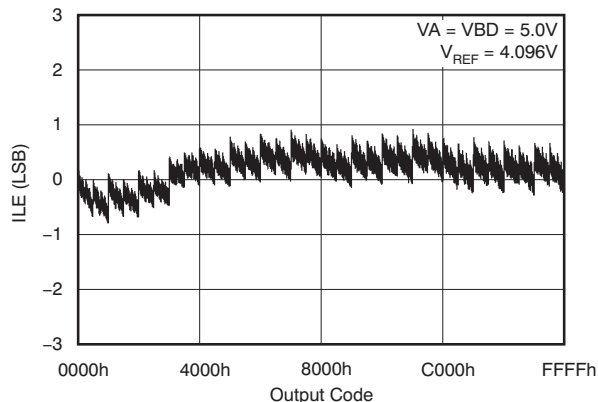


Figure 6.

**DIFFERENTIAL LINEARITY ERROR
vs CODE**

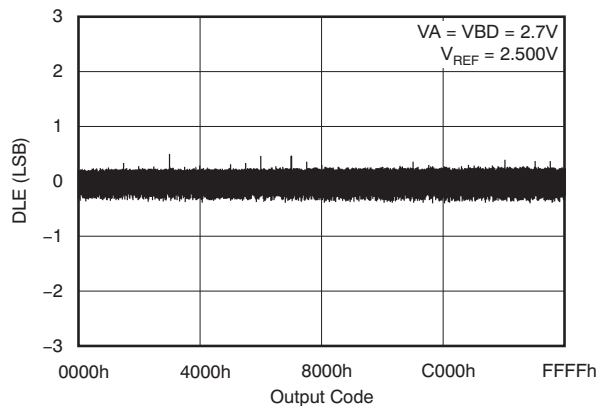


Figure 7.

**DIFFERENTIAL LINEARITY ERROR
vs CODE**

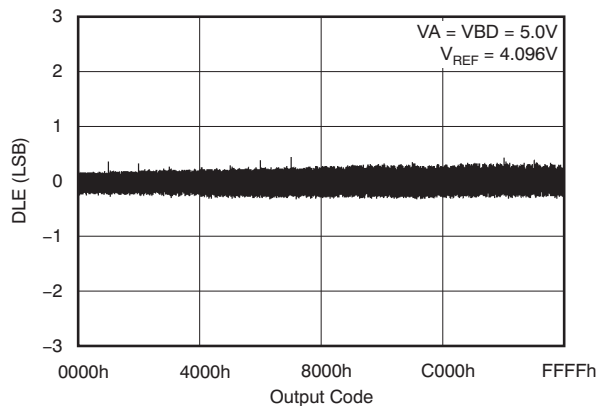


Figure 8.

**ANALOG SUPPLY CURRENT
vs ANALOG SUPPLY VOLTAGE**

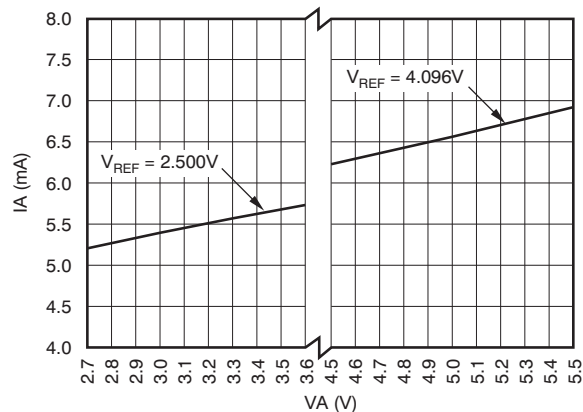


Figure 9.

**ANALOG SUPPLY CURRENT IN NAP MODE
vs ANALOG SUPPLY VOLTAGE**

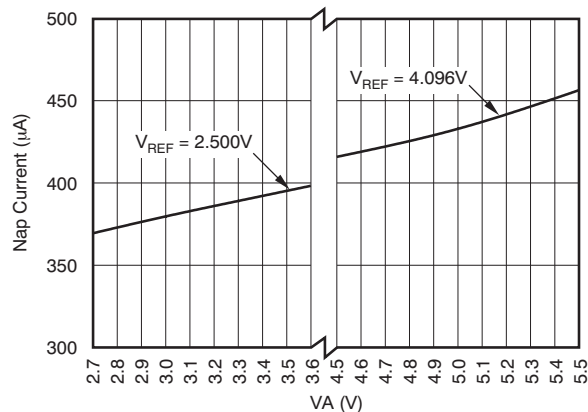


Figure 10.

TYPICAL CHARACTERISTICS: DC Performance (continued)

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF}+ - \text{REF}-) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF}+ - \text{REF}-) = 2.5\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{CLK}} = 21\text{MHz}$, and $f_{\text{SAMPLE}} = 500\text{kSPS}$, unless otherwise noted.

**ANALOG SUPPLY CURRENT
vs SAMPLING RATE IN AUTO-NAP MODE**

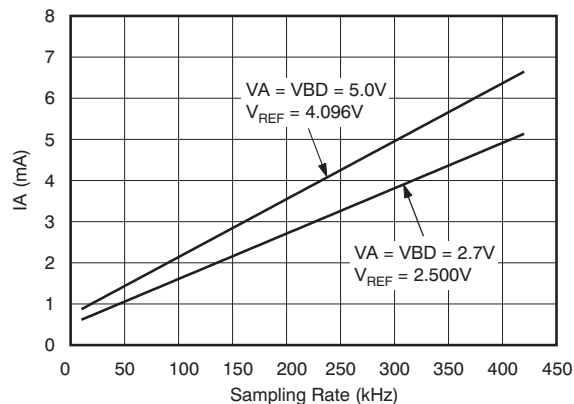


Figure 11.

**DEEP POWER-DOWN CURRENT
vs TEMPERATURE**

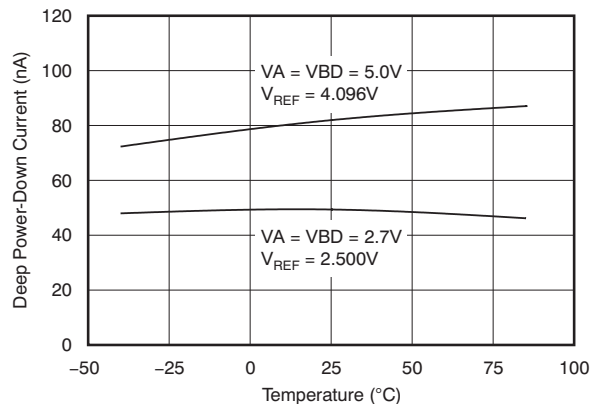


Figure 12.

**INTERNAL CLOCK FREQUENCY
vs ANALOG SUPPLY VOLTAGE**

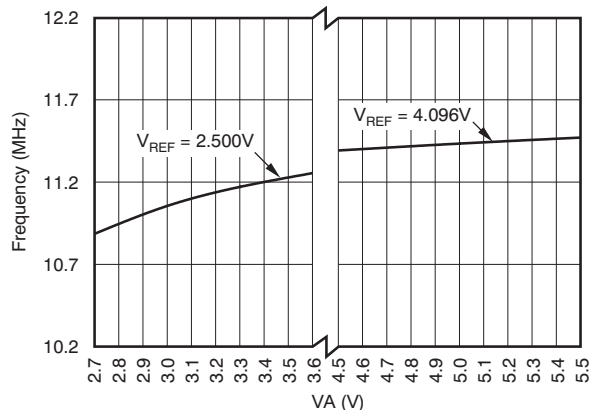


Figure 13.

**CHANGE IN GAIN
vs TEMPERATURE**

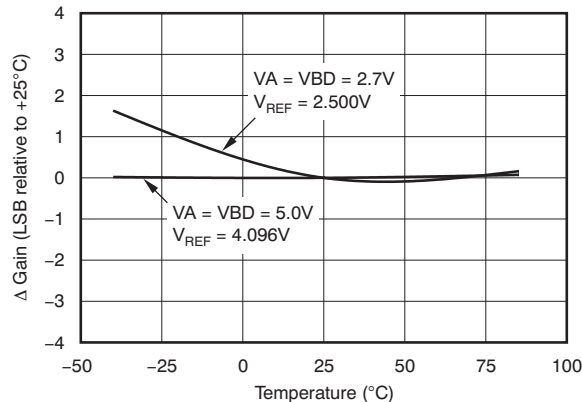


Figure 14.

**CHANGE IN OFFSET
vs TEMPERATURE**

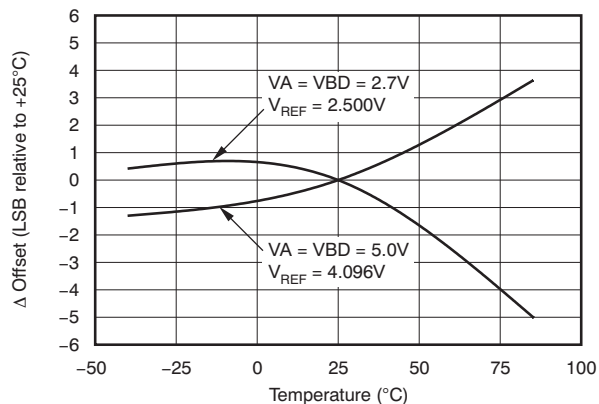


Figure 15.

**CHANGE IN ANALOG SUPPLY CURRENT
vs TEMPERATURE**

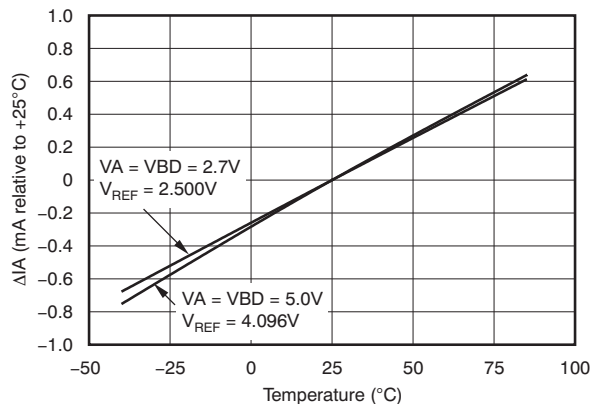


Figure 16.

TYPICAL CHARACTERISTICS: DC Performance (continued)

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 2.5\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{SCLK}} = 21\text{MHz}$, and $f_{\text{SAMPLE}} = 500\text{kSPS}$, unless otherwise noted.

**CHANGE IN DIGITAL SUPPLY CURRENT
vs TEMPERATURE**

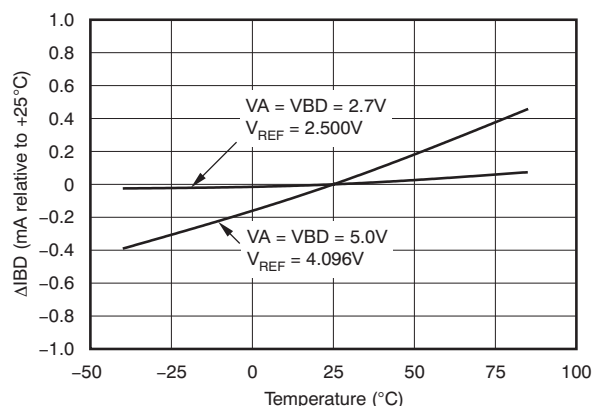


Figure 17.

**CHANGE IN INTERNAL CLOCK FREQUENCY
vs TEMPERATURE**

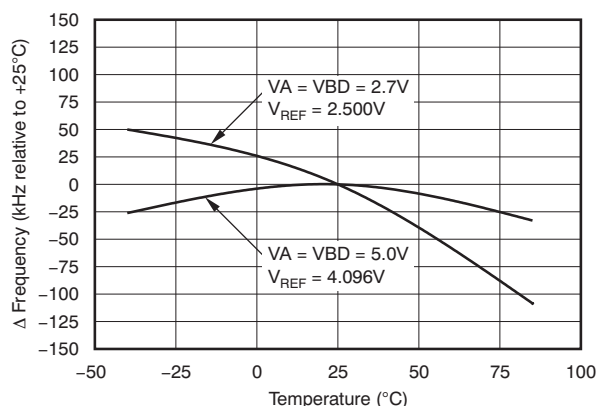


Figure 18.

**CHANGE IN ANALOG SUPPLY CURRENT IN NAP MODE
vs TEMPERATURE**

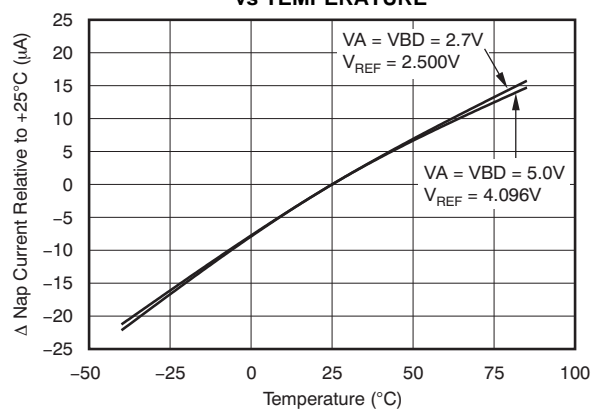


Figure 19.

TYPICAL CHARACTERISTICS: AC Performance

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 2.5\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{SCLK}} = 21\text{MHz}$, $f_{\text{SAMPLE}} = 500\text{kSPS}$, and $f_{\text{IN}} = 10\text{kHz}$, unless otherwise noted.

**OUTPUT CODE HISTOGRAM
FOR A DC INPUT (8192 Conversions)**

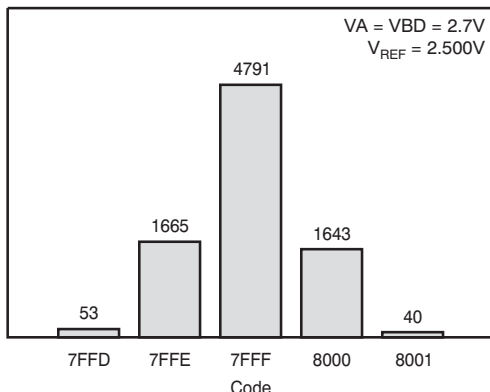


Figure 20.

**OUTPUT CODE HISTOGRAM
FOR A DC INPUT (8192 Conversions)**

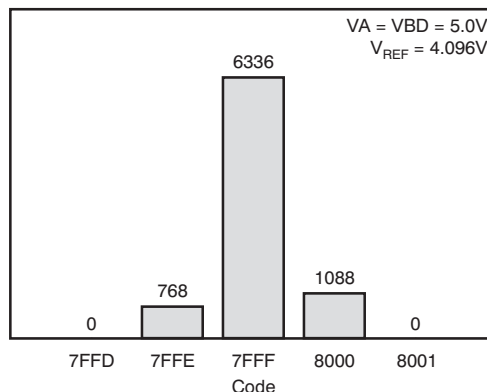


Figure 21.

**FREQUENCY SPECTRUM
(8192 Point FFT, $f_{\text{IN}} = 1.0376\text{kHz}$, -0.2dB)**

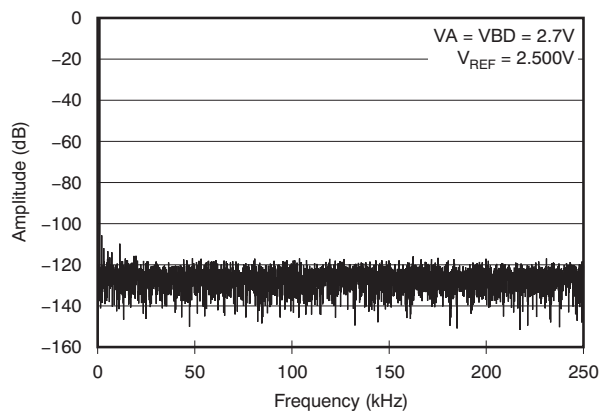


Figure 22.

**FREQUENCY SPECTRUM
(8192 Point FFT, $f_{\text{IN}} = 1.0376\text{kHz}$, -0.2dB)**

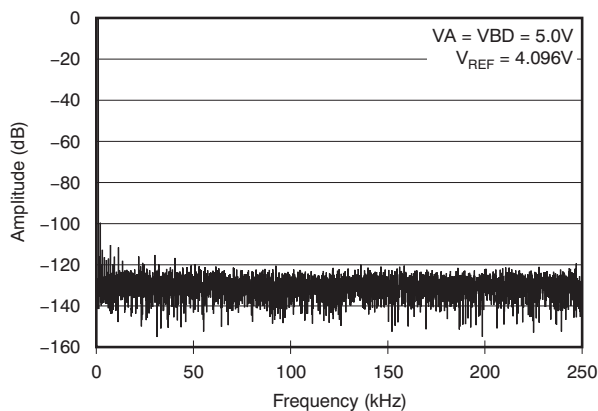


Figure 23.

**FREQUENCY SPECTRUM
(8192 Point FFT, $f_{\text{IN}} = 10.0708\text{kHz}$, -0.2dB)**

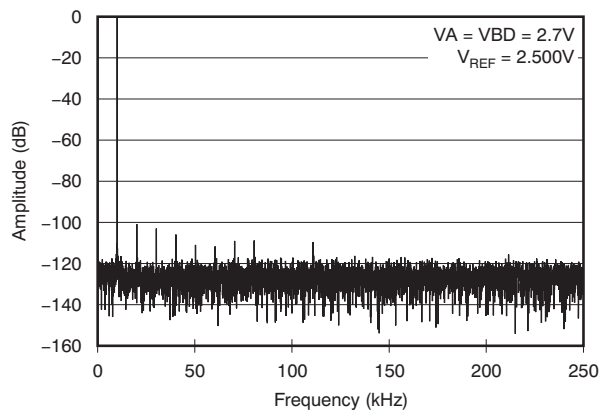


Figure 24.

**FREQUENCY SPECTRUM
(8192 Point FFT, $f_{\text{IN}} = 10.0708\text{kHz}$, -0.2dB)**

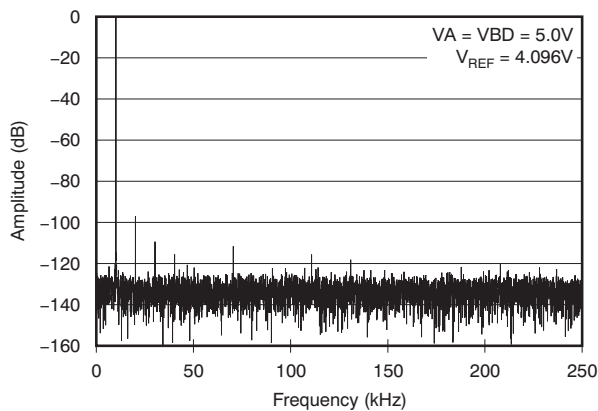


Figure 25.

TYPICAL CHARACTERISTICS: AC Performance (continued)

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF}+ - \text{REF}-) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF}+ - \text{REF}-) = 2.5\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{SCLK}} = 21\text{MHz}$, $f_{\text{SAMPLE}} = 500\text{kSPS}$, and $f_{\text{IN}} = 10\text{kHz}$, unless otherwise noted.

**SIGNAL-TO-NOISE + DISTORTION
vs TEMPERATURE**

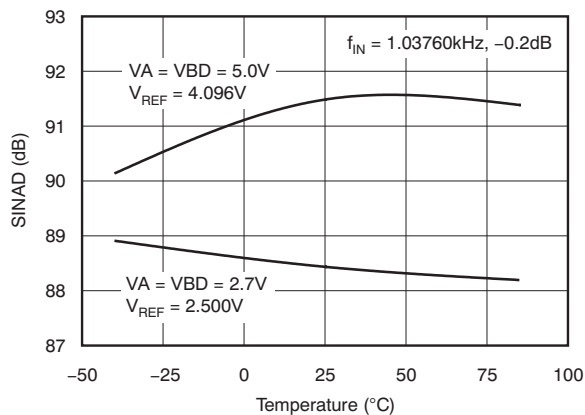


Figure 26.

**SIGNAL-TO-NOISE RATIO
vs INPUT FREQUENCY**

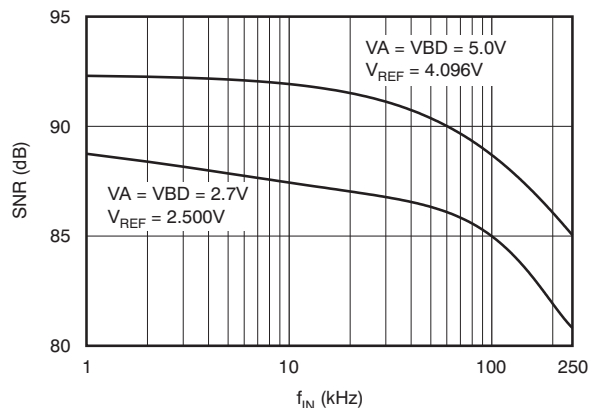


Figure 27.

**TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY**

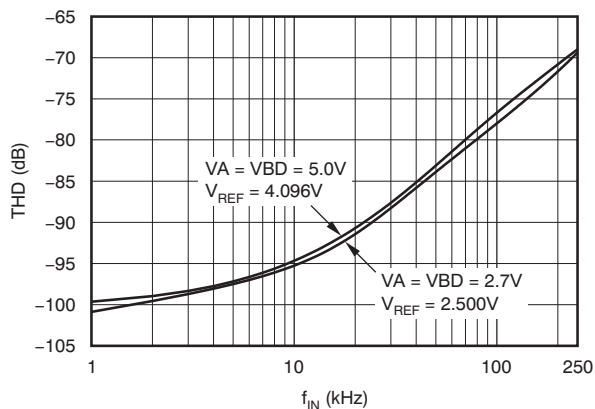


Figure 28.

**SPURIOUS-FREE DYNAMIC RANGE
vs INPUT FREQUENCY**

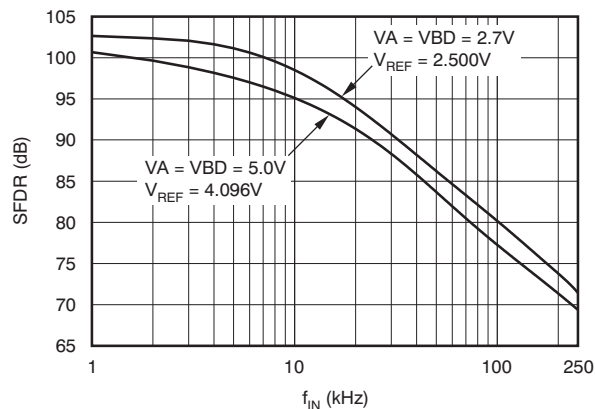


Figure 29.

**SIGNAL-TO-NOISE + DISTORTION
vs INPUT FREQUENCY**

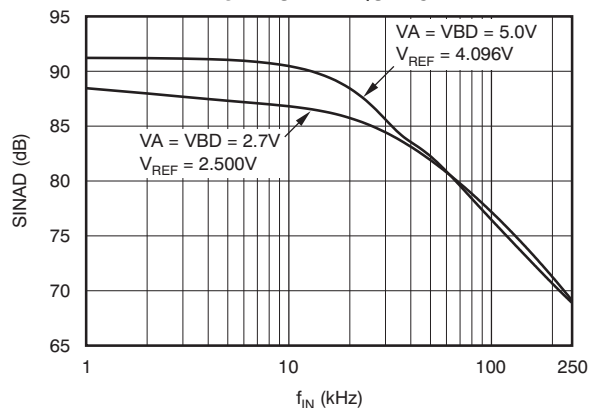


Figure 30.

TYPICAL CHARACTERISTICS: AC Performance (continued)

At $T_A = +25^\circ\text{C}$, $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 4.096\text{V}$ when $V_A = V_{\text{BD}} = 5\text{V}$ or $V_{\text{REF}} (\text{REF+} - \text{REF-}) = 2.5\text{V}$ when $V_A = V_{\text{BD}} = 2.7\text{V}$, $f_{\text{SCLK}} = 21\text{MHz}$, $f_{\text{SAMPLE}} = 500\text{kSPS}$, and $f_{\text{IN}} = 10\text{kHz}$, unless otherwise noted.

**EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY**

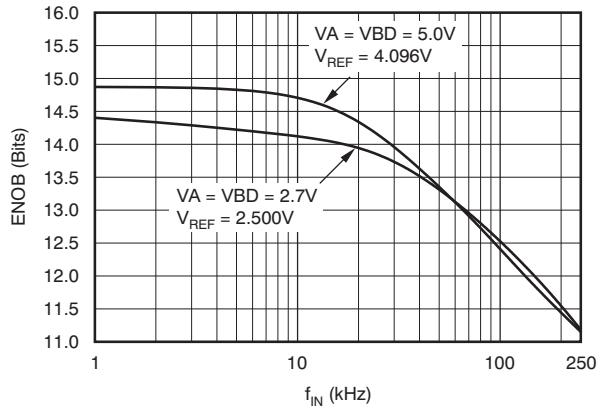


Figure 31.

**POWER-SUPPLY REJECTION RATIO
vs POWER-SUPPLY RIPPLE FREQUENCY**

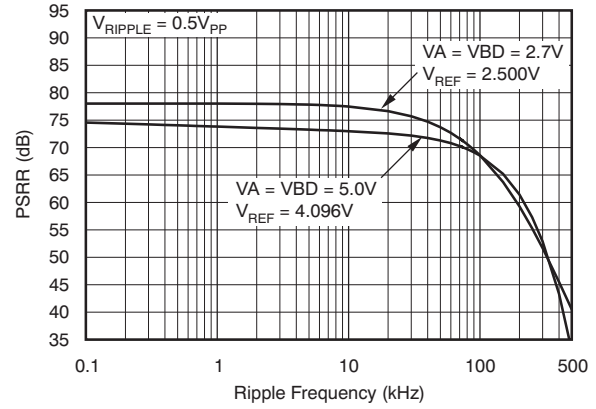


Figure 32.

**CROSSTALK
vs INPUT FREQUENCY**

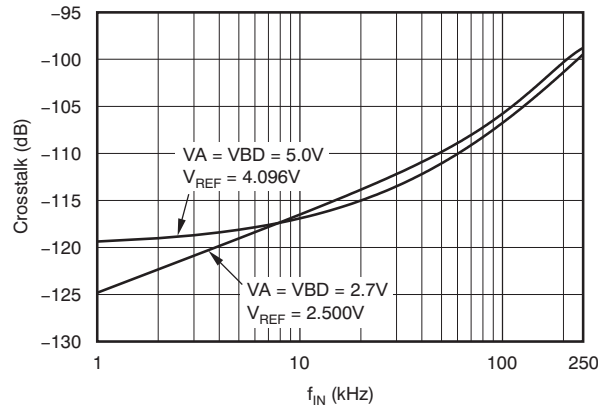


Figure 33.

THEORY OF OPERATION

DESCRIPTION

The ADS8331/32 is a high-speed, low-power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The ADS8331/32 has an internal clock that is used to run the conversion. However, the ADS8331/32 can be programmed to run the conversion based on the external serial clock (SCLK).

The analog input to the ADS8331/32 is provided to two input pins: one of the IN_X input channels and the shared COM pin. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both IN_X and COM inputs are disconnected from any internal function.

The ADS8331 has four analog inputs while the ADS8332 has eight inputs. All inputs share the same common pin, COM. Both the ADS8331 and ADS8332 can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

SIGNAL CONDITIONING

The ADS8331/32 has the flexibility to add signal conditioning between the MUXOUT and ADCIN pins, such as a programmable gain amplifier (PGA) or filter. This feature reduces the system component count and cost because each input channel does not require separate signal conditioning circuits, especially if the source impedance connected to each channel is similar in value.

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the IN_X and COM inputs is captured on the internal capacitor array. The voltage on the COM pin is limited between (AGND – 0.2V) and (AGND + 0.2V). This limitation allows the ADS8331/32 to reject small signals that are common to both the IN_X and COM inputs. The IN_X inputs have a range of –0.2V to ($V_A + 0.2V$). The input span of ($IN_X - COM$) is limited to 0V to V_{REF} .

The peak input current through the analog inputs depends upon a number of factors: reference voltage, sample rate, input voltage, and source impedance. The current flowing into the ADS8331/32 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the maximum input capacitance (45pF) to a 16-bit settling level within the minimum acquisition time (238ns). When the converter goes into hold mode, the input impedance is greater than 1G Ω .

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the IN_X inputs, the COM input, and the input span of ($IN_X - COM$) should be within the limits specified. If these inputs are outside of these ranges, the linearity of the converter may not meet specifications. To minimize noise, low-bandwidth input signals with low-pass filters should be used. Care should be taken to ensure that the output impedance of the sources driving the IN_X and COM inputs are matched, as shown in Figure 34. If this matching is not observed, the two inputs could have different settling times, which may result in an offset error, gain error, and linearity error that change with temperature and input voltage.

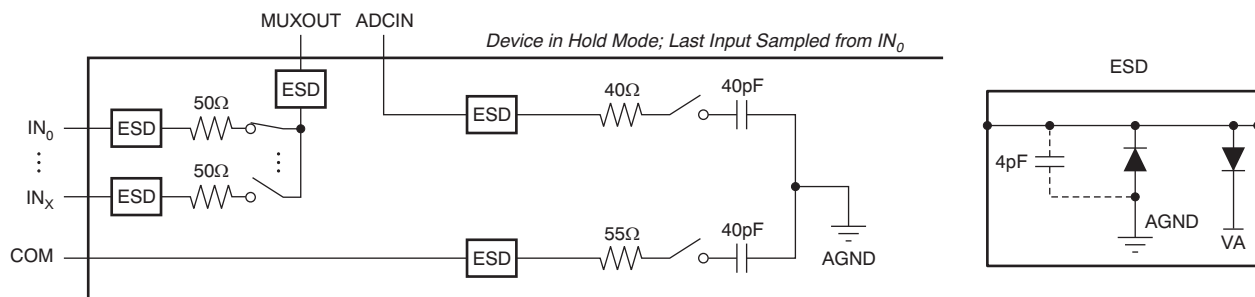


Figure 34. Input Equivalent Circuit

Driver Amplifier Choice

In order to take advantage of the high sample rate offered by the ADS8331/32, the analog inputs to the converter should be driven with low-noise operational amplifiers (op amps), such as the [OPA365](#), [OPA211](#), [OPA827](#), or [THS4031](#). An RC filter is recommended at each of the input channels to low-pass filter noise generated by the input driving sources. These channels can accept unipolar signals with voltages between IN_X and COM in the range of 0V to V_{REF} . If RC filters are not used between the op amps and the input channels, the minimum –3dB bandwidth required by the driving op amps for the sampled signals to settle to within 1/2 LSB of the final voltage can be calculated using [Equation 1](#):

$$f_{-3dB} \geq \frac{(n + 1) \times \ln(2)}{2\pi \times t_{SAMPLE_MIN}} \quad (1)$$

Where:

n = resolution of the converter ($n = 16$ for the ADS8331/32).

t_{SAMPLE_MIN} = minimum acquisition time.

The minimum value of t_{SAMPLE} in the Electrical Characteristics tables is 238ns (3 CCLKs with the internal oscillator at 12.6MHz). Substituting these values for n and t_{SAMPLE_MIN} into [Equation 1](#) shows f_{-3dB} must be at least 7.9MHz. This bandwidth can be relaxed if the acquisition time is increased or an RC filter is added between the driving op amp and the corresponding input channel (refer to Texas Instruments' Application Report [SBAA173](#) and associated references for additional information, available for download at [www.ti.com](#)). The [OPA365](#) used in the source-follower (unity-gain) configuration is shown in [Figure 35](#) with recommended values for the RC filter.

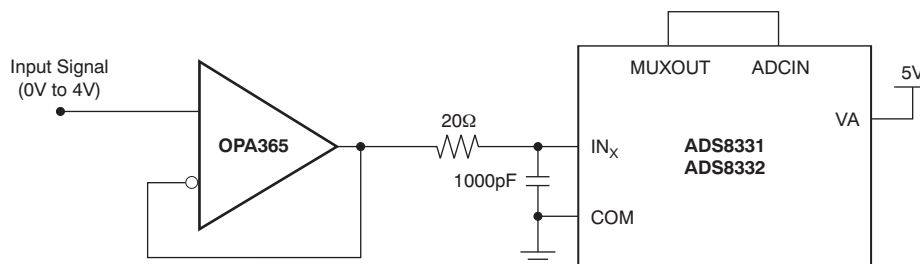


Figure 35. Unipolar Input Drive Configuration

Bipolar to Unipolar Driver

In systems where the input signal is bipolar, op amps such as the [OPA365](#) and [OPA211](#) can be used in the inverting configuration with a dc bias applied to the noninverting input in order to keep the input signal to the ADS8331/32 within its rated operating voltage range. This configuration is also recommended when the ADS8331/32 is used in signal-processing applications where good SNR and THD performance is required. The dc bias can be derived from low-noise reference voltage ICs such as the [REF5025](#) or [REF5040](#). The input configuration shown in [Figure 36](#) is capable of delivering better than 91dB SNR and –99dB THD at an input frequency of 1kHz. If bandpass filters are used to filter the input to the driving op amp, the signal swing at the input of the bandpass filter should be small enough to minimize the distortion introduced by the filter. In these cases, the gain of the circuit shown in [Figure 36](#) can be increased to maintain a large enough input signal to the ADS8331/32 to keep the system SNR as high as possible.

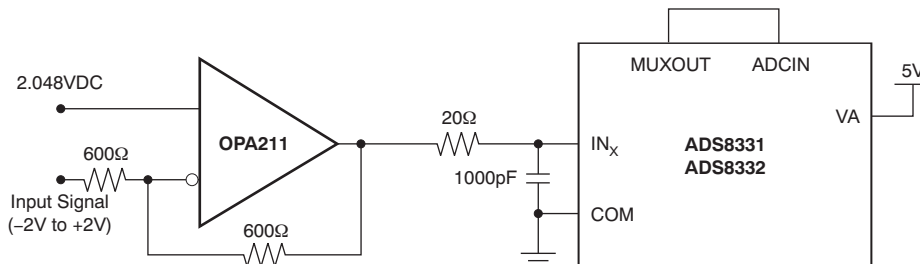


Figure 36. Bipolar Input Drive Configuration

REFERENCE

The ADS8331/32 can operate with an external reference with a range from 1.2V to 4.2V. A clean, low-noise reference voltage on this pin is required to ensure good converter performance. A low-noise band-gap reference such as the [REF5025](#) or [REF5040](#) can be used to drive this pin. A 10µF ceramic bypass capacitor is required between the REF+ and REF– pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Note that the REF– pin should not be connected to the AGND pin of the converter; instead, the REF– pin must be connected to the analog ground plane with a separate via.

CONVERTER OPERATION

The ADS8331/32 has an internal oscillator that can be used as the conversion clock (CCLK) source. The minimum frequency of this oscillator is 10.5MHz. The internal oscillator is only active during the conversion period unless the converter is using Auto-Trigger and/or Auto-Nap modes. The minimum acquisition/sampling time for the ADS8331/32 is 3 CCLKs (250ns with a 12MHz conversion clock), while the minimum conversion time is 18 CCLKs (1500ns with a 12MHz conversion clock).

As shown in [Figure 37](#), the ADS8331/32 can also be programmed to run conversions using the external serial clock (SCLK). This feature allows system designers to achieve system synchronization. Each rising edge of SCLK toggles the state of the conversion clock (CCLK), which reduces the frequency of SCLK by a factor of two before it is used as CCLK. For example, a 21MHz SCLK provides a 10.5MHz CCLK. If the start of a conversion must occur on a specific rising edge of SCLK when the external serial clock is used for the conversion clock (and Manual-Trigger mode is enabled), a minimum setup time of 20ns between the falling edge of $\overline{\text{CONVST}}$ and the rising edge of SCLK must be met. This timing ensures the conversion is completed in 18 CCLKs (36 SCLKs).

The duty cycle of SCLK is not critical, as long as the minimum high and low times (11ns for $V_A = 5.0V$) are satisfied. Because the ADS8331/32 is designed for high-speed applications, a high-frequency serial clock must be supplied to maintain the high throughput of the interface. This requirement can be accomplished if the period of SCLK is at most 1µs when SCLK is used as the conversion clock (CCLK). The 1µs maximum period for SCLK is also set by the leakage of charge from the capacitors in the capacitive digital-to-analog converter (CDAC) block in the ADS8331/32. If SCLK is used as the conversion clock, the SCLK source must have minimal rise/fall times and low jitter to provide the best converter performance.

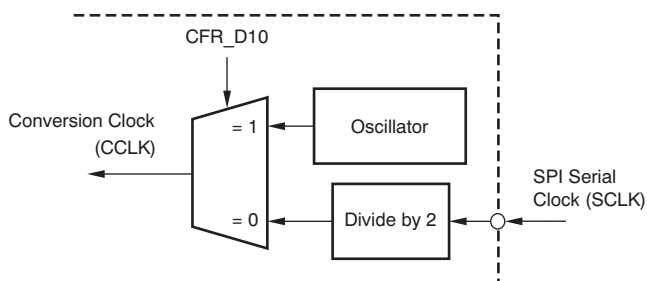


Figure 37. Conversion Clock Source

Manual Channel Select Mode

Manual Channel Select mode is enabled through the Configuration register (CFR) by setting the CFR_D11 bit to '0' (see [Table 5](#)). The acquisition process starts with selecting an input channel. This selection is done by writing the desired channel number to the Command register (CMR); see [Table 4](#) for further details. The associated timing diagram is shown in [Figure 38](#).

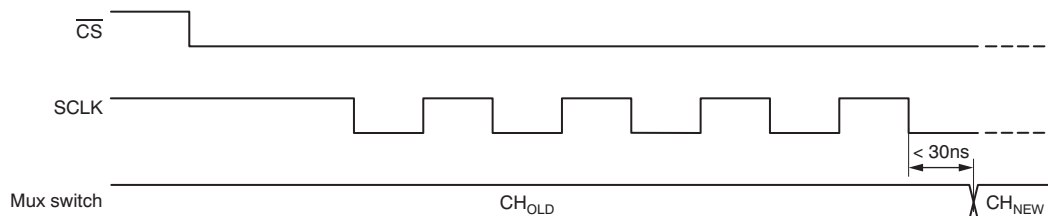


Figure 38. Manual Channel Select Timing

Auto Channel Select Mode

Channel selection can also be done automatically if Auto Channel Select mode (default) is enabled (CFR_D11 = '1'). If the device is programmed for Auto Channel Select mode, then signals from all channels are acquired in a fixed order. In Auto Channel Select mode, the first conversion after entering this mode is always from the channel of the last conversion completed before this mode is enabled. The channels are then sequentially scanned up to and including the last channel (that is, channel 3 for the ADS8331 and channel 7 for the ADS8332) and then back to the channel that started the sequence. For example, if the last channel used in the conversion before enabling Auto Channel Select mode was channel 2, the sequence for the ADS8332 would be: 2, 3, 4, 5, 6, 7, 2, etc., as shown in Figure 39. If the last channel in Manual Channel Select mode happened to be channel 7, the sequence would be: 7, 7, 7, etc. Figure 40 shows when the next channel in the sequence activates during Auto Channel Select mode. This timing allows the next channel to settle before it is acquired. This automatic sequencing stops the cycle after CFR_D11 is set to '0'.

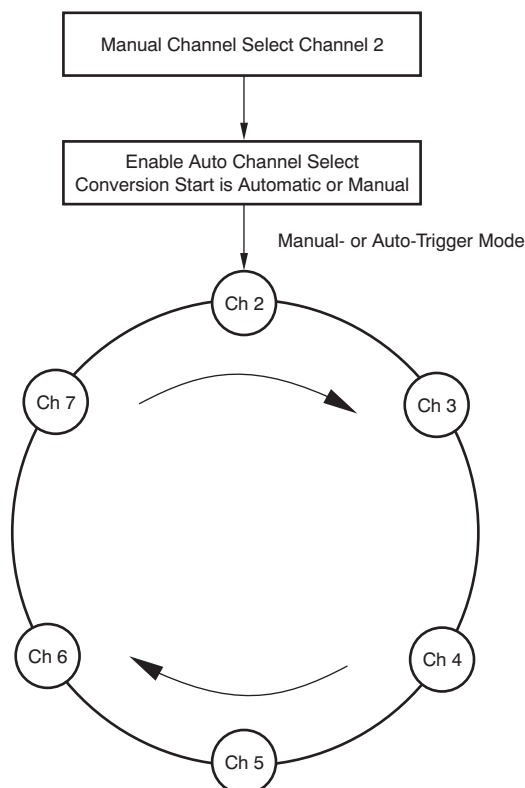


Figure 39. Auto Channel Select for the ADS8332

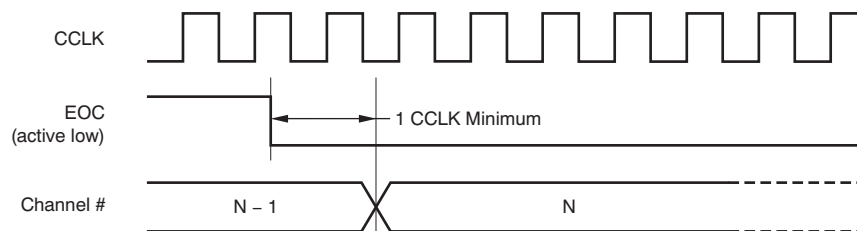


Figure 40. Channel-Number Update in Auto Channel Select Mode Timing

Start of a Conversion

The end of acquisition is the same as the start of a conversion. This process is initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 40ns. After the minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high. $\overline{\text{CONVST}}$ acts independently of FS/CS so it is possible to use one common $\overline{\text{CONVST}}$ for applications that require simultaneous sample/hold with multiple converters. The ADS8331/32 switches from sample to hold mode on the falling edge of the $\overline{\text{CONVST}}$ signal. The ADS8331/32 requires 18 conversion clock (CCLK) cycles to complete a conversion. The conversion time is equivalent to 1500ns with a 12MHz internal clock. The minimum time between two consecutive $\overline{\text{CONVST}}$ signals is 21 CCLKs.

A conversion can also be initiated without using $\overline{\text{CONVST}}$ if the ADS8331/32 is programmed for Auto-Trigger mode (CFR_D9 = '0'). When the converter is configured in this mode, and with CFR_D8 = '0', the next conversion is automatically started three conversion clocks (CCLK) after the end of a conversion. These three conversion clocks (CCLK) are used for the acquisition time. In this case, the time to complete one acquisition and conversion cycle is 21 CCLKs. Table 1 summarizes the different conversion modes.

Table 1. Different Types of Conversion

MODE	SELECT CHANNEL	START CONVERSION
Automatic	Auto Channel Select ⁽¹⁾	Auto-Trigger Mode
	No need to write channel number to CMR. Use internal sequencer for ADS8331/32.	Start a conversion based on conversion clock CCLK
Manual	Manual Channel Select	Manual-Trigger Mode
	Write channel number to CMR	Start a conversion with $\overline{\text{CONVST}}$

(1) Auto channel select should be used with Auto-Trigger mode and TAG bit output enabled.

Manual Channel select with Auto-Trigger mode enabled is generally used when continuous conversions from a single channel are desired. In this mode, cycling the input mux to change the channel requires that conversions are halted by setting the converter to Manual-Trigger mode. When the proper input channel is selected, the converter can be placed back to Auto-Trigger mode to continue continuous conversions from the new channel.

Status Output Pin (EOC/ $\overline{\text{INT}}$)

The status output pin is programmable. It can be used as an EOC output (CFR_D[7:6] = '11') where the low time is equal to the conversion time. When the status pin is programmed as EOC and the polarity is set as active low, the pin works in the following manner: the EOC output goes low immediately following $\overline{\text{CONVST}}$ going low with Manual-Trigger mode enabled. EOC stays low throughout the conversion process and returns high when the conversion has ended. If Auto-Trigger mode is enabled, the EOC output remains high for three conversion clocks (CCLK) after the previous rising edge of EOC.

This status pin can also be used as an interrupt output, $\overline{\text{INT}}$ (CFR_D[7:6] = '10'), which is set low at the end of a conversion, and is brought high (cleared) by the next read cycle. The polarity of this pin, whether used as EOC or $\overline{\text{INT}}$, is programmable through the CFR_D7 bit.

Power-Down Modes and Acquisition Time

There are three power-down modes that reduce power dissipation: Nap, Deep, and Auto-Nap. The first two, Nap and Deep Power-Down modes, are enabled/disabled by bits CFR_D3 and CFR_D2, respectively, in the Configuration register (see Table 5 for details).

Deep Power-Down mode provides maximum power savings. When this mode is enabled, the analog core in the converter is shut down, and the analog supply current falls from 6.6mA (VA = 5.0V) to 1µA in 2µs. The wakeup time from Deep Power-Down mode is 1µs. The device can wake up from Deep Power-Down mode by either disabling this mode, issuing the wakeup command, loading the default value into the CFR, or performing a reset (either with the software reset command, CFR_D0 bit, or the external reset). See Table 4 and Table 5 along with the [Reset Function](#) section for further information.

In Nap Power-Down mode, the bias currents for the analog core of the device are significantly reduced. Because the bias currents are not completely shut off, the ADS8331/32 can wake up from this power-down mode much faster than from Deep Power-Down mode. After Nap Power-Down mode is enabled, the analog supply current falls from 6.6mA (VA = 5.0V) to 0.39mA in 200ns. The wakeup time from this mode is three conversion clock cycles (CCLK). The device can wake up from Nap Power-Down mode in the same manner as waking up from Deep Power-Down mode.

The third power-down mode, Auto-Nap, is enabled/disabled by bit CFR_D4 in the Configuration register (see Table 5 for details). Once this mode is enabled, the device is controlled by the digital core logic on the chip. The device is automatically placed into Nap Power-Down mode after the next end of conversion (EOC). The analog supply current falls from 6.6mA (VA = 5.0V) to 0.39mA in 200ns. A conversion start wakes up the device in three conversion clock cycles. Issuing the wake-up command, loading the default value into the CFR, disabling Auto-Nap Power-Down mode, issuing a manual channel select command, or resetting the device can wake the ADS8331/32 from Auto-Nap Power-Down mode. A comparison of the three power-down modes is listed in Table 2.

Table 2. Comparison of Power-Down Modes

TYPE OF POWER-DOWN	POWER CONSUMPTION (VA = 5.0V)	POWER-DOWN BY:	POWER-DOWN TIME	WAKEUP BY:	WAKEUP TIME	ENABLE
Normal operation	6.6mA	—	—	—	—	—
Deep power-down	1µA	Setting CFR_D2	2µs	Wakeup command 1011b	1µs	Set CFR_D2
Nap power-down	0.39mA	Setting CFR_D3	200ns	Wakeup command 1011b	3 CCLKs	Set CFR_D3
Auto-Nap power-down	0.39mA	EOC (end of conversion)	200ns	CONVST, any channel select command, default command 1111b, or wakeup command 1011b.	3 CCLKs	Set CFR_D4

The default acquisition time is three conversion clock (CCLK) cycles. Figure 41 shows the timing diagram for CONVST, EOC, and auto-nap power-down signals in Manual-Trigger mode. As shown in the diagram, the device wakes up after a conversion is triggered by the CONVST pin going low. However, a conversion is not yet started at this time. The conversion start signal to the analog core of the chip is internally generated no less than six conversion clock (CCLK) cycles later, to allow at least three CCLKs for wake up and three CCLKs for acquisition. The ADS8331/32 enters Nap Power-Down mode one conversion cycle after the end of conversion (EOC).

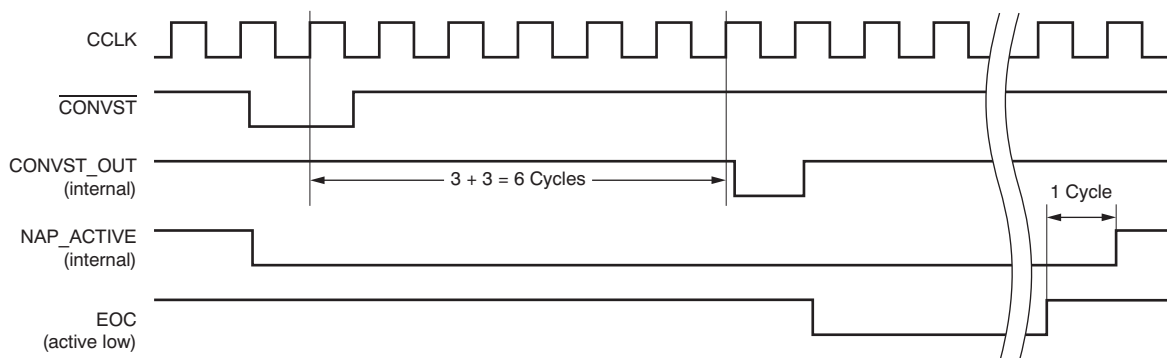


Figure 41. Timing for CONVST, EOC, and Auto-Nap Power-Down Signals in Manual-Trigger Mode (Three Conversion Clock Cycles for Acquisition)

The ADS8331/32 can support sampling rates of up to 500kSPS in Auto-Trigger mode. This rate is selectable by programming the CFR_D8 bit in the Configuration register. In 500kSPS mode, consecutive conversion start pulses to the analog core are generated 21 conversion clock cycles apart. In 250kSPS mode, consecutive conversion-start pulses are 42 conversion clock cycles apart. The Nap and Deep Power-Down modes are available with either sampling rate; however, Auto-Nap mode is available only with a sampling rate of 250kSPS when Auto-Trigger mode is enabled. The analog core cannot be powered down when the Auto-Nap mode sampling rate is 500kSPS because at that rate, there is no period of time when the analog core is not actively being used.

Figure 42 shows the timing diagram for conversion start and auto-nap power-down signals for a 250kSPS sampling rate in Auto-Trigger mode. For a 16-bit ADC output word, consecutive new conversion start pulses are generated $2 \times (18 + 3)$ cycles apart. NAP_ACTIVE (the signal to power down the analog core in Nap and Auto-Nap modes) goes low six $(3 + 3)$ conversion clock cycles before the conversion start falling edge, thus powering up the analog core. It takes three conversion clock cycles after NAP_ACTIVE goes low to power up the analog core. The analog core is powered down a cycle after the end of a conversion. For a 16-bit ADC with a 500kSPS sampling rate and three conversion clock cycle sampling, consecutive conversion start pulses are generated 21 conversion clock cycles apart.

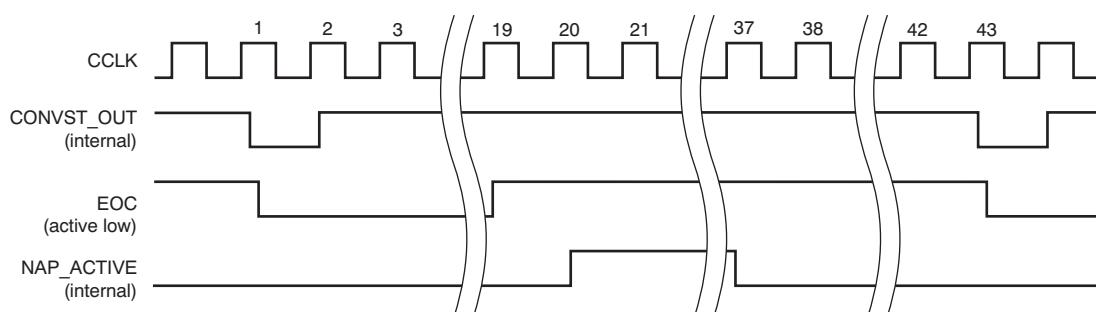


Figure 42. Timing for Conversion Start and Auto-Nap Power-Down Signals in Auto-Trigger Mode (250kSPS Sampling and Three Conversion Clock Cycles for Acquisition)

Timing diagrams for reading from the ADS8331/32 with various trigger and power-down modes are shown in Figure 43 through Figure 45. The total (acquisition + conversion) times for the different trigger and power-down modes are listed in Table 3.

Table 3. Total Acquisition + Conversion Times

MODE	ACQUISITION + CONVERSION TIME
Auto-Trigger at 500kSPS	= 21 CCLK
Manual-Trigger	≥ 21 CCLK
Manual-Trigger with Deep Power-Down	≥ 4 SCLK + 1μs + 3 CCLK + 18 CCLK + 16 SCLK + 2μs
Manual-Trigger with Nap Power-Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK + 200ns
Manual-Trigger with Auto-Nap Power-Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200ns (using wakeup to resume)
	≥ 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200ns (using $\overline{\text{CONVST}}$ to resume)

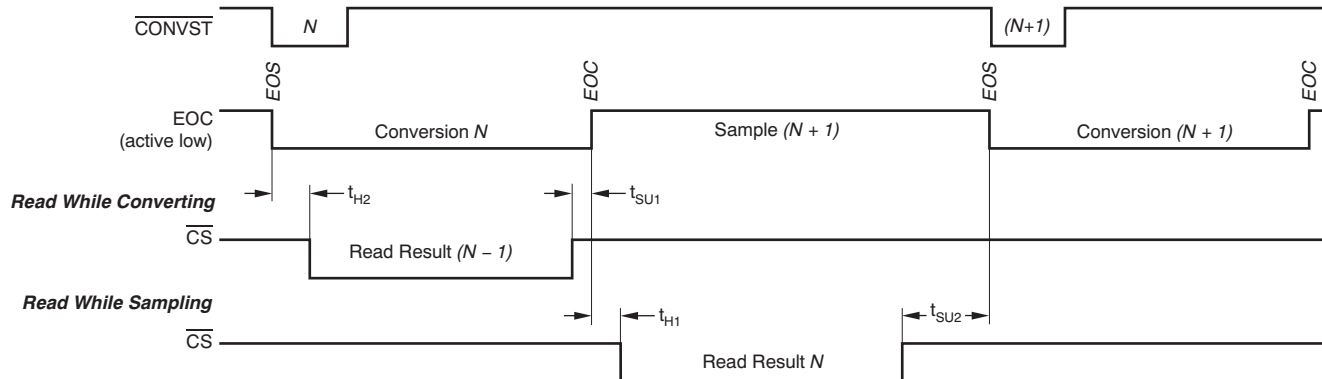
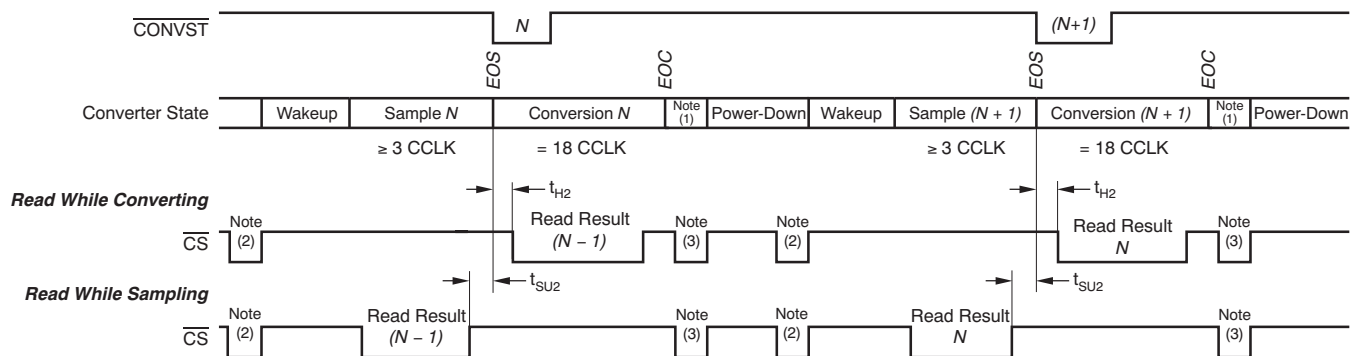


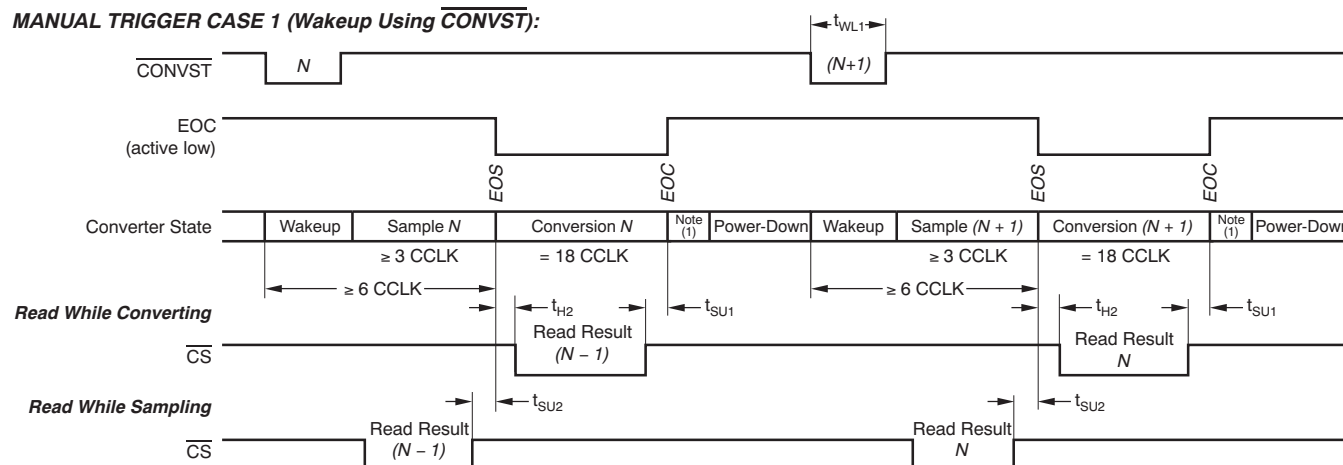
Figure 43. Read While Converting vs Read While Sampling (Manual-Trigger Mode)



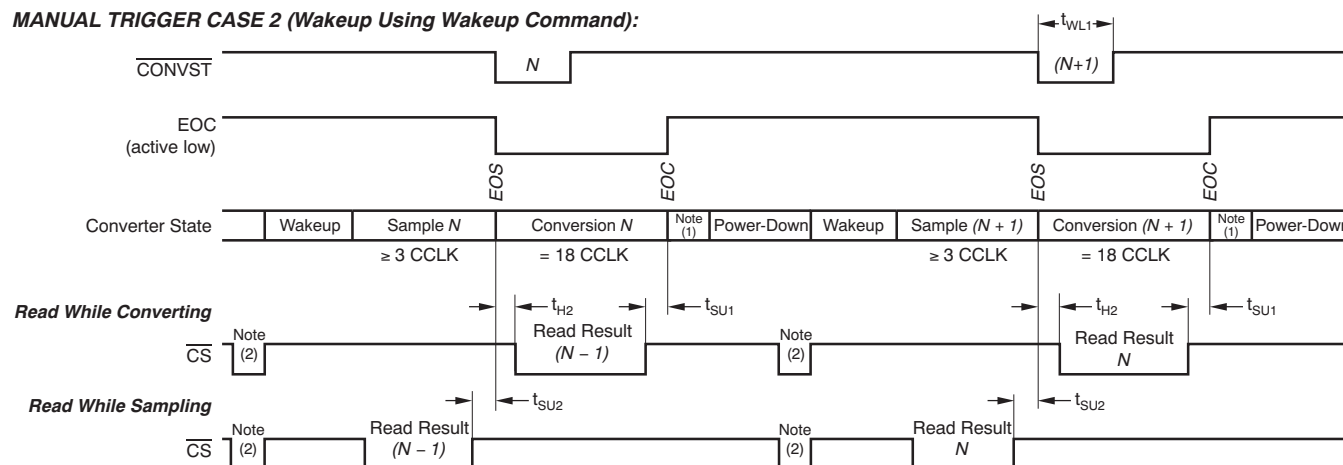
- (1) Converter is in acquisition mode between end of conversion and activation of Nap or Deep Power-Down mode.
- (2) Command on SDI pin to wake up converter (minimum of four SCLKs).
- (3) Command on SDI pin to place converter into Nap or Deep Power-Down mode (minimum of 16 SCLKs).

Figure 44. Read While Converting vs Read While Sampling with Nap or Deep Power-Down (Manual-Trigger Mode)

MANUAL TRIGGER CASE 1 (Wakeup Using CONVST):



MANUAL TRIGGER CASE 2 (Wakeup Using Wakeup Command):



- (1) Time between end of conversion and Nap Power-Down mode is 1 CCLK.
- (2) Command on SDI to wake up converter (minimum of four SCLKs).

Figure 45. Read While Converting vs Read While Sampling with Auto-Nap Power-Down

DIGITAL INTERFACE

The serial interface is designed to accommodate the latest high-speed processors with an SCLK frequency of up to 40MHz ($V_A = V_{BD} = 5.0V$). Each cycle starts with the falling edge of $\overline{FS/CS}$. The internal data register content, which is made available to the output register at the end of conversion, is presented on the SDO output pin on the falling edge of $\overline{FS/CS}$. The first bit is the most significant bit (MSB). The output data bits are valid on the falling edge of SCLK with the t_{D2} delay (see the Timing Characteristics) so that the host processor can read the data on the falling edge. Serial data input is also read on the falling edge of SCLK.

The complete serial I/O cycle starts after the falling edge of $\overline{FS/CS}$ and ends 16 falling edges of SCLK later (see NOTE). The serial interface works with CPOL = '1', CPHA = '0'. This setting means the falling edge of $\overline{FS/CS}$ may fall while SCLK is high. The same timing relaxation applies to the rising edge of $\overline{FS/CS}$ where SCLK may be high or low as long as the last SCLK falling edge happens before the rising edge of $\overline{FS/CS}$.

NOTE

There are cases where a cycle can be anywhere from 4 SCLKs up to 24 SCLKs, depending on the read mode combination. See Table 4 for details.

Internal Register

The internal register consists of two parts: four bits for the Command register (CMR) and 12 bits for the Configuration register (CFR).

Table 4. Command Set Defined by Command Register (CMR)⁽¹⁾

D[15:12]	HEX	COMMAND	D[11:0]	WAKE UP FROM AUTO- NAP	MINIMUM SCLKs REQUIRED	R/W
0000b	0h	Select analog input channel 0	Don't care	Y	4	W
0001b	1h	Select analog input channel 1	Don't care	Y	4	W
0010b	2h	Select analog input channel 2	Don't care	Y	4	W
0011b	3h	Select analog input channel 3	Don't care	Y	4	W
0100b	4h	Select analog input channel 4 ⁽²⁾	Don't care	Y	4	W
0101b	5h	Select analog input channel 5 ⁽²⁾	Don't care	Y	4	W
0110b	6h	Select analog input channel 6 ⁽²⁾	Don't care	Y	4	W
0111b	7h	Select analog input channel 7 ⁽²⁾	Don't care	Y	4	W
1000b	8h	Reserved	Reserved	—	—	—
1001b	9h	Reserved	Reserved	—	—	—
1010b	Ah	Reserved	Reserved	—	—	—
1011b	Bh	Wake up	Don't care	Y	4	W
1100b	Ch	Read CFR	Don't care	—	16	R
1101b	Dh	Read data	Don't care	—	16	R
1110b	Eh	Write CFR	CFR Value	—	16	W
1111b	Fh	Default mode (load CFR with default value)	Don't care	Y	4	W

(1) The first four bits from SDO after the falling edge of $\overline{FS/CS}$ are the four MSBs from the previous conversion result. The next 12 bits from SDO are the contents of the CFR.

(2) These commands apply only to the ADS8332; they are reserved (not available) for the ADS8331.

WRITING TO THE CONVERTER

There are two different types of writes to the register: a 4-bit write to the CMR and a full 16-bit write to the CMR plus CFR. The command set is listed in [Table 4](#) and the configuration register map is listed in [Table 5](#). A simple command requires only four SCLKs; the write takes effect on the fourth falling edge of SCLK. A 16-bit write or read takes at least 16 SCLKs (see [Table 7](#) for exceptions that require more than 16 SCLKs).

Configuring the Converter and Default Mode

The converter can be configured with command 1110b (write to the CFR) or command 1111b (default mode). A write to the CFR requires a 4-bit command followed by 12 bits of data. A 4-bit command takes effect on the fourth falling edge of SCLK. A write to the CFR takes effect on the 16th falling edge of SCLK.

The CFR default value for each bit is '1'. The default values are applied to the CFR after issuing command 1111b or when the device is reset with a power-on reset (POR), software reset, or external reset using the **RESET** pin (see the [Reset Function](#) section).

The communication protocol of the ADS8331/32 is full duplex. That is, data are transmitted to and from the device simultaneously. For example, the input mux channel can be changed via the SDI pin while data are being read via the SDO pin. All commands, except *Read CFR*, output conversion data on the SDO pin. If a *Read CFR* command is issued, the *Read Data* command can then be used to read back the conversion result.

READING THE CONFIGURATION REGISTER

The host processor can read back the value programmed in the CFR by issuing command 1100b. The timing is similar to reading a conversion result except **CONVST** is not used. There is also no activity on the **EOC/INT** pin. The CFR value readback contains the first four bits (MSBs) of the previous conversion data plus the 12-bit CFR contents.

Table 5. Configuration Register (CFR) Map

CFR SDI BIT (Default = FFFh)	DEFINITION	BIT = '0'	BIT = '1'
D11	Channel select mode	Manual channel select enabled. Use channel select commands to access a desired channel.	Auto channel select enabled. Channels are sampled and converted sequentially until the cycle after this bit is set to 0.
D10	Conversion clock (CCLK) source select	Conversion clock (CCLK) = SCLK/2	Conversion clock (CCLK) = internal OSC
D9	Trigger (conversion start) select: start conversion at the end of sampling (EOS). If D9 = '0' and D8 = '0', the D4 setting is ignored.	Auto-Trigger: conversions automatically start three conversion clocks after EOC at 500kSPS	Manual-Trigger: conversions manually start on falling edge of CONVST
D8	Sample rate for Auto-Trigger mode	500kSPS (21 CCLKs)	250kSPS (42 CCLKs)
D7	Pin 10 polarity select when used as an output (EOC/INT)	EOC/INT active high	EOC/INT active low
D6	Pin 10 function select when used as an output (EOC/INT)	Pin used as INT	Pin used as EOC
D5	Pin 10 I/O select for daisy-chain mode operation	Pin 10 is used as CDI input (daisy-chain mode enabled)	Pin 10 is used as EOC/INT output
D4	Auto-Nap Power-Down enable/disable. This bit setting is ignored if D9 = '0' and D8 = '0'.	Auto-Nap Power-Down mode enabled (not activated)	Auto-Nap Power-Down mode disabled
D3	Nap Power-Down. This bit is set to 1 automatically by wake-up command.	Nap Power-Down enabled	Nap Power-Down disabled (resume normal operation)
D2	Deep Power-Down. This bit is set to 1 automatically by wake-up command.	Deep Power-Down enabled	Deep Power-Down disabled (resume normal operation)
D1	TAG bit output enable	TAG bit output disabled	TAG bit output enabled. TAG bits appear after conversion data
D0	Software reset	System reset, returns to '1' automatically	Normal operation

READING THE CONVERSION RESULT

The conversion result is available to the input of the output data register (ODR) at EOC and presented to the output of the output register at the next falling edge of FS/CS. The host processor can then shift the data out via the SDO pin at any time except during the quiet zone. This duration is 20ns before and 20ns after the end of sampling (EOS) period. End of sampling (EOS) is defined as the falling edge of CONVST when Manual-Trigger mode is used or the end of the third conversion clock (CCLK) after EOC if Auto-Trigger mode is used.

The falling edge of FS/CS should not be placed at the precise moment at the end of a conversion (by default when EOC goes high). Otherwise, the data could be corrupt. If FS/CS is placed before the end of a conversion, the previous conversion result is read. If FS/CS is placed after the end of a conversion, the current conversion result is read.

The conversion result is 16-bit data in straight binary format as shown in Table 6. Generally 16 SCLKs are necessary, but there are exceptions when more than 16 SCLKs are required (see Table 7). Data output from the serial output (SDO) is left-adjusted MSB first. The trailing bits are filled with three TAG bits first (if enabled) plus all '0's. SDO remains low until FS/CS is brought high again.

SDO is active when FS/CS is low. The rising edge of FS/CS 3-states the SDO output.

NOTE

Whenever SDO is not in 3-state (that is, when FS/CS is low and SCLK is running), a portion of the conversion result is output at the SDO pin. The number of bits depends on how many SCLKs are supplied. For example, a manual channel select command cycle requires 4 SCLKs. Therefore, four MSBs of the conversion result are output at SDO. The exception is when SDO outputs all '1's during the cycle immediately after any reset (POR, software reset, or external reset).

If SCLK is used as the conversion clock (CCLK) and a continuous SCLK is used, it is not possible to clock out all 16 bits from SDO during the sampling time (6 SCLKs) because of the quiet zone requirement. In this case, it is better to read the conversion result during the conversion time (36 SCLKs or 48 SCLKs in Auto-Nap mode).

Table 6. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
		STRAIGHT BINARY	
Full-scale range	V_{REF}		
Least significant bit (LSB)	$V_{REF}/65536$	BINARY CODE	HEX CODE
Full-scale	$V_{REF} - 1 \text{ LSB}$	1111 1111 1111 1111	FFFF
Midscale	$V_{REF}/2$	1000 0000 0000 0000	8000
Midscale – 1 LSB	$V_{REF}/2 - 1 \text{ LSB}$	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

TAG Mode

The ADS8331/32 includes a TAG feature that can be used to indicate which channel sourced the converted result. If TAG mode is enabled, three address bits are added after the LSB of the conversion data is read out from SDO to indicate which channel corresponds to the result. These address bits are '000' for channel 0, '001' for channel 1, '010' for channel 2, '011' for channel 3, '100' for channel 4, '101' for channel 5, '110' for channel 6, and '111' for channel 7. The converter requires at least 19 SCLKs when TAG mode is enabled in order to transfer the 16-bit conversion result and the three TAG bits.

Daisy-Chain Mode

The ADS8331/32 can operate as a single converter or in a system with multiple converters. System designers can take advantage of the simple, high-speed, SPI-compatible serial interface by cascading converters in a single chain when multiple converters are used. The CFR_D5 bit in the Configuration register is used to reconfigure the EOC/INT status pin as the chain data input (CDI) pin, a secondary serial data input, for the conversion result from an upstream converter. This configuration is called *daisy-chain mode* operation. A typical connection of three converters in daisy-chain mode is shown in Figure 46.

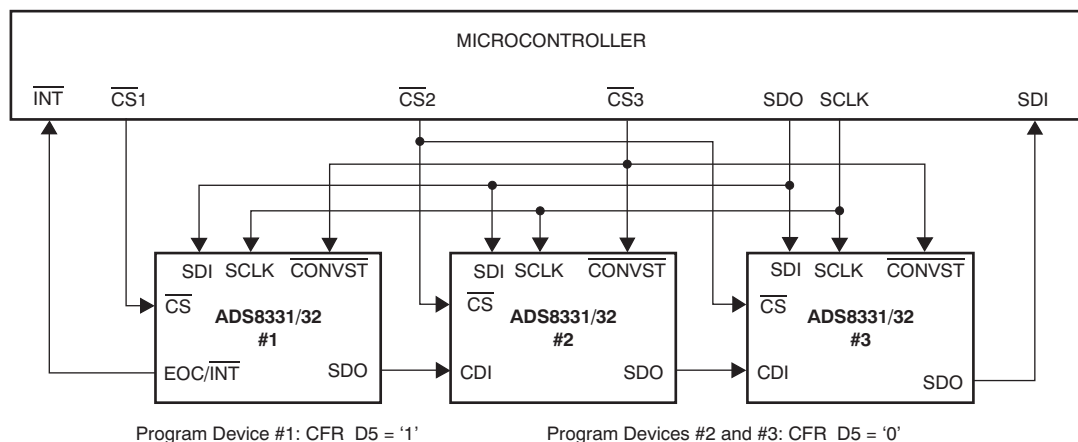


Figure 46. Multiple Converters Connected Using Daisy-Chain Mode

When multiple converters are used in daisy-chain mode, the first converter is configured in regular mode while the rest of the converters downstream are configured in daisy-chain mode. When a converter is configured in daisy-chain mode, the CDI input data go straight to the output register. Therefore, the serial input data passes through the converter with either a 16 SCLK (if the TAG feature is disabled) or 24 SCLK delay, as long as $\overline{\text{CS}}$ is active. See Figure 47 for detailed timing. In this timing diagram, the conversion in each converter is performed simultaneously.

Manual Trigger, Read While Sampling
(Use internal CCLK, EOC active low, and TAG mode disabled)

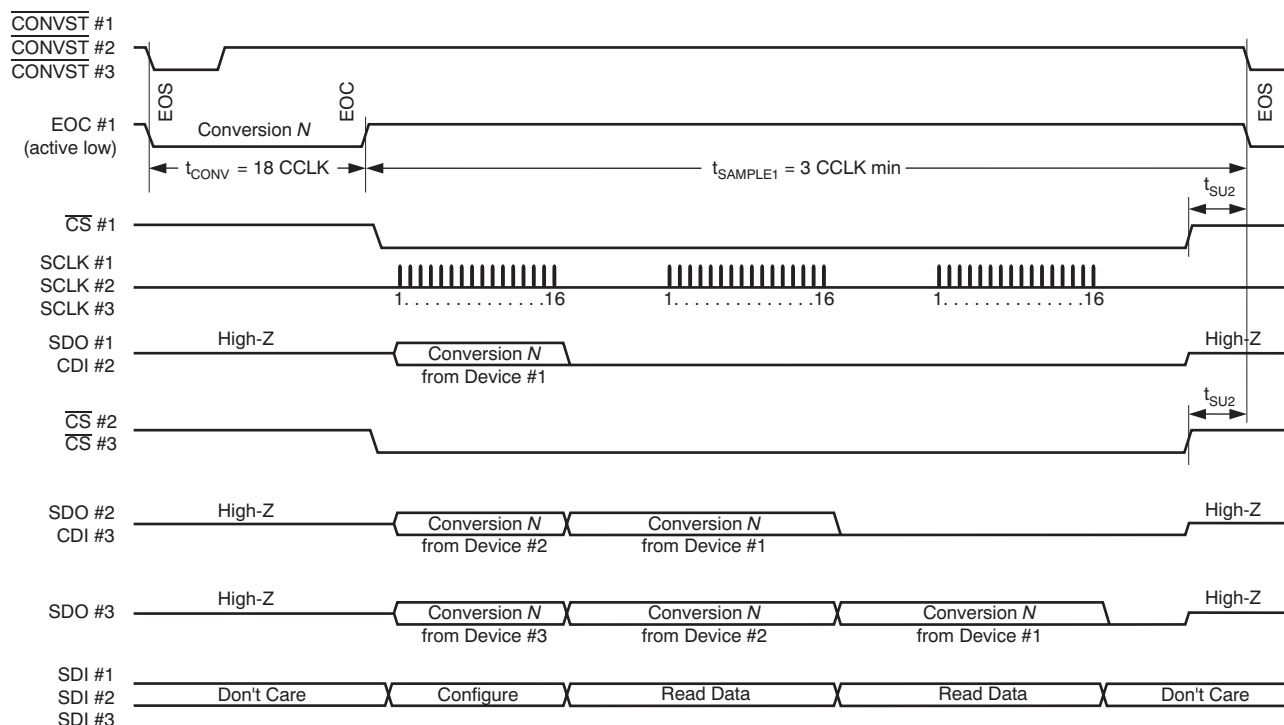


Figure 47. Simplified Dasiy-Chain Mode Timing with Shared $\overline{\text{CONVST}}$ and Continuous $\overline{\text{CS}}$

The multiple $\overline{\text{CS}}$ signals must be handled with care when the converters are operating in daisy-chain mode. The different chip select signals must be low for the entire data transfer (in this example, 48 bits for three conversions). The first 16-bit word after the falling chip select is always the data from the chip that received the chip select signal.

Case 1: If chip select is not toggled (\overline{CS} stays low), the next 16 bits of data are from the upstream converter, and so on. This configuration is shown in Figure 47.

Case 2: If the chip select is toggled during a daisy-chain mode data transfer cycle, as illustrated in Figure 48, the same data from the converter are read out again and again in all three discrete 16-bit cycles. This state is **not** a desired result.

Manual Trigger, Read While Sampling

(Use internal CCLK, EOC active low, and TAG mode disabled)

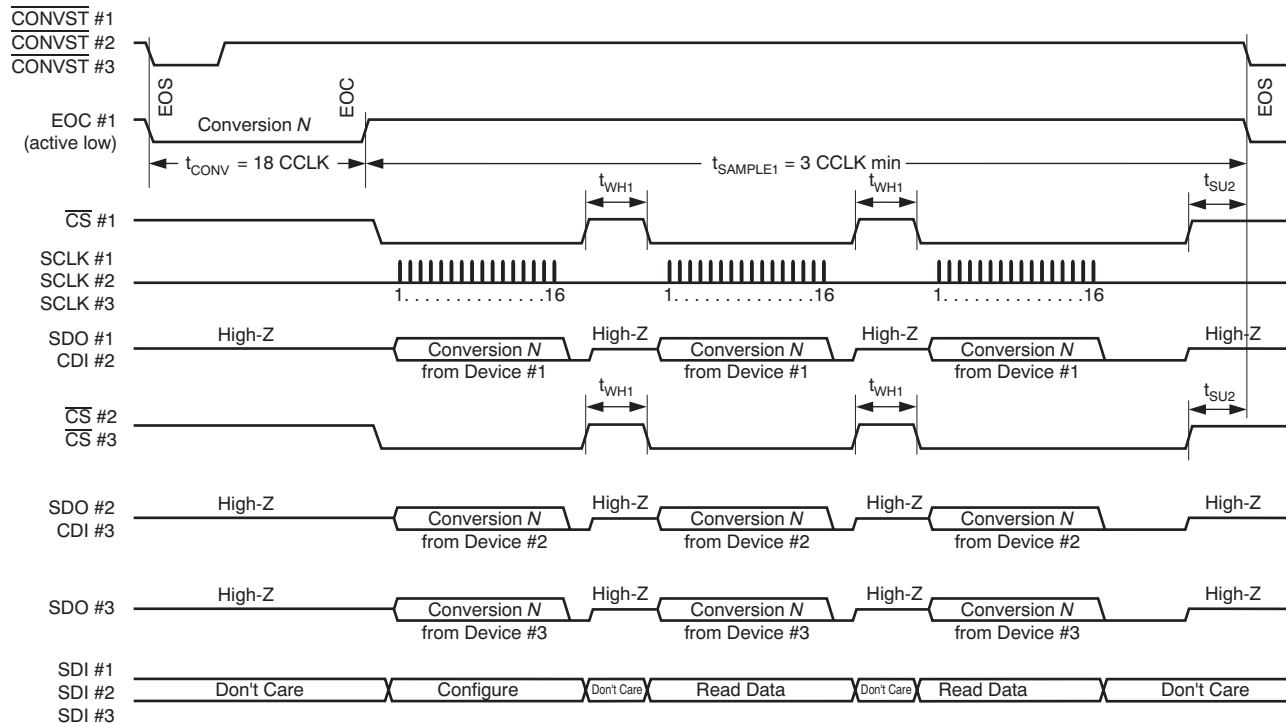
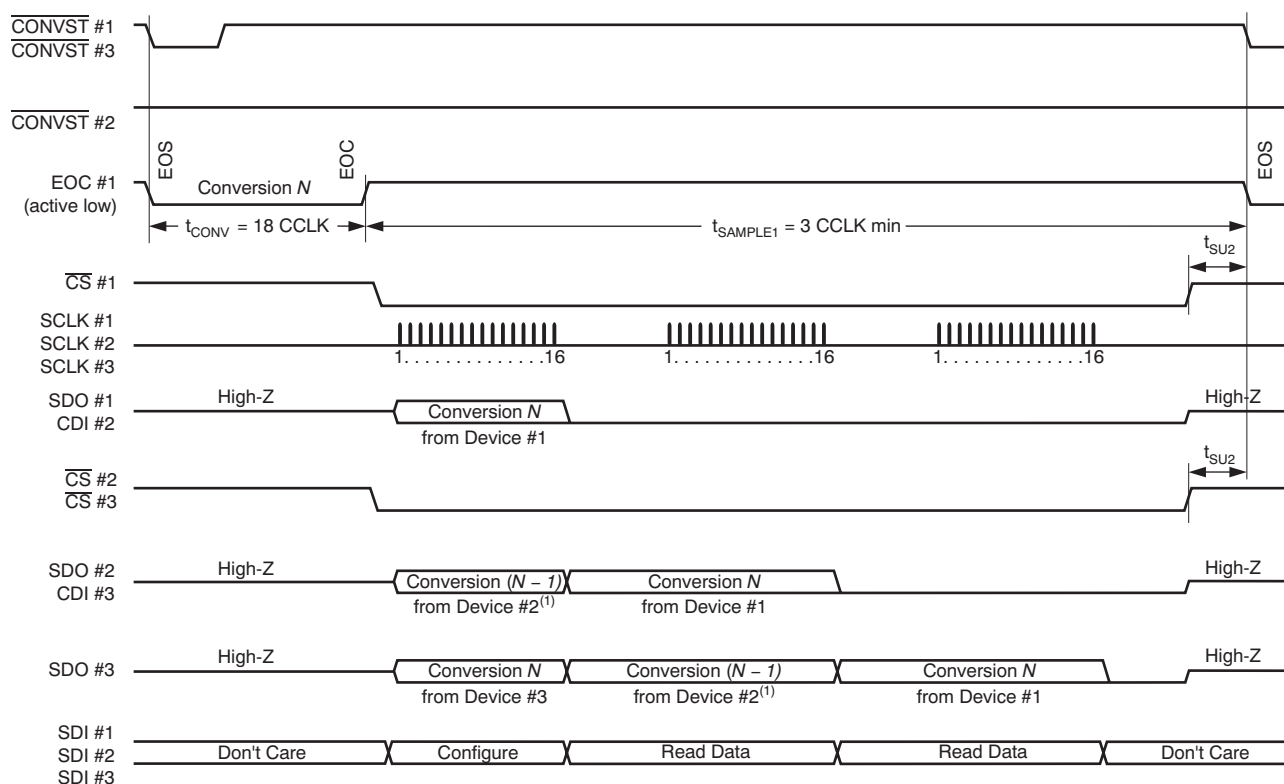


Figure 48. Simplified Daisy-Chain Mode Timing with Shared \overline{CONVST} and Noncontinuous \overline{CS}

Figure 49 shows a slightly different scenario where $\overline{\text{CONVST}}$ is not shared with the second converter. Converters #1 and #3 have the same $\overline{\text{CONVST}}$ signal. In this case, converter #2 simply passes previous conversion data downstream.

Manual Trigger, Read While Sampling
(Use internal CCLK, EOC active low, and TAG mode disabled)



(1) Data from device #2 is from previous conversion.

Figure 49. Simplified Daisy-Chain Mode Timing with Separate $\overline{\text{CONVST}}$ and Continuous $\overline{\text{CS}}$

The number of SCLKs required for a serial read cycle depends on the combination of different read modes, TAG mode, daisy-chain mode, and the manner in which a channel is selected (for example, Auto Channel Select mode). The required number of SCLKs for different readout modes are listed in Table 7.

Table 7. Required SCLKs For Different Readout Mode Combinations

DAISY-CHAIN MODE CFR_D5	TAG MODE CFR_D1	NUMBER OF SCLK CYCLES PER SPI READ	TRAILING BITS
1	0	16	None
1	1	≥ 19	TAG bits plus up to 5 zeros
0	0	16	None
0	1	24	TAG bits plus 5 zeros

SCLK skew between converters in a daisy-chain configuration can affect the maximum frequency of SCLK. The skew can also be affected by supply voltage and loading. It may be necessary to slow down the SCLK when the devices are configured in daisy-chain mode.

RESET FUNCTION

The ADS8331/32 can be reset with three different methods: internal POR, software reset, and external reset using the $\overline{\text{RESET}}$ pin.

The internal POR circuit is activated when power is initially applied to the converter. This internal circuit eliminates the need for commands to be sent to the converter after power-on in order to set the default mode of operation (see the [Power-On Sequence Timing](#) section for further details).

Software reset can be used to place the converter in the default mode by setting the CFR_D0 bit to '0' in the Configuration register (see [Table 5](#)). This bit is automatically returned to '1' (default) after the converter is reset. This reset method is useful in systems that cannot dedicate a separate control signal to the $\overline{\text{RESET}}$ pin. In these situations, the RESET pin must be connected to VBD in order for the ADS8331/32 to operate properly.

If communication in the system becomes corrupted and a software reset cannot be issued, the $\overline{\text{RESET}}$ pin can be used to reset the device manually. In order to reset the device and return the device to default mode, this pin must be held low for a minimum of 25ns.

After the ADS8331/32 detects a reset condition, the minimum time before the device can be reconfigured by $\overline{\text{FS/CS}}$ going low and data clocking in on SDI is 2 μ s.

APPLICATION INFORMATION

TYPICAL CONFIGURATION EXAMPLE

Figure 50 illustrates a typical circuit configuration using the ADS8331/32.

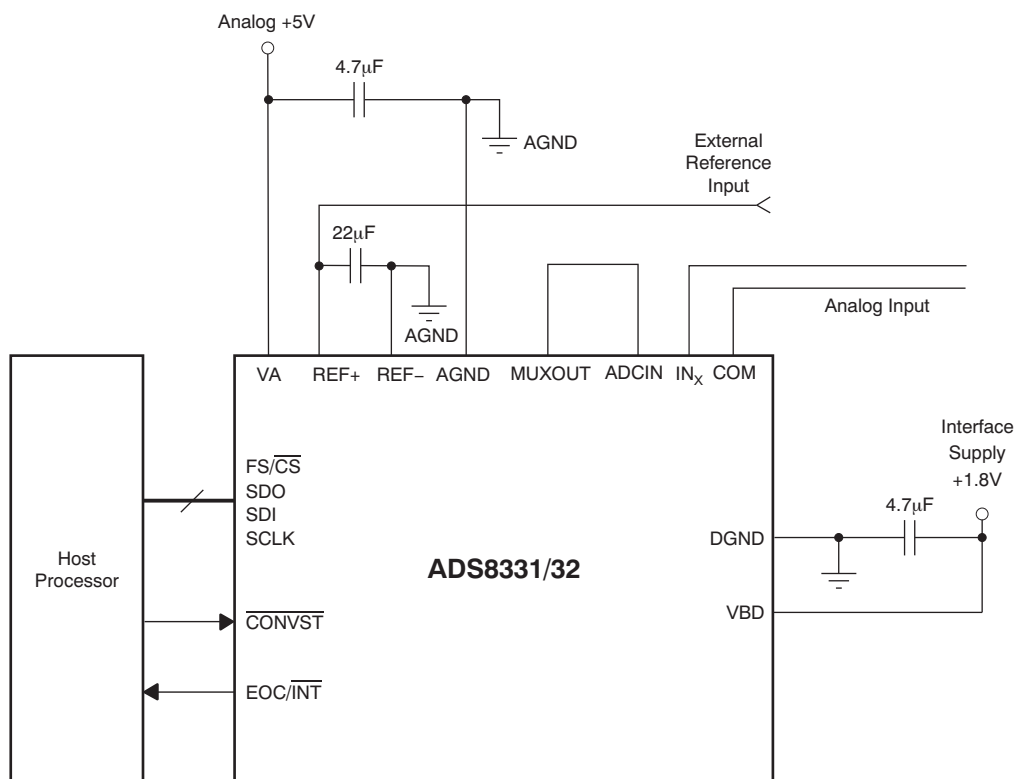


Figure 50. Typical Circuit Configuration

POWER-ON SEQUENCE TIMING

During power-on of the ADS8331/32, the digital interface supply voltage (VBD) should not exceed the analog supply voltage (VA). This condition is specified in the *Power-Supply Requirements* section of the Electrical Characteristics tables. If the analog and digital interface supplies for the converter are not generated by a single voltage source, it is recommended to power-on the analog supply and wait for it to reach its final value before the digital interface supply is activated. Furthermore, the voltages applied to the analog input pins (IN_x, ADCIN) and digital input pins (RESET, FS/CS, SCLK, SDI, and CONVST) should not exceed the voltages on VA and VBD, respectively, during the power-on sequence. This requirement prevents these input pins from powering the ADS8331/32 through the ESD protection diodes/circuitry, and causing an increase in current consumption, until both supplies are fully powered (see the Electrical Characteristics and Figure 34 for further details).

Communication with the ADS8331/32, such as initiating a conversion with CONVST or writing to the Configuration register, should not occur for a minimum of 2µs after the analog and digital interface supplies have finished the power-on sequence and reached the respective final values in the system. This time is required for the internal POR to activate and place the digital core of the device into the default mode of operation. This minimum delay time must also be adhered to whenever a reset condition occurs (see the *Reset Function* section for additional information).

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8331/32 circuitry. This consideration is particularly true if the reference voltage is low and/or the conversion rate is high. With a conversion clock of 12MHz, the ADS8331/32 makes a bit decision every 83ns. That is, for each subsequent bit decision, the capacitor array must be switched and charged, and the input to the comparator settled to a 16-bit level, all within one conversion clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n -bit SAR converter, there are n windows in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high-power devices, to name a few potential sources. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter CCLK signal because the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this possibility in mind, power to the ADS8331/32 should be clean and well-bypassed. A 0.1 μ F ceramic bypass capacitor should be placed as close as possible to the ADS8331/32 package. In addition, a 1 μ F to 10 μ F capacitor and a 5 Ω or 10 Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 22 μ F capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Although the ADS8331/32 draws very little current from the reference on average, there can still be instantaneous current demands placed on the external input and reference circuitry.

The [OPA365](#) or [OPA211](#) from Texas Instruments provide optimum performance for buffering the signal inputs; the [OPA350](#) can be used to effectively buffer the reference input.

Also, keep in mind that the ADS8331/32 offers no inherent rejection of noise or voltage variation in regards to the reference input. This consideration is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered, voltage variation resulting from the line frequency (50Hz or 60Hz) can be difficult to remove.

The AGND pin on the ADS8331/32 should be placed on a clean ground point. In many cases, this location is the analog ground. Avoid connecting the AGND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.

REVISION HISTORY

NOTE: Page numbers from previous revisions may differ from the page numbers in the current version.

Changes from Revision B (December 2010) to Revision C Page

- Changed name of last column in Low-Power, High-Speed, SAR Converter Family table 1
- Deleted 4-channel and 8-channel rows from 14-Bit Pseudo-Diff resolution in Low-Power, High-Speed, SAR Converter Family table 1
- Added last paragraph to *Start of a Conversion* section 22

Changes from Revision A (November 2010) to Revision B Page

- Deleted Ordering Information table 2

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
ADS8331IBPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IBPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8331IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IBPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IBPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS8332IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

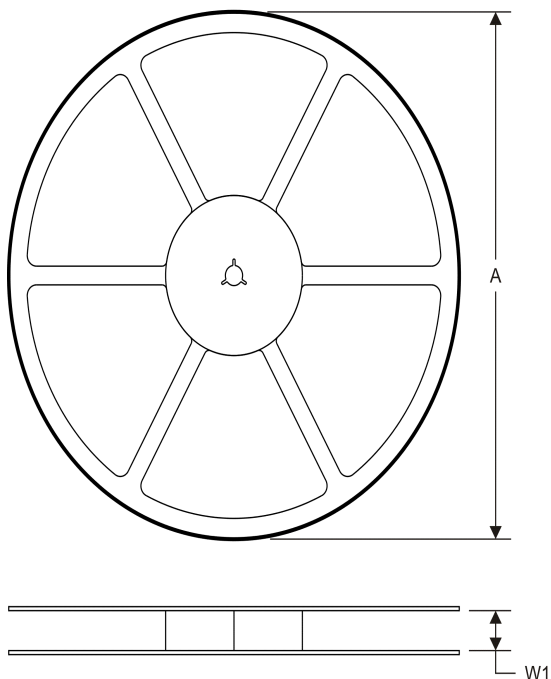
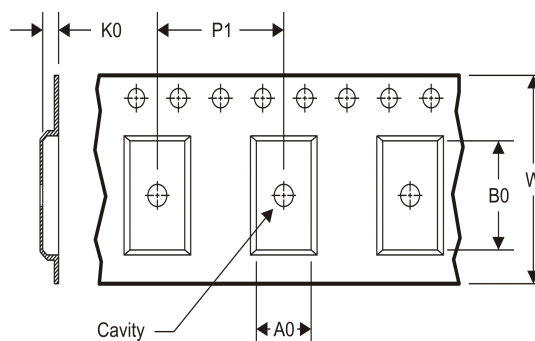
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8331BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8331BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8331RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8331RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8332BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS8332RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8332RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

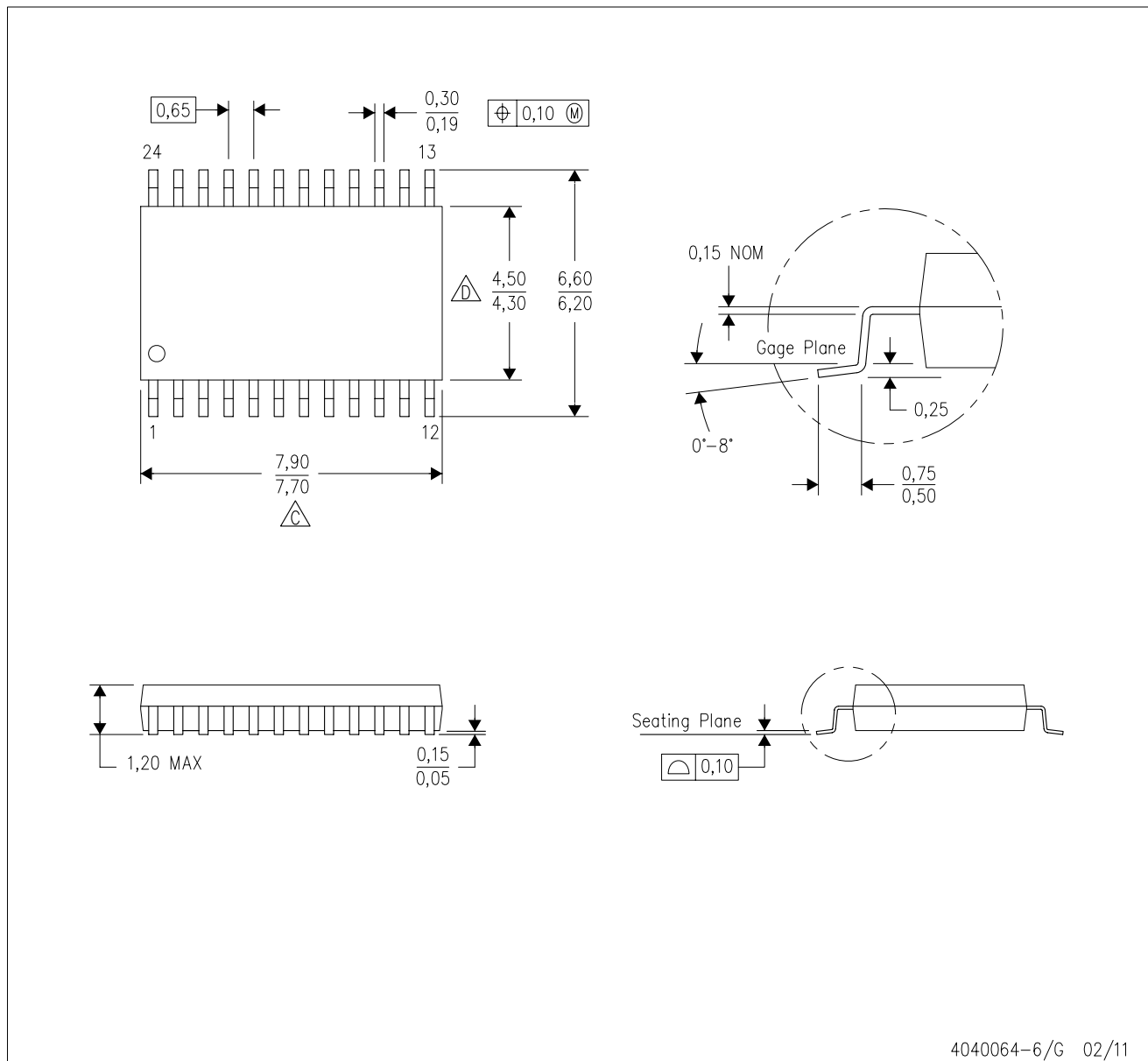


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8331IBPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8331IBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8331IBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8331IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8331IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8331IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8332IBPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8332IBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8332IBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8332IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
ADS8332IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8332IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

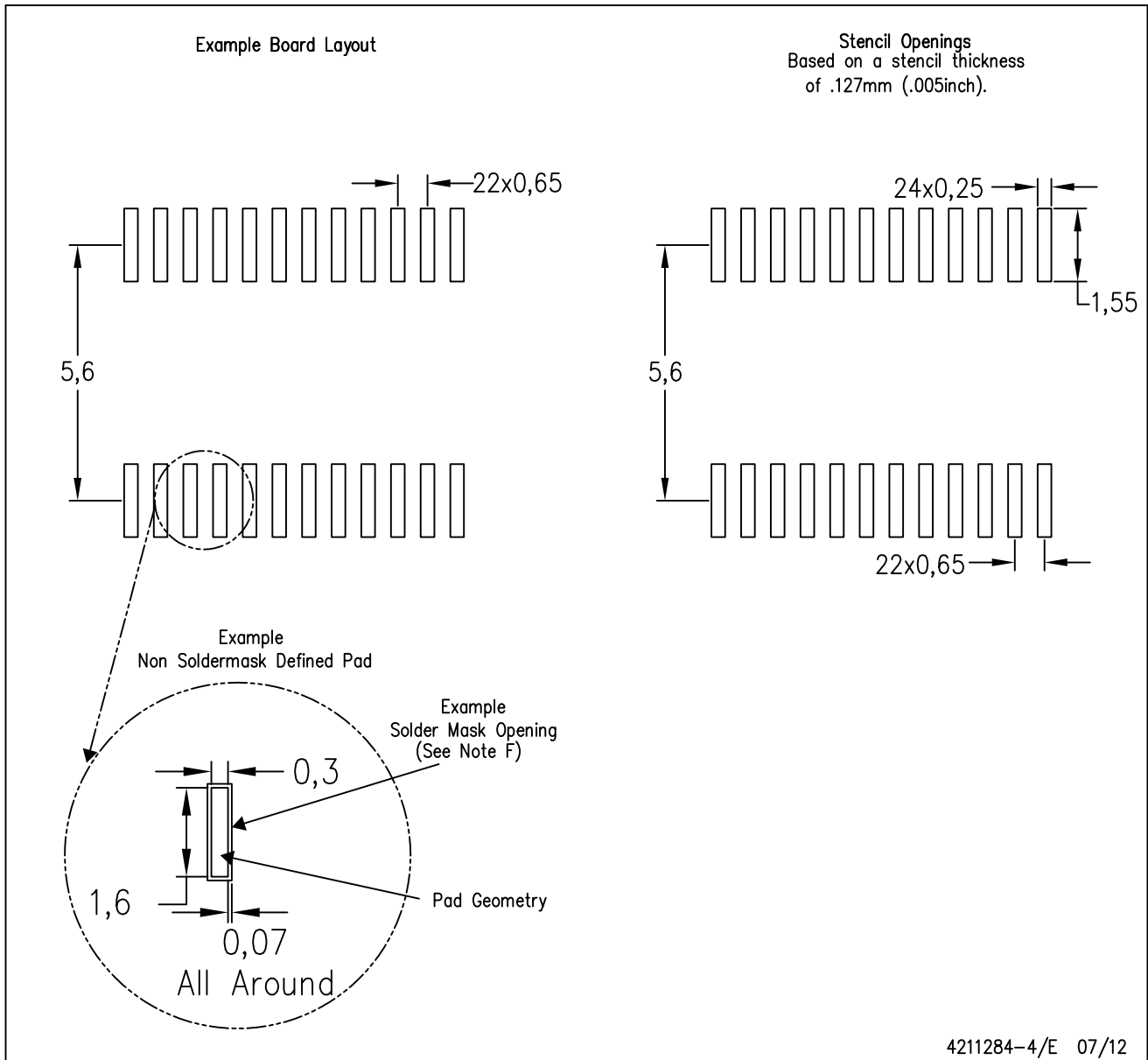


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

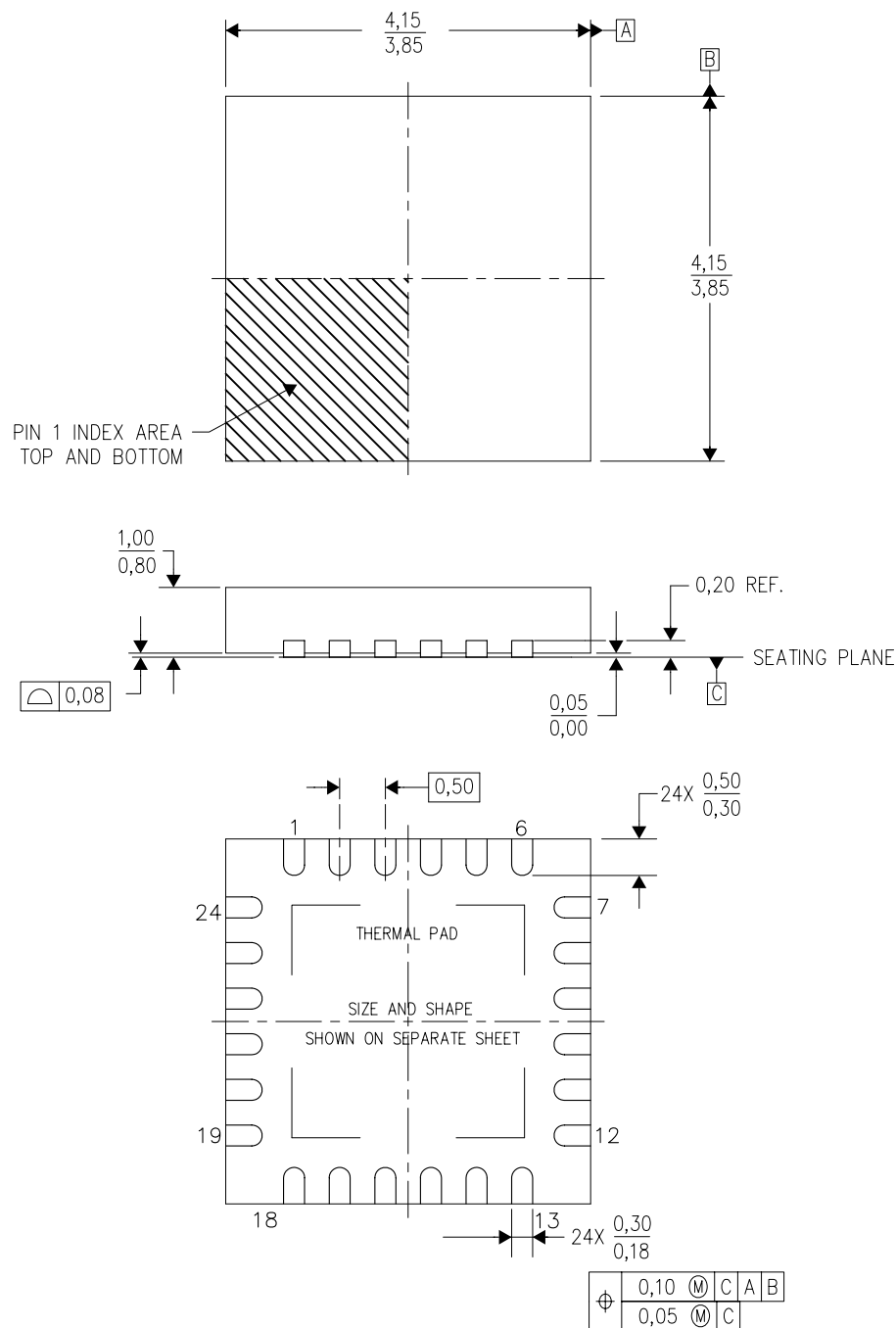
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

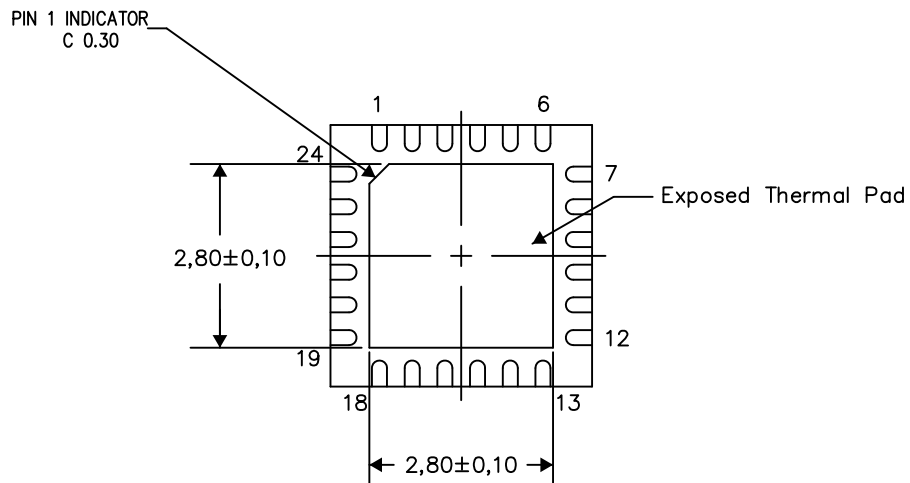
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

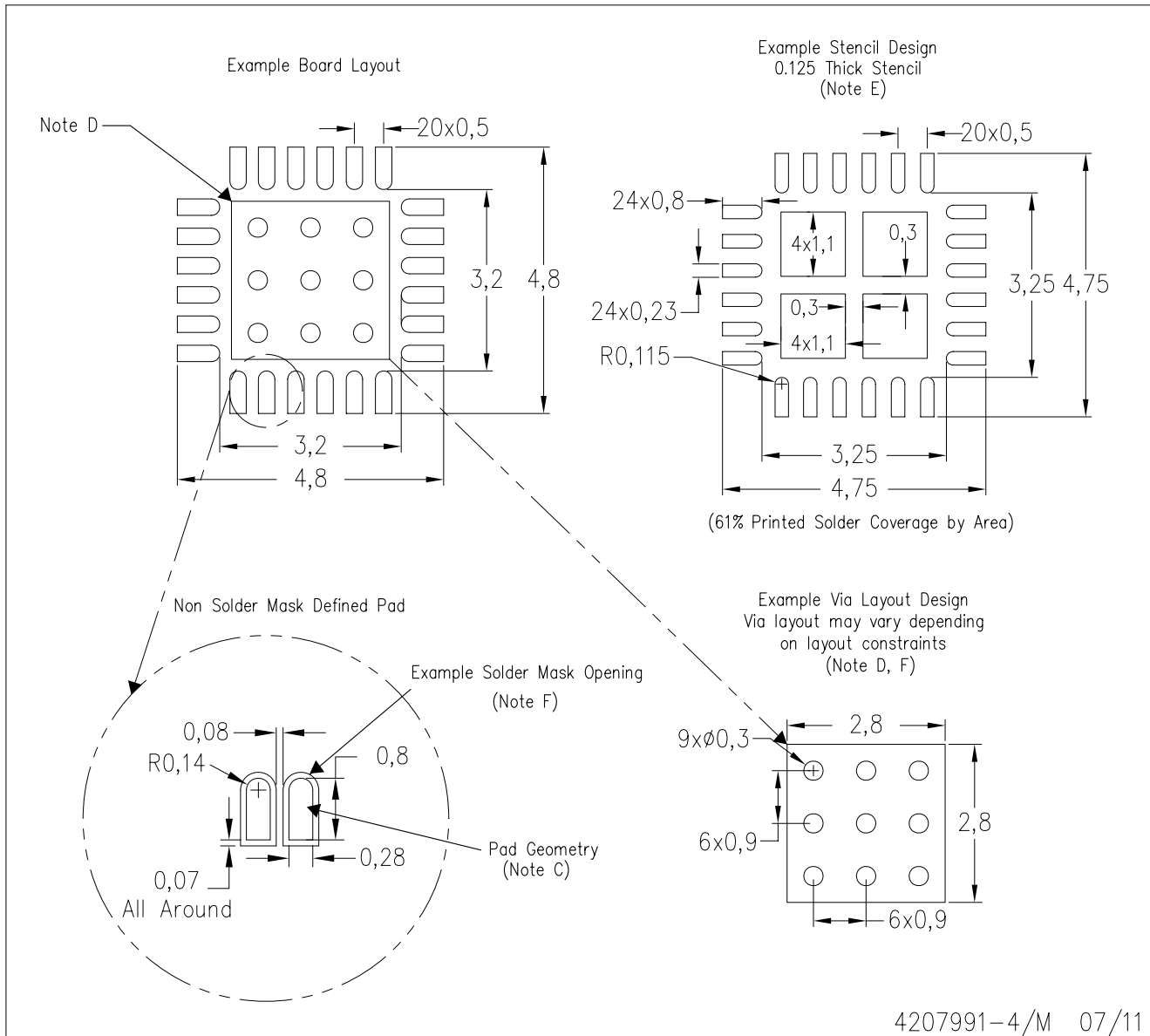
Exposed Thermal Pad Dimensions

4206344-5/AA 04/12

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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