Homework 2
The IA64 Architecture And Its Implementation

This homework is based on the following documents: *Introducing the IA-64 Architecture*, *Itanium Processor Microarchitecture*, and *The Intel IA-64 Compiler Code Generator*. All of them can be found on the web page of the course.

1 Speculation

1. What are the 3 main features of the IA64 architecture for speculation? Describe each of them and explain why they are useful to achieve high performance. Note that such features may not explicitly be named "speculation" - speculation occurs any time the processor executes instructions which may not be necessary or useful to the program.

2. What is the specific hardware support needed in order to use these features and that is implemented in Itanium?

2 Software Pipelining and Register Model

1. Describe the specific architectural support introduced in IA64 for software pipelining. Explain why it makes software pipelining less expensive and easier.

2. Considering the following program, write the assembly code that an Itanium compiler doing software pipelining would generate. Comment each line. The Itanium instruction set can be found in Intel Itanium Architecture Software Developer's Manual Volume 3.

$int * ptr1, *ptr2, i;$
$ptr1 = R1;$
$ptr2 = R2;$
$for(i = 0; i < 100; ++i)$
{
    $*ptr2 = *ptr1;$
    $++ptr1;$
    $++ptr2;$
}

3. Suppose that the for loop is replaced by a while loop, for example $while(*ptr1 != NULL)$. Explain what kind of changes your code would need.

4. Explain the register model for the programmer and the parameter passing convention. Illustrate the concept with the code which calls a C function `objA foo(int a, int b, int c)` where `objA` is a structure which occupies 32 bytes. Details on the calling conventions for Itanium can be found in the Itanium Software Conventions and Runtime Architecture

Guide. List advantages and disadvantages of this scheme in terms of (1) programmer/compiler comfort, (2) microarchitectural complexity, and (3) performance. Indicate with a simple diagram how the register addressing scheme might be implemented.