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S1D13517 Display Controller

Technical Manual

SEIKO EPSON CORPORATION

Rev. 1.2

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Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13517 External SDRAM LCD Controller. Included in this document are timing diagrams. AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This specification will be updated as appropriate. Please check the Epson Research and Development Website at http://www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13517 is a low power color LCD Controller with support for up to 128M-bit external SDRAM memory. The S1D13517 supports an 8/16-bit asynchronous bus while providing high performance bandwidth into the external display memory allowing for fast screen updates. The S1D13517 also provides support for multiple display buffers, Picture-in-Picture, Alpha-Blend, and display rotation/mirror.

The S1D13517 is an excellent solution for WVGA LCD panel systems while keeping CPU performance.

Chapter 2 Features

2.1 Frame Buffer

- External 16M-bit, 64M-bit or 128M-bit SDRAM memory support
- Maximum 90MHz SDRAM clock
- 16-bit bus interface (SDRAM is just one piece)

Note
Memory data cannot be read.

2.2 Host Interface

- 2 types 8/16-bit asynchronous bus interface (register or memory data)
  - Indirect Intel 80 bus
  - Indirect ALE (Address Latch Enable) bus

Note
1. Memory data cannot be read.
2. Write cycle time changes depend on SDRAM clock frequency.

2.3 Input Data Formats

- RGB 8:8:8 and RGB 5:6:5

2.4 Display Mode

- 24bpp (RGB 8:8:8) color depth. (RGB 5:6:5 data is converted from 16bpp to 24bpp)

2.5 Display Support

- Active Matrix TFT interface
  - 18/24-bit interface
- Maximum 960 x 960 display setting supported (maximum PCLK is 45MHz)
  - HVGA: 640 x 240 x 16/18/24-bit LCD panel
  - VGA: 640 x 480 x 16/18/24-bit LCD panel
  - WVGA: 800 x 480 x 16/18/24-bit LCD panel
  - SVGA: 800 x 600 x 16/18/24-bit LCD panel
  - QHD: 960 x 540 x 16/18/24-bit LCD panel

2.6 Display Features

- Display Window
  The display window is defined by the size of the LCD display. Complete or partial updates to the display window are done through the Write Window. The write window size and start position are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). All window coordinates are referenced to top left corner of the display window (even when rotation or mirror are enabled no host side translation is required).
  All display updates can have independent mirror, rotation, and transparency settings.
- Picture-in-Picture (PIP) display
  Up to two PIP windows are supported. When enabled the PIP windows are displayed over the Main window. The PIP windows sizes and start positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). Image scrolling can be performed by changing the start address of a PIP window. The PIP windows do not support a transparent overlay function.
- Alpha-Blend
  Alpha-blending allows two images to be blended to create a new image which can then be displayed using a PIP window. The Alpha-blend image size is specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). The processing speed of Alpha-blend function varies depending on the image size. Optionally, a single input image can be processed.
- Mirror / Rotation
  Mirror and 180° counter-clockwise hardware rotation functions are available for image data writes. All windows can have independent rotation and mirror settings. No additional programming is necessary when enabling these modes.
- Transparency
  A transparency function is available for image data writes. When enabled, input image data matching a specified key color is not written to the memory. This function can be used to overwrite text and icons in display data.
- Double Buffer
  Double buffering is available to prevent image tearing during streaming input.
- Multi Buffer
  Multi buffering allows the active display window to be switched between a maximum of 16 buffers. The number of buffers depends on the external SDRAM size and the desired size of the write buffers. Multi buffering allows a simple animation display to be performed by switching the buffers.

2.7 Clock Source

- Internal programmable PLL (Maximum 180MHz)
- Single MHz clock input: CLKI (2MHz~64MHz)
  - Internal system clock (Maximum 45MHz)
  - LCD pixel clock (Maximum 45MHz)
  - The frequency of the internal system clock and the LCD pixel clock is the same
- SDRAM clock (Maximum 90MHz)
  - Two or three times the clock frequency can be selected for the internal system clock
- Spread spectrum clock
  - Available to add to the internal clock. (Note: the frequency is only 31MHz-80MHz.)

2.8 Power Supply

- I/O voltage: 3.3V +/- 0.3V
- Core voltage: 2.5V +/- 0.2V
- PLL voltage: 2.5V +/- 0.2V

2.9 Miscellaneous

- PWM output for the LCD backlight control
- Software Power Save Mode
- Tearing Effect output
- Interrupt output (Alpha-Blend complete)
- General Purpose Output (GPO[3:0])
- Test Color-bar display (does not use SDRAM data)
- Package: QFP15-128

Chapter 3 System Diagrams

The following figures are example of the system diagram.

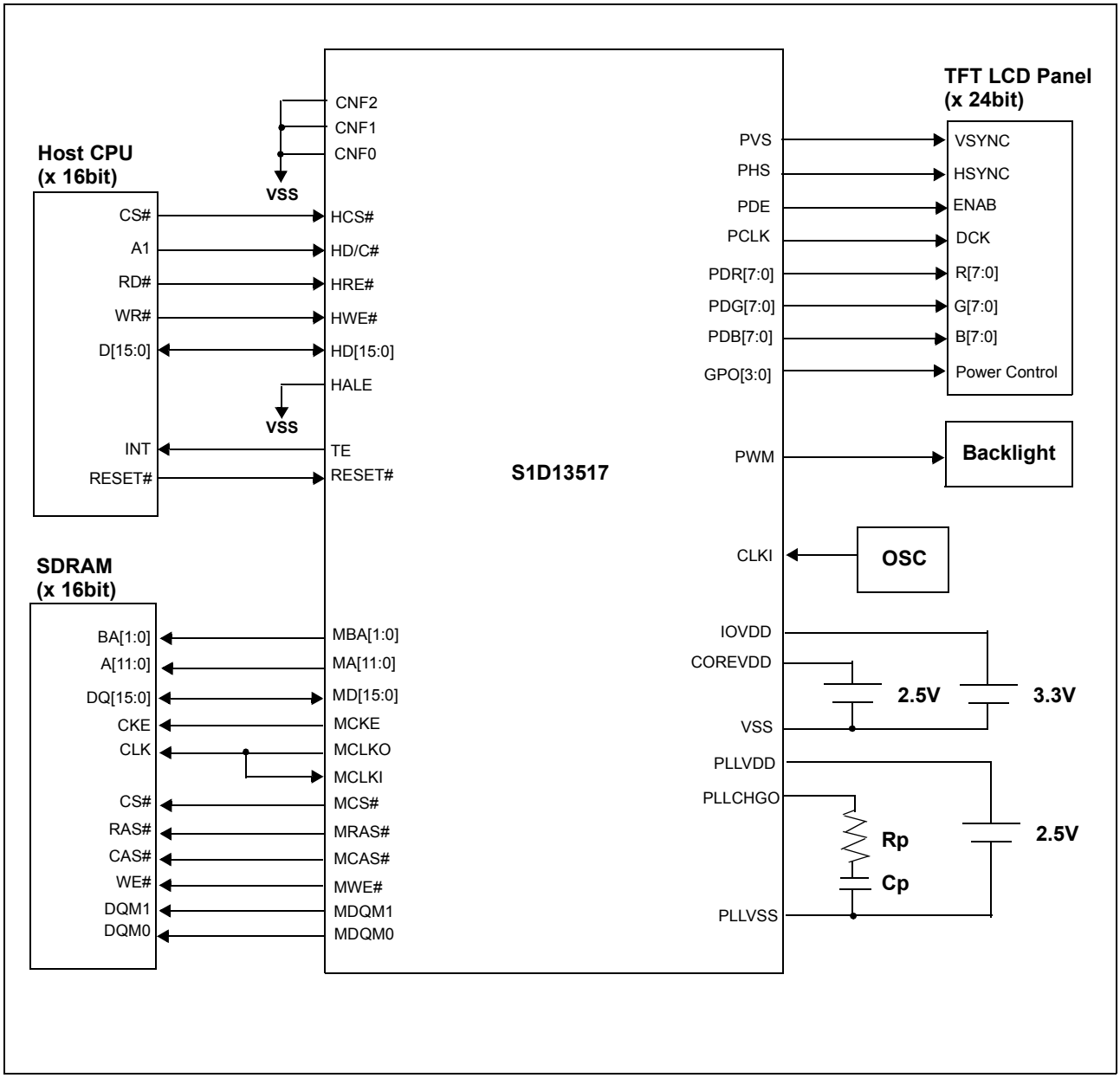


Figure 3-1: System Diagram Example (16-bit Intel80 bus)

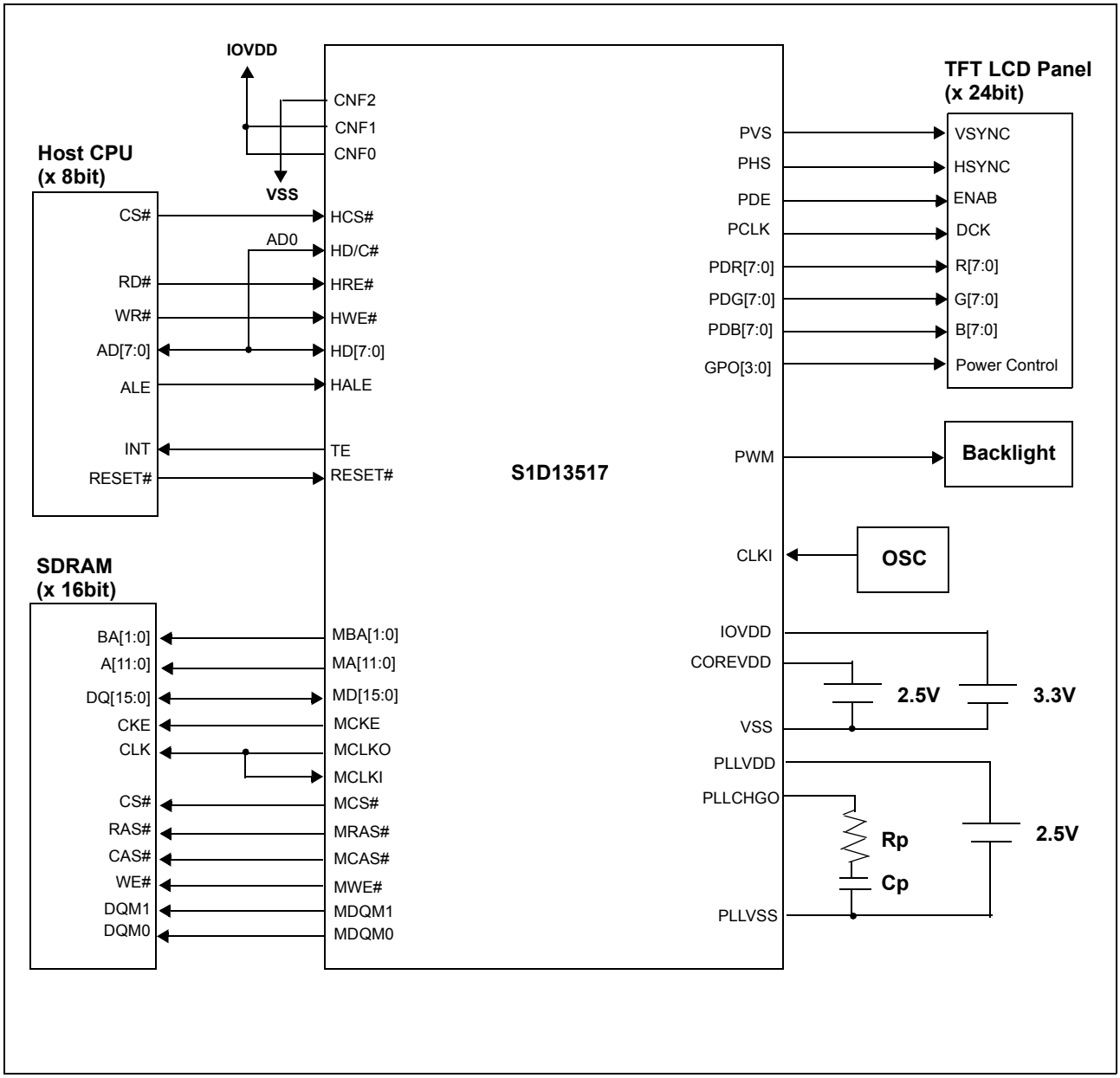


Figure 3-2: System Diagram Example (8-bit ALE bus)

Chapter 4 Block Diagram

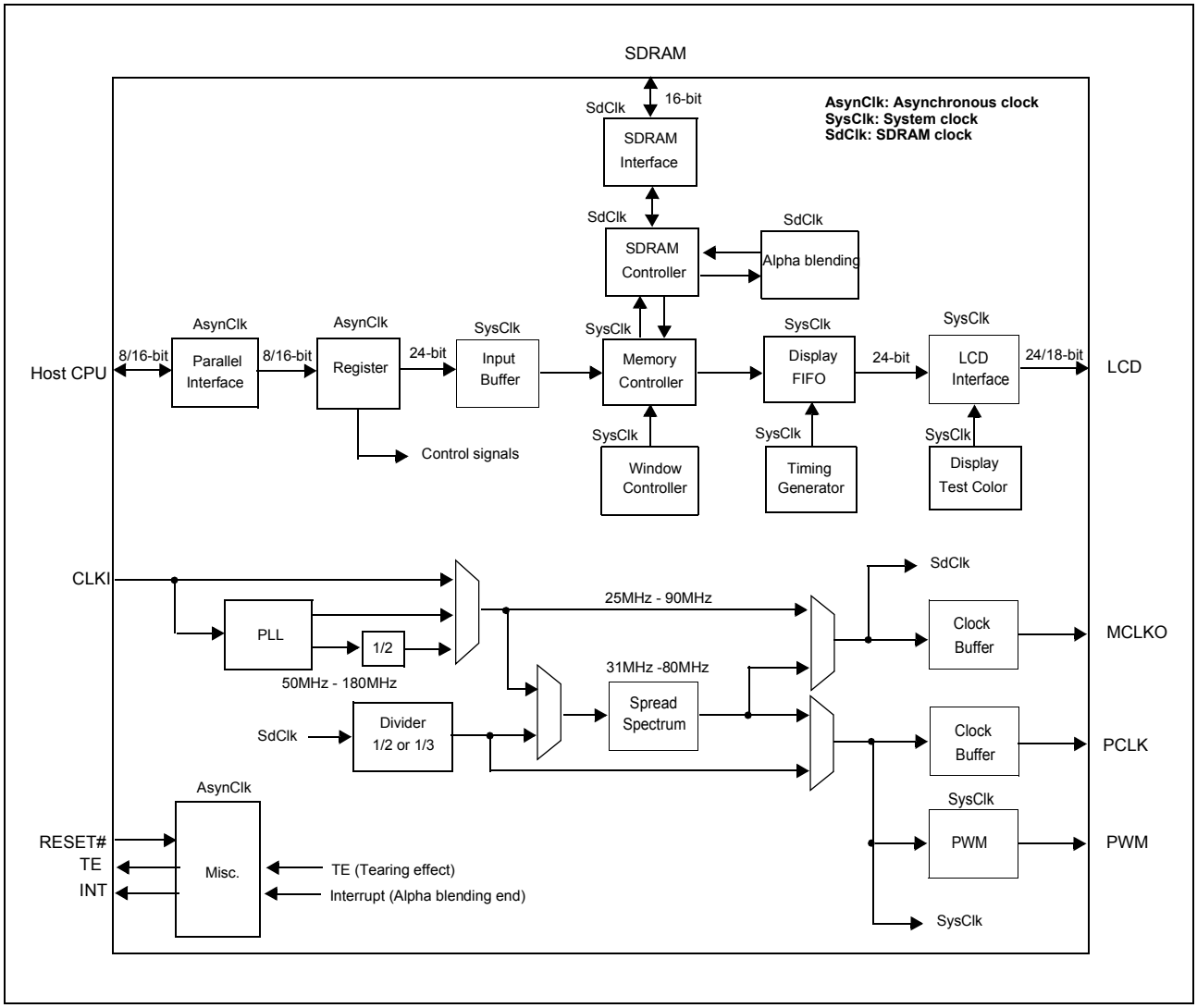


Figure 4-1: S1D13517 Block Diagram

Chapter 5 Display Data Path

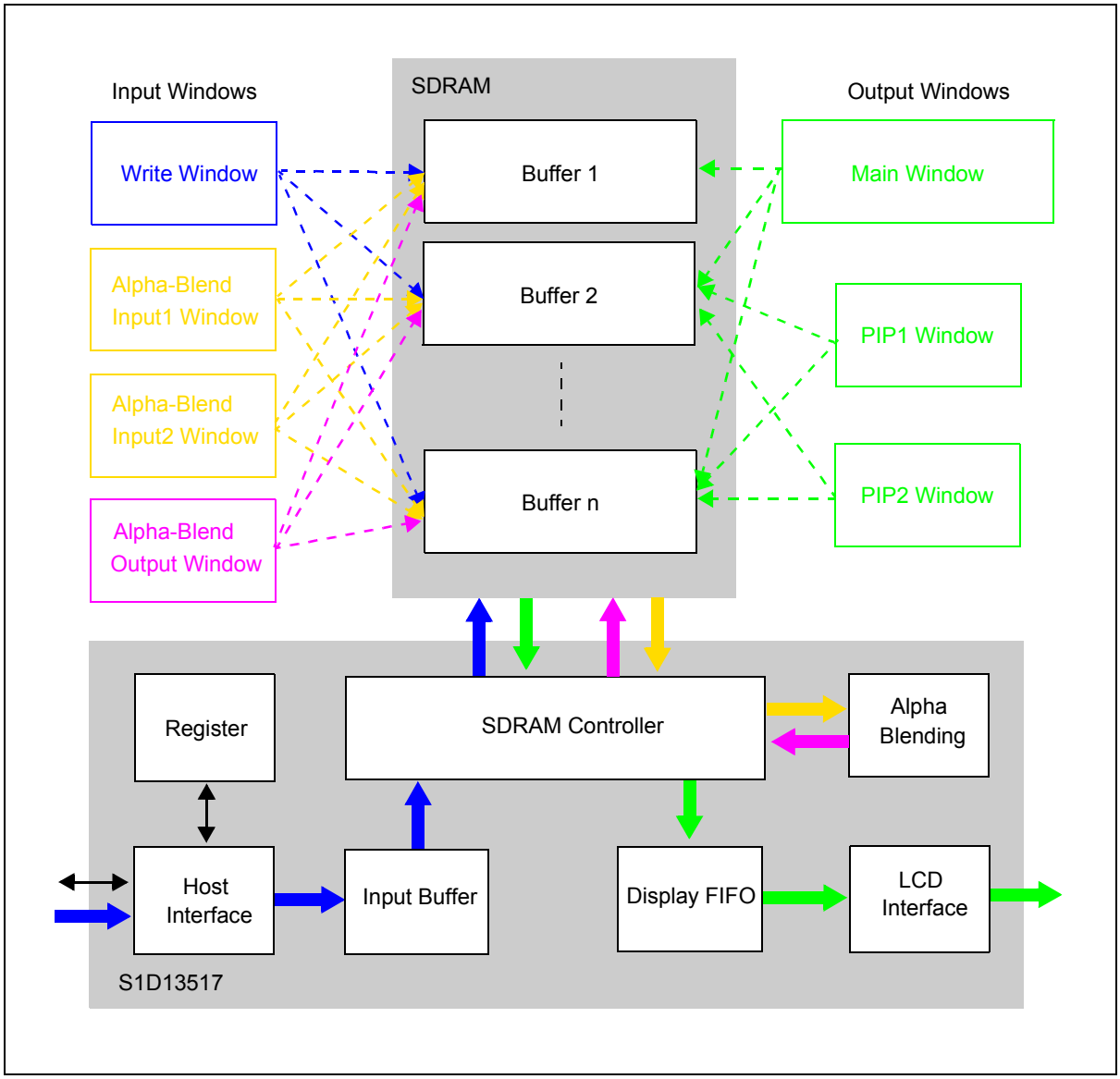


Figure 5-1: Display Data Path

Chapter 6 Pinout Diagram

6.1 Pin-Out

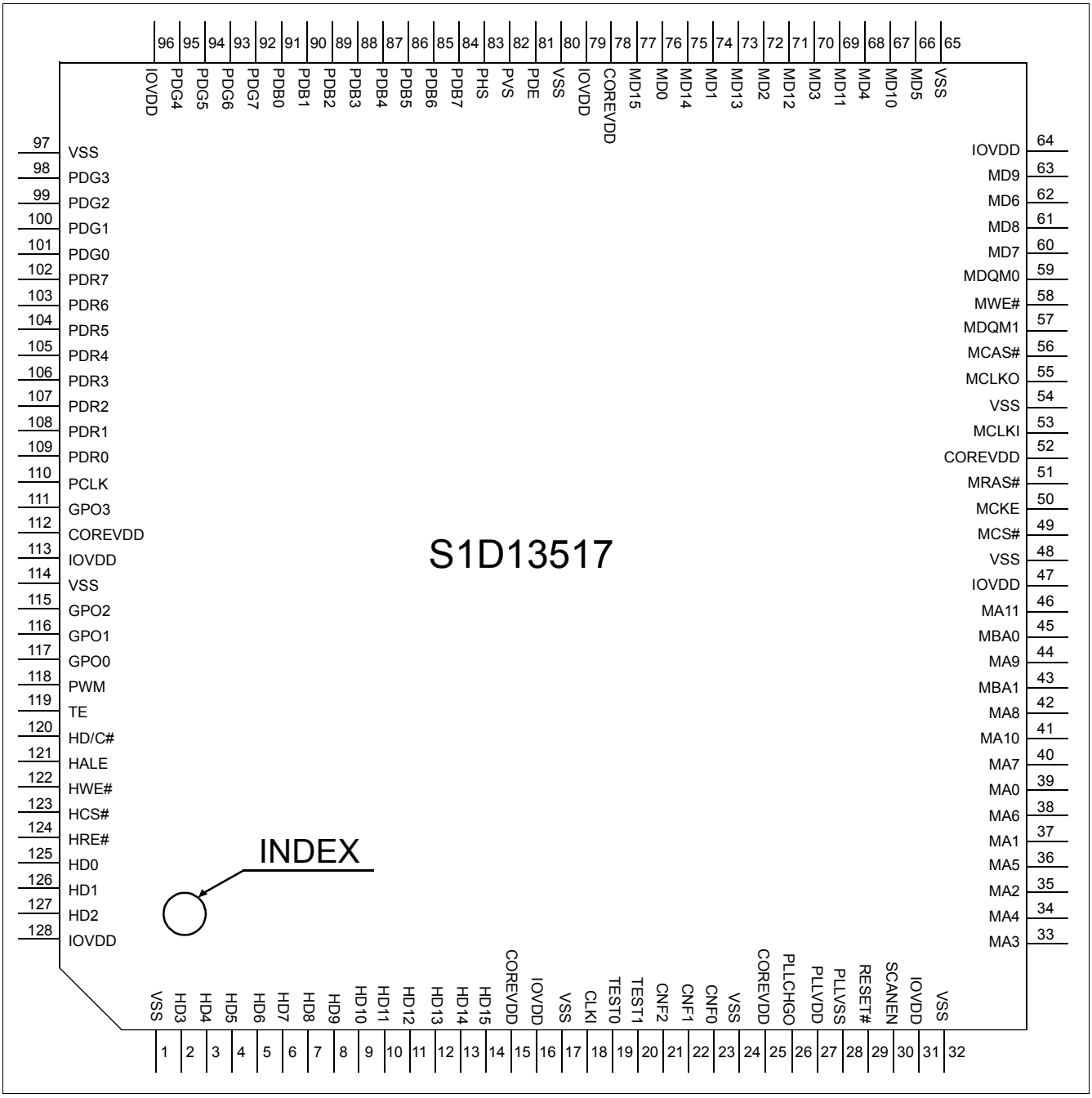


Figure 6-1: S1D13517 Pinout (Top View)

6.2 Pin Descriptions

Key:

Pin Types

I = Input

O = Output

IO = Bi-Directional (Input/Output)

P = Power pin

RESET# / Power Save Status

H = High level output

L = Low level output

Z = High Impedance

0 = Pull-down resistor on

Table 6-1: Cell Description

Item	Description
HI	H System LVCMO Input Buffer
HIS	H System LVCMOS Schmitt Input Buffer
HID	H System LVCMOS Input Buffer with pull-down resistor
HO1	H System LVCMOS Output Buffer Type 1 (+/- 3mA)
HO2	H System LVCMOS Output Buffer Type 2 (+/- 6mA)
HB1G	H System LVCMOS Bidirectional Buffer Type 1 (+/- 3mA) with gated input
HB1D	H System LVCMOS Bidirectional Buffer Type 1 (+/- 3mA) with pull-down resistor
LOT	L System Analog Output

Note

1. H System is IOVDD
2. L System is COREVDD and PLLVDD

6.2.1 Host Interface

For a summary of the Host pin mapping see Section 6.5, “Host Interface Data Pin Mapping” and Section 6.6, “Host Interface Control Pin Mapping” on page 24

Table 6-2: Host Interface Pin Descriptions

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
HD[15:8]	IO	14, 13, 12, 11, 10, 9, 8, 7	HB1G	IOVDD	Z	Input	Intel80 bus / ALE bus These pins are data bus. When the 8-bit interface is selected by CNF0, the input is gated. The input can be still floating. When HCS# is high input, the input also can be floating.
HD[7:0]	IO	6, 5, 4, 3, 2, 127, 126, 125	HB1G	IOVDD	Z	Input	Intel80 bus / ALE bus These pins are data bus. When HCS# is high input, the input also can be floating.
HWE#	I	122	HIS	IOVDD	Input	Input	Intel80 bus / ALE bus This pin is the write enable.
HRE#	I	124	HI	IOVDD	Input	Input	Intel80 bus / ALE bus This pin is the read enable.
HCS#	I	123	HI	IOVDD	Input	High Input	Intel80 bus / ALE bus This pin is the chip select. When the power save mode is enabled, this pin should be high level.
HD/C#	I	120	HI	IOVDD	Input	Input	Intel80 bus This pin is used to select between address and data. ALE bus This pin is used to select between address and data. The data is latched by the rising edge of HALE. When in 8-bit mode, this pin should be connected to HD0. When the 16-bit mode, this pin should be connected to HD1. This input should never be floating.
HALE	I	121	HI	IOVDD	Input	Input	Intel80 bus This pin is not used. This pin must be connected directly to VSS. ALE bus This pin is the address latch enable. The data on HD/C# is latched on the rising edge of HALE.

Table 6-2: Host Interface Pin Descriptions (Continued)

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
TE/INT	O	119	HO1	IOVDD	L	Stop	Tearing effect (default) This output is the status signal of VNDP and HNDP. When power save mode is enabled, this signal is stopped. Interrupt This pin is the interrupt output. When power save mode is enabled, this signal is stopped. See REG[6Ah] bits 1-0 on page 78 for TE/INT pin configuration.
RESET#	I	29	HIS	IOVDD	Input	High Input	This pin is reset input. Active low input to set all internal registers to the default value. This input has the Schmitt input and delay line for noise input. See Section 8.2, “Reset Timing” on page 31 for further information.

6.2.2 LCD Interface

For a summary of the LCD Interface pin mapping see Section 6.7, “LCD Interface Pin Mapping” on page 25

Table 6-3: LCD Interface Pin Descriptions

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
PDR[7:2]	O	102, 103, 104, 105, 106, 107	HO1	IOVDD	L	L	These pins are R[7:2] of the panel data output.
PDR[1:0] / GPO[5:4]	O	108, 109	HO1	IOVDD	L	L	These pins are R[1:0] of the panel data output in 24-bit mode. These pins are GPO[5:4] output in 18-bit mode.
PDG[7:2]	O	92, 93, 94, 95, 98, 99	HO1	IOVDD	L	L	These pins are G[7:2] of the panel data output.
PDG[1:0] / GPO[7:6]	O	100, 101	HO1	IOVDD	L	L	These pins are G[1:0] of the panel data output in 24-bit mode. These pins are GPO[7:6] output in 18-bit mode.
PDB[7:2]	O	84, 85, 86, 87, 88, 89	HO1	IOVDD	L	L	These pins are B[7:2] of the panel data output.
PDB[1:0] / GPO[9:8]	O	90, 91	HO1	IOVDD	L	L	These pins are B[1:0] of the panel data output in 24-bit mode. These pins are GPO[9:8] output in 18-bit mode.
PVS	O	82	HO1	IOVDD	L	L	This pin is the vertical sync pulse output.

Table 6-3: LCD Interface Pin Descriptions (Continued)

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
PHS	O	83	HO1	IOVDD	L	L	This pin is the horizontal sync pulse output.
PCLK	O	110	HO1	IOVDD	L	L	This pin is the pixel clock output.
PDE	O	81	HO1	IOVDD	L	L	This pin is the pixel data enable output.
GPO[3:0]	O	111, 115, 116, 117	HO1	IOVDD	L	L	These pins are GPO[3:0] output.

6.2.3 SDRAM Interface

Table 6-4: SDRAM Interface Pin Descriptions

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
MD[15:0]	I/O	77, 75, 73, 71, 69, 67, 63, 61, 60, 62, 66, 68, 70, 72, 74, 76	HB1D	IOVDD	0	0	These pins are the data bus for the SDRAM. These pins have internal pull-down resistors.
MBA[1:0]	O	43, 45	HO1	IOVDD	L	L	These pins are the bank address output for the SDRAM.
MA[11:0]	O	46, 41, 44, 42, 40, 38, 36, 34, 33, 35, 37, 39	HO1	IOVDD	L	L	These pins are the address output for the SDRAM.
MCS#	O	49	HO1	IOVDD	H	H	This pin is the chip select for the SDRAM.
MRAS#	O	51	HO1	IOVDD	H	H	This pin is the row address strobe output of the SDRAM.
MCAS#	O	56	HO1	IOVDD	H	H	This pin is the column address strobe output of the SDRAM.
MWE#	O	58	HO1	IOVDD	H	H	This pin is the write enable output of the SDRAM.
MDQM1	O	57	HO1	IOVDD	L	L	This pin is the DQMH output of the SDRAM.
MDQM0	O	59	HO1	IOVDD	L	L	This pin is the DQML output of the SDRAM.
MCLKO	O	55	HO2	IOVDD	H or L	H or L	This pin is the clock output of the SDRAM.
MCLKI	I	53	HI	IOVDD	Input	Input	This pin is the feedback clock input of the MCLKO.
MCKE	O	50	HO1	IOVDD	H	H	This pin is the CKE output of the SDRAM.

6.2.4 Clocks

Table 6-5: Clock Input Pin Description

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET #State	Power Save Status	Description
CLKI	I	18	HI	IOVDD	Input	Input	This pin is MHz input for PLL operation or MHz input if PLL is bypassed.

6.2.5 Miscellaneous

Table 6-6: Miscellaneous Pin Descriptions

Pin Name	TYpe	PIN #	Cell	IO Voltage	RESET# State	Power Save Status	Description
PWM	O	118	HO1	IOVDD	L	L	This pin is PWM output for the LCD backlight control.
CNF[2:0]	I	21, 22, 23	HI	IOVDD	Input Fix	Input Fix	These pins are used for power-up configuration. Note: These pins must be connected directly to IOVDD or VSS. See Section 6.4, “Configuration Options” on page 23 for further information.
PLLCHGO	O	26	LOT	PLLVDD	—	—	This pin is the low-path filter of the PLL. The external component are needed. When the PLL is bypassed, this pin should be left unconnected. See Chapter 18, “PLL” on page 131 for further information.
TEST[1:0]	I	20, 19	HID	IOVDD	—	—	These pins are the test signals. When unused these pins should be connected to VSS.
SCANEN	I	30	HID	IOVDD	—	—	This pin is the test signal. When unused this pin should be connected to VSS.

6.2.6 Power

Table 6-7: Power Pin Descriptions

Pin Name	Type	Pin #	Cell	Descriptions
COREVDD	P	15, 25, 52, 78, 112	P	Core power supply, all pins must be connected.
IOVDD	P	16, 31, 47, 64, 79, 96, 113, 128	P	IO power supply, all pins must be connected.
PLLVDD	P	27	P	PLL power supply
PLLVSS	P	28	P	PLL GND
VSS	P	1, 17, 24, 32, 48, 54, 65, 80, 97, 114	P	GND, all pins must be connected.

6.3 Pin Structure

6.3.1 Input Pin

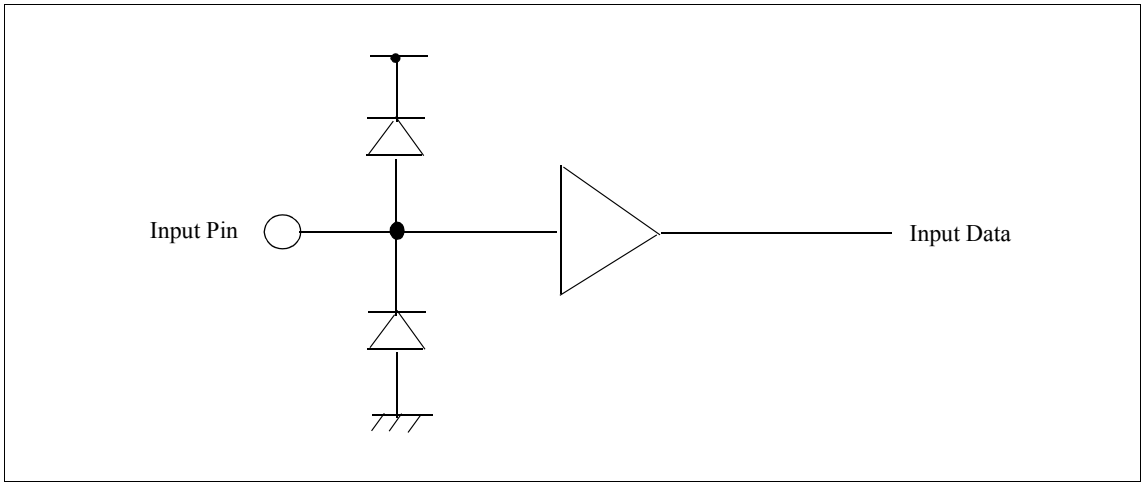


Figure 6-2: Input Pin (HI, HIS) Structure

6.3.2 Output Pin

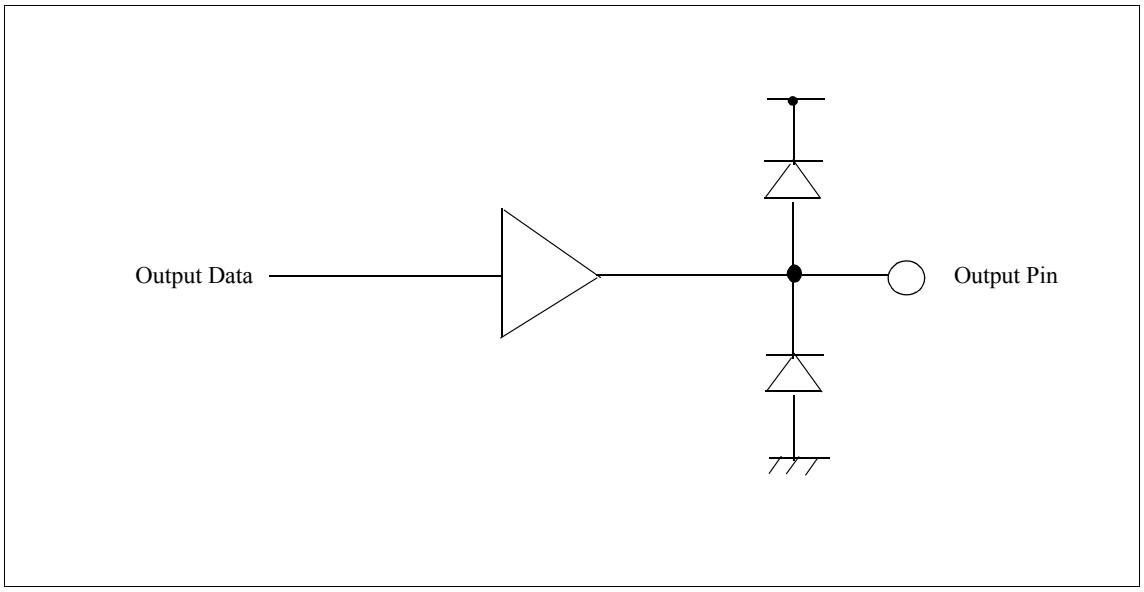


Figure 6-3: Output Pin (HO1, HO2) Structure

6.3.3 Bi-directional Pin

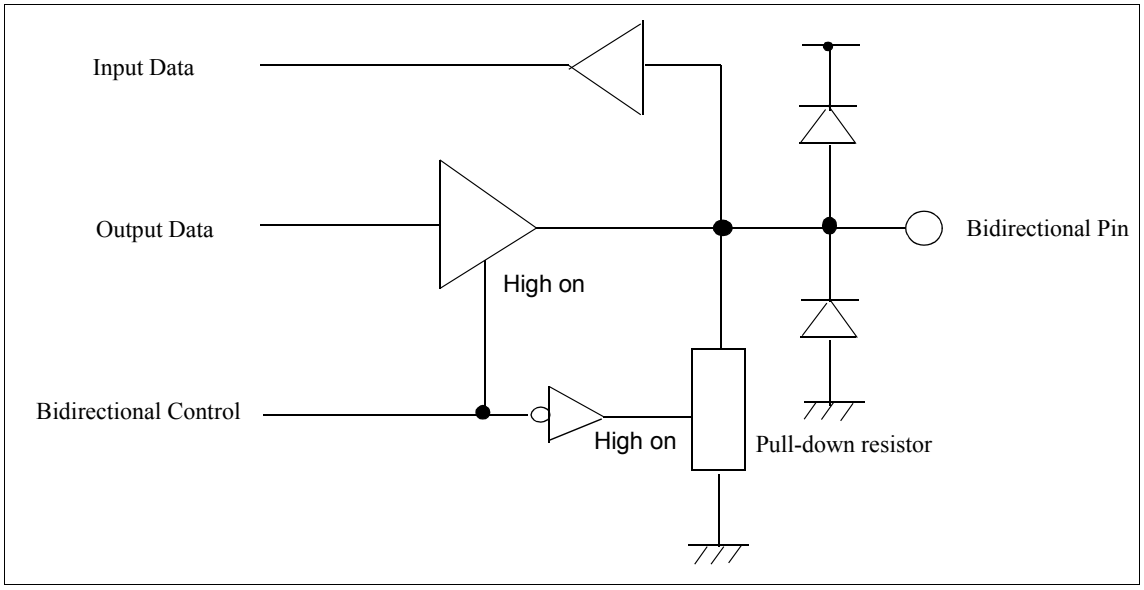


Figure 6-4: Bi-directional (HB1D) Structure

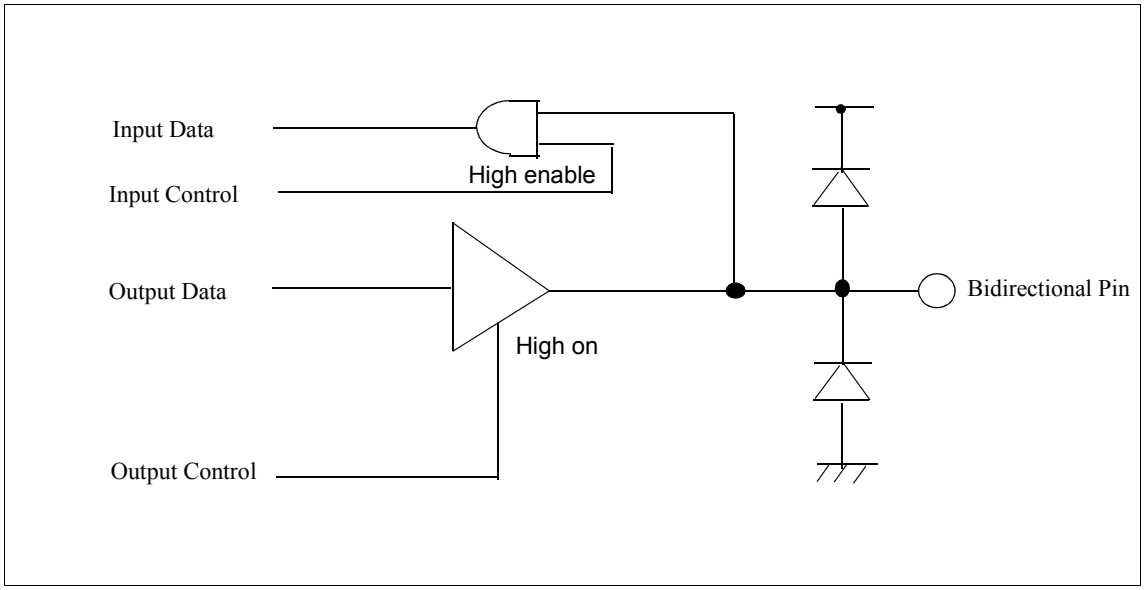


Figure 6-5: Bi-directional (HB1G) Structure

6.4 Configuration Options

These pins are used for power-up configuration and must be connected directly to IOVDD or VSS. The state of CNF[2:0] must not be changed during normal operation.

Pins	Power-on State	
	1 (connected to IOVDD)	0 (connected to VSS)
CNF0	Host interface 8-bit bus	Host interface 16-bit bus
CNF[2:1]	Host interface type CNF[2:1] = 00b: Indirect Intel80 bus CNF[2:1] = 01b: Indirect ALE bus CNF[2:1] = 1xb: Reserved	

Note

When CNF0 = 1b all register access is 8-bit only.

When CNF0 = 0b the memory data port (REG[66h] ~ REG[67h]) is 16-bit access. All other registers are 8-bit access only.

6.5 Host Interface Data Pin Mapping

This function is controlled by CNF0.

If 16-bit bus interface is NOT used, pins HD[15:8] should not be connected directly to the power rails, please leave these pins un-connected.

Table 6-8: Host Interface Data Pin Mapping

Pin Name	16-bit bus (CNF0 = 0b)	8-bit bus (CNF0 = 1b)
HD15	HD15	Open
HD14	HD14	Open
HD13	HD13	Open
HD12	HD12	Open
HD11	HD11	Open
HD10	HD10	Open
HD9	HD9	Open
HD8	HD8	Open
HD7	HD7	HD7
HD6	HD6	HD6
HD5	HD5	HD5
HD4	HD4	HD4
HD3	HD3	HD3
HD2	HD2	HD2
HD1	HD1	HD1
HD0	HD0	HD0

6.6 Host Interface Control Pin Mapping

This function is controlled by CNF[2:1].

Table 6-9: Host Interface Control Pin Mapping

Pin Name	Intel80 bus (CNF[2:1] = 00b)	ALE bus (CNF[2:1] = 01b)
HCS#	HCS#	HCS#
HRE#	HRE#	HRE#
HWE#	HWE#	HWE#
HD/C#	HD/C#	HD/C#
HALE	Connect to VSS	HALE
TE / INT	TE / INT	TE / INT

6.7 LCD Interface Pin Mapping

This function is controlled by REG[14h] bit 0.

Table 6-10: LCD Interface Pin Mapping

Pin Name	TFT Interface	
Color depth	**18bpp**	**24bpp**
PVS	PVS	
PHS	PHS	
PCLK	PCLK	
PDE	PDE	
PDR0	GPO4	R0
PDR1	GPO5	R1
PDR2	R2	
PDR3	R3	
PDR4	R4	
PDR5	R5	
PDR6	R6	
PDR7	R7	
PDG0	GPO6	G0
PDG1	GPO7	G1
PDG2	G2	
PDG3	G3	
PDG4	G4	
PDG5	G5	
PDG6	G6	
PDG7	G7	
PDB0	GPO8	B0
PDB1	GPO9	B1
PDB2	B2	
PDB3	B3	
PDB4	B4	
PDB5	B5	
PDB6	B6	
PDB7	B7	
GPO0	GPO0	GPO0
GPO1	GPO1	GPO1
GPO2	GPO2	GPO2
GPO3	GPO3	GPO3

Chapter 7 D.C. Characteristics

7.1 Absolute Maximum Rating

Table 7-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
CORE V_{DD}	Core Supply Voltage	VSS - 0.3 ~ 3.0	V
PLL V_{DD}	PLL Supply Voltage	VSS - 0.3 ~ 3.0	V
IO V_{DD}	IO Supply Voltage	COREVDD ~ 4.0	V
V_{IN}	Input Signal Voltage	VSS - 0.3 ~ IOVDD + 0.5	V
V_{OUT}	Output Signal Voltage	VSS - 0.3 ~ IOVDD + 0.5	V
I_{OUT}	Output Signal Current	±30	mA

7.2 Recommended Operating Conditions

Table 7-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
CORE V_{DD}	Core Supply Voltage	VSS = 0 V	2.30	2.50	2.70	V
PLL V_{DD}	PLL Supply Voltage	VSS = 0 V	2.30	2.50	2.70	V
IO V_{DD}	IO Supply Voltage	VSS = 0 V	3.00	3.30	3.60	V
V_{IN}	Input Voltage	—	VSS	—	IOVDD	V
T_{OPR}	Operating Temperature	—	-40	+25	+85	°C

7.3 Electrical Characteristics

The following conditions are for VSS = 0V, TOPR = -40 to +85°C.

Table 7-3: Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	Quiescent Conditions	—	—	1	mA
I_{PLL}	PLL Current	f_{PLL} = 90MHz	—	1	—	mA
I_{CORE}	Operating Current	COREVDD Pin	—	50	100	mA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH1}	High Level Output Voltage (1)	IOV_{DD} = min I_{OH1} = -3mA	IOVDD - 0.40	—	IOVDD	V
IOV_{OH2}	High Level Output Voltage (2)	IOV_{DD} = min I_{OH2} = -6mA	IOVDD - 0.40	—	IOVDD	V
IOV_{OL1}	Low Level Output Voltage (1)	IOVDD = min I_{OL1} = 3.0mA	VSS	—	0.40	V
IOV_{OL2}	Low Level Output Voltage (2)	IOVD = min I_{OL2} = 6.0mA	VSS	—	0.40	V
IOV_{IH1}	High Level Input Voltage	CMOS Input	2.20	—	—	V
IOV_{IL1}	Low Level Output Voltage	CMOS Input	—	—	0.80	V
IOV_{IH2}	High Level Input Voltage	Gated Input	1.70	—	—	V
IOV_{IL2}	Low Level Input Voltage	Gated Input	—	—	0.70	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	1.40	—	2.70	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.60	—	1.80	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.30	—	—	V
R_{PD}	Pull-Down Resistance	V_I = VDD	60	120	288	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	10	pF

Chapter 8 A.C. Characteristics

Conditions: IOVDD = 3.3V ± 0.3V, COREVDD = PLLVDD = 2.5V ± 0.2V, T_A = -40°C ~ 85°C
T_{rise} and T_{fall} for all inputs except Schmitt must be ≤50ns (10% ~ 90%)
T_{rise} and T_{fall} for all Schmitt must be$_l$ ≤5ms (10% ~ 90%)
C_L = 30pF (Host Interface)
C_L = 15pF (SDRAM Interface)
C_L = 30pF (LCD Interface)
C_L = 30pF (Other Interface)

8.1 Clock Timing

8.1.1 Input Clocks

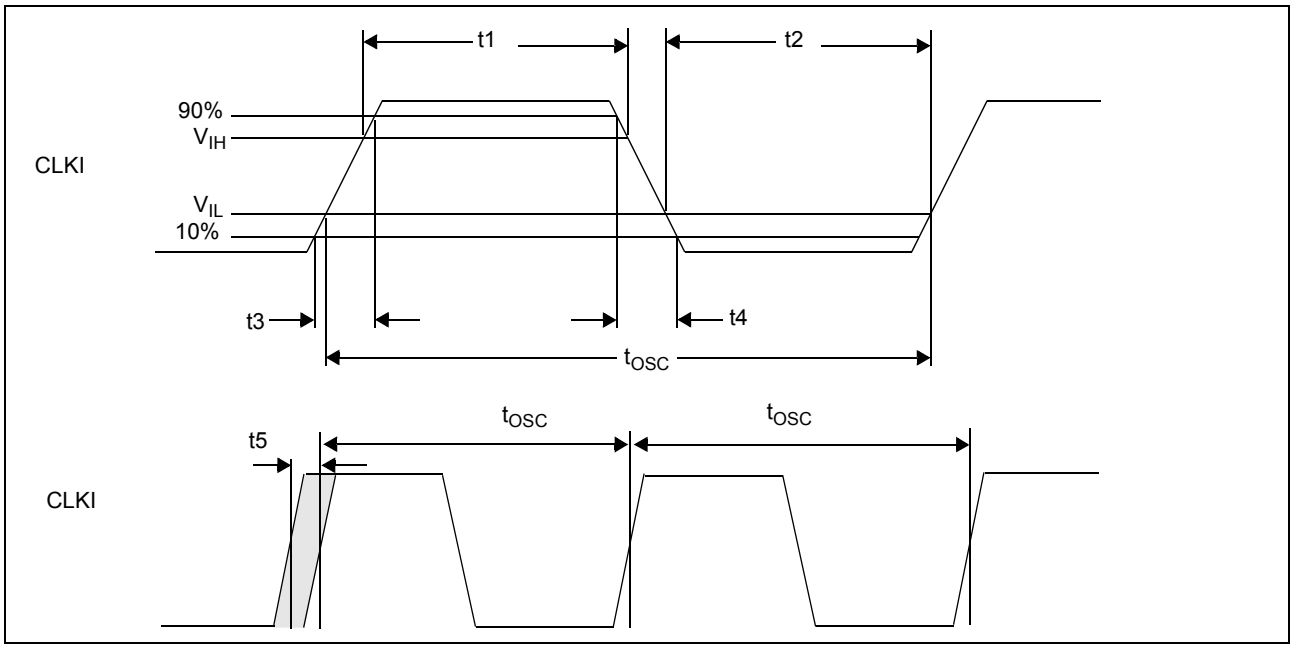


Figure 8-1: Clock Input Requirement (CLKI)

Table 8-1: Clock Input Requirement (CLKI)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	Input clock frequency	2	—	64	MHz
t_{OSC}	Input clock period	—	$1/f_{OSC}$	—	ns
t1	Input clock pulse width high	5	—	—	ns
t2	Input clock pulse width low	5	—	—	ns
t3	Input clock rise time (10% - 90%)	—	—	10	ns
t4	Input clock fall time (90% - 10%)	—	—	10	ns
t5	Input clock cycle jitter (see note 1)	-150		150	ps

1. The input clock cycle jitter is the difference in period between adjacent cycles.

8.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

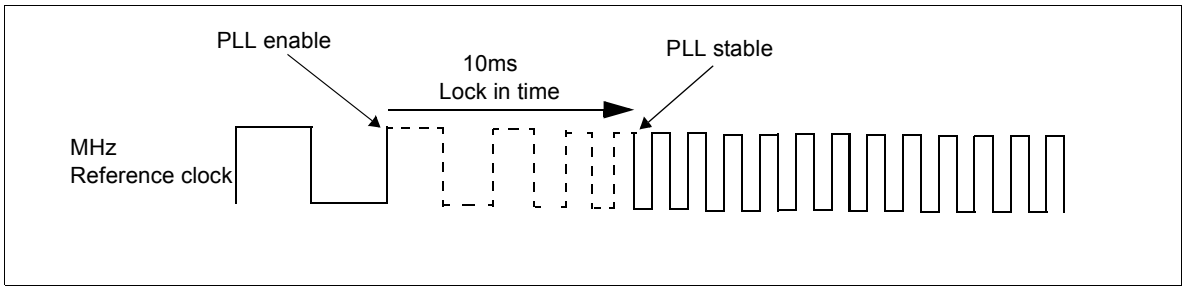


Figure 8-2: PLL Start-up Time

Table 8-2: PLL Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{PLLI}	PLL input clock frequency	0.99	1.00	2.00	MHz
f_{PLLO}	PLL output clock frequency	50	—	180	MHz
$f_{PLLDuty1}$	PLL output clock duty	30	50	70	%
$f_{PLLDuty2}$	PLL output clock duty (note)	40	50	60	%
t_{PJref}	PLL output clock period jitter	-500	—	500	ps
t_{PStal}	PLL output stable time	—	—	10	ms

Note
When REG[08h] bit 0 = 1b, the PLL output is divided to 1/2 clock.

8.1.3 Clock Output

Table 8-3: Clock Output (SYSCLK: SDCLK = 1:3)

Symbol	Parameter	Min	Typ	Max	Units
f_{SDCLK}	SDRAM clock (note1, 2)	—	—	90	MHz
t_{SDuty1}	SDRAM clock duty	30	50	70	%
t_{SDuty2}	SDRAM clock duty (note 3)	40	50	60	%
f_{SYSCLK}	Internal system clock (note 1)	—	—	30	MHz
f_{PCLK}	Pixel clock (note 1)	—	—	30	MHz
t_{PDuty}	Pixel clock duty	45	50	55	%

Table 8-4: Clock Output (SYSCLK: SDCLK = 1:2)

Symbol	Parameter	Min	Typ	Max	Units
f_{SDCLK}	SDRAM clock (note1, 2)	—	—	90	MHz
t_{SDuty1}	SDRAM clock duty	30	50	70	%
t_{SDuty2}	SDRAM clock duty (note 3)	40	50	60	%
f_{SYSCLK}	Internal system clock (note 1)	—	—	45	MHz
f_{PCLK}	Pixel clock (note 1)	—	—	45	MHz
t_{PDuty}	Pixel clock duty	45	50	55	%

Note
1. These values do not include the PLL jitter value and CLKI input difference.
2. The AC characteristic in the host interface changes depending on the frequency of the SDRAM clock.
3. When REG[08h] bit 0 = 1b, PLL output is divided to 1/2 clock.

8.1.4 Spread Spectrum (SS) Clock

As Spread Spectrum modulation clock EMI decreases, the spread Spectrum modulation can be increased.

Table 8-5: Spread Spectrum Clock

Symbol	Parameter	Min	Max	Units
f_{SSCLK}	Input SS clock (note)	31	80	MHz
t_{SSW}	SS clock diffusion width (REG[10h] bits 6-4 = 000b)	-0.37	0.37	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 001b)	-0.52	0.52	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 010b)	-0.67	0.67	ns
	SS clock diffusion width (REG[10h] bits 6-4 = 011b)	-0.82	0.82	ns
	SS clock diffusion width (REG[10h bits 6-4 = 100b)	-0.97	0.97	ns

Note
The input frequency of the SS must be from 31 to 80MHz. SS cannot be used between 82MHz to 90MHz.

8.2 Reset Timing

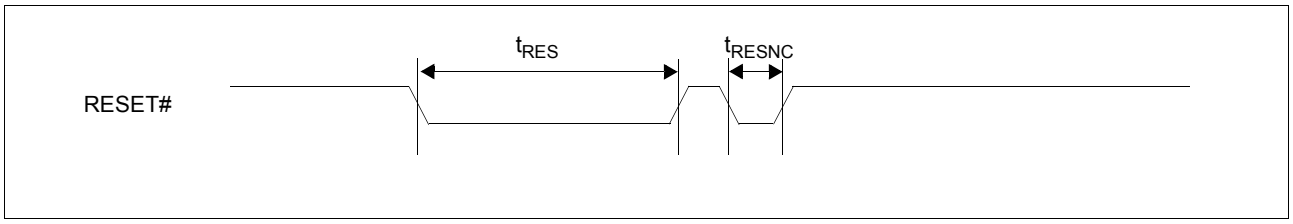


Figure 8-3: Reset Timing

Table 8-6: Reset Timing

Symbol	Parameter	Min	Max	Units
t_{RES}	Active reset pulse width	100	—	us
t_{RESNC}	Noise cancel pulse width	—	3	ns

8.3 Power Sequence Timing

8.3.1 Power-on Sequence Timing

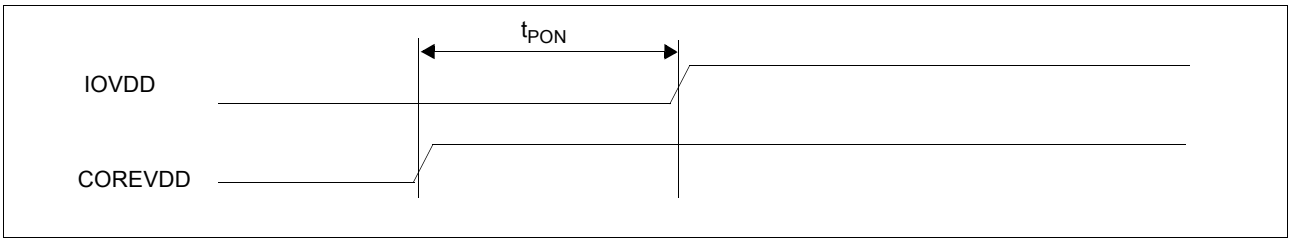


Figure 8-4: Power-on Sequence Timing

Table 8-7: Power-on Sequence Timing

Symbol	Parameter	Min	Max	Units
t_{PON}	Power-on difference time	0	—	ms

8.3.2 Power-off Sequence Timing

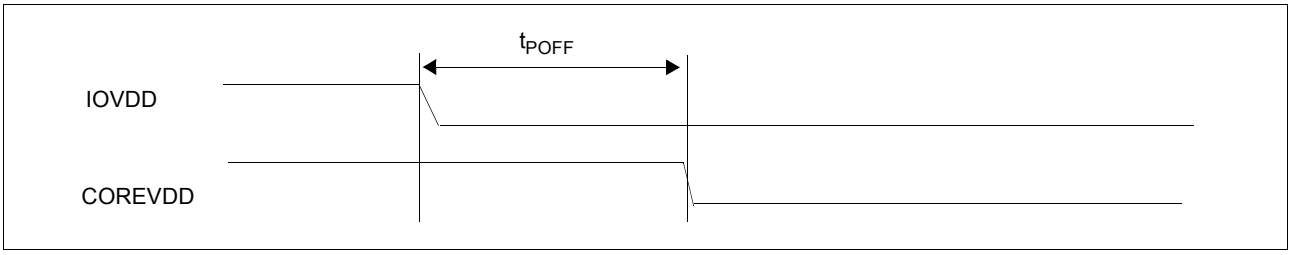


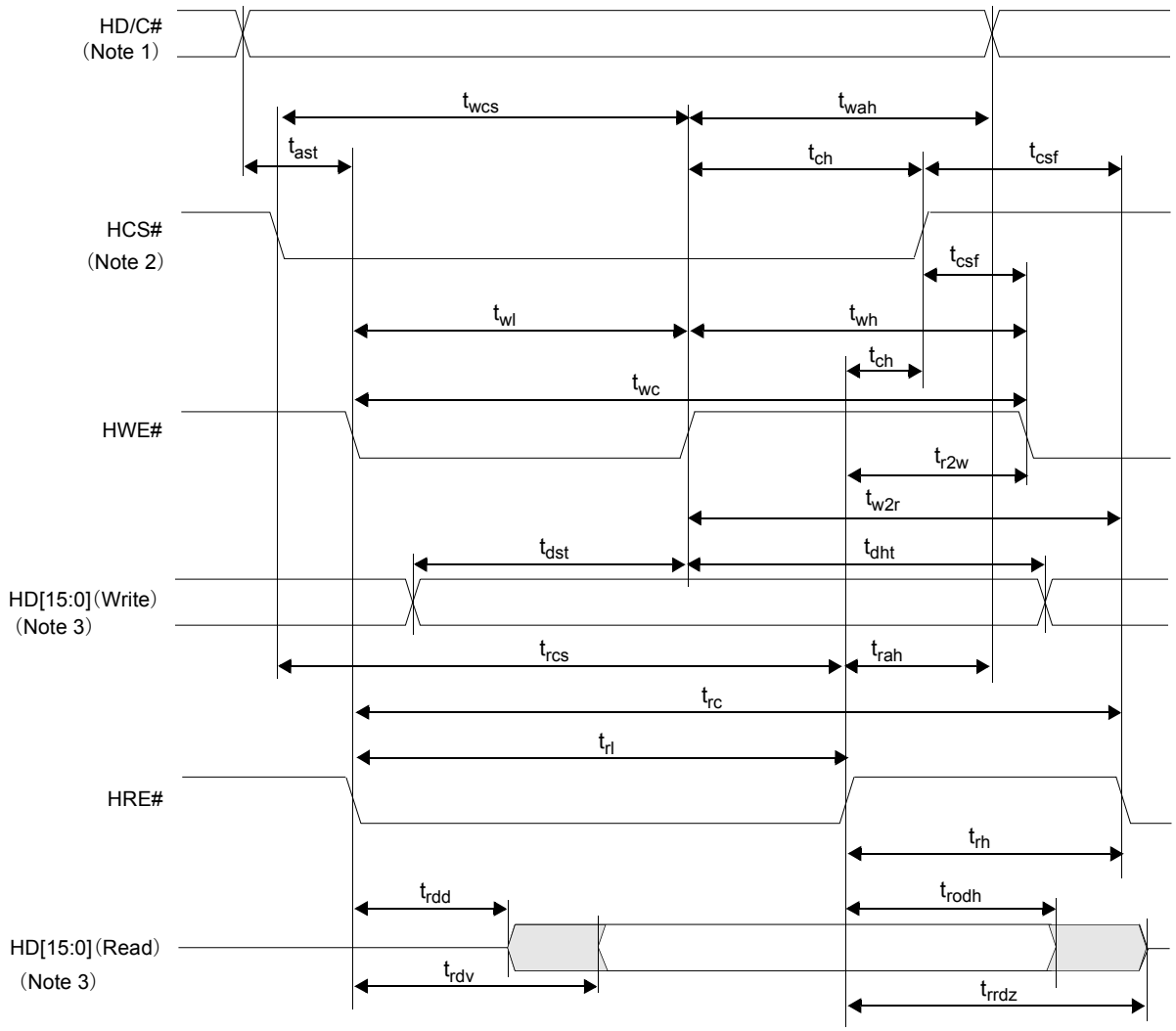
Figure 8-5: Power-off Sequence Timing

Table 8-8: Power-off Sequence Timing

Symbol	Parameter	Min	Max	Units
t_{POFF}	Power-off difference time	0	—	ms

8.4 Host Interface Timing

8.4.1 Indirect Intel80 Bus



Note 1: The HD/C# input pin is used to distinguish between Address and Data
Note 2: The register address will auto-increment in word increments for all register access except the memory data port. Writes to the memory data port will not increment the register address to support burst data write to memory.
Note 3: When CNF0=1, only HD[7:0] are used.
When CNF0=0, HD[15:0] are used for accesses to the Memory Data Port. HD[7:0] are used for all other accesses.

Figure 8-6: Intel80 Bus A.C. Characteristics

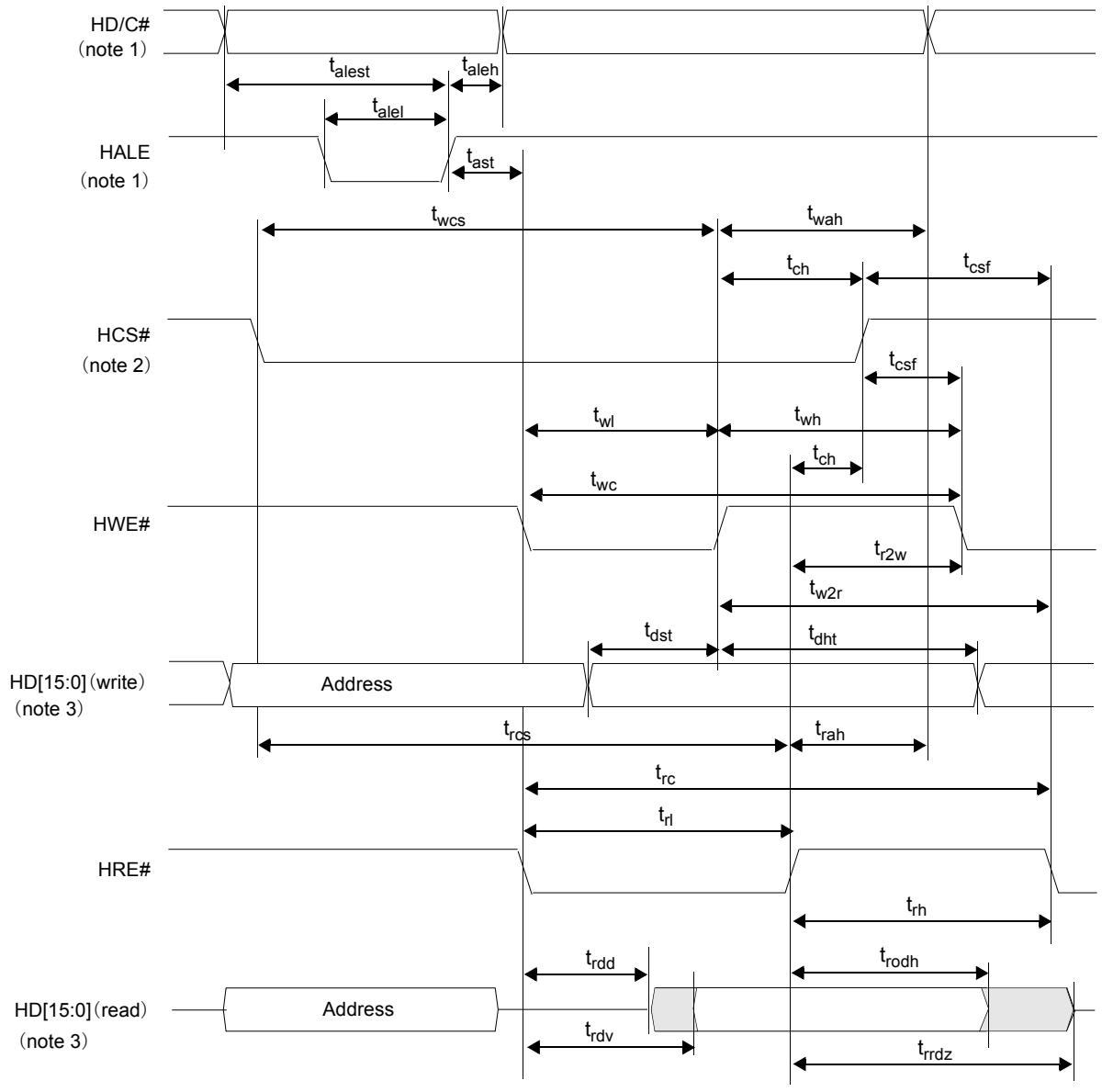
Table 8-9: Intel80 Bus A.C. Characteristics

Pin	Symbol	Parameter		Min	Max	Units	Note
HD/C#	t_{ast}	Address setup time (read/write)		1	—	ns	
	t_{wah}	Address hold time (write)		5	—	ns	
	t_{rah}	Address hold time (read)		5	—	ns	
HCS#	t_{wcs}	Chip select setup time (write)		t_{wl}	—	ns	
	t_{rcs}	Chip select setup time (read)		t_{rl}	—	ns	
	t_{ch}	Chip select hold time (read/write)		0	—	ns	
	t_{csf}	Chip select wait time (read/write)		1	—	ns	
HWE#	t_{wc}	Write cycle for registers		30	—	ns	
		Write cycle for memory (REG[12h] bit 4 = 0b)	8-bit 16bpp mode	$3.5 * (1/f_{SDCLK})$	—	ns	(note 1)
			8-bit 24bpp mode	$2.5 * (1/f_{SDCLK})$	—	ns	(note 1)
			16-bit 16bpp mode	$7 * (1/f_{SDCLK})$	—	ns	(note 1)
			16-bit 24bpp mode 1	$5 * (1/f_{SDCLK})$	—	ns	(note 1)
			16-bit 24bpp mode 2	$3.5 * (1/f_{SDCLK})$	—	ns	(note 1)
		Write cycle for memory (REG[12h] bit 4 = 1b)	8-bit 16bpp mode	$7 * (1/f_{SDCLK})$	—	ns	(note 2)
			8-bit 24bpp mode	$5 * (1/f_{SDCLK})$	—	ns	(note 2)
			16-bit 16bpp mode	$14 * (1/f_{SDCLK})$	—	ns	(note 2)
			16-bit 24bpp mode 1	$10 * (1/f_{SDCLK})$	—	ns	(note 2)
			16-bit 24bpp mode 2	$7 * (1/f_{SDCLK})$	—	ns	(note 2)
	t_{wl}	Pulse low duration		10	—	ns	
	t_{wh}	Pulse high duration		$t_{wc} - t_{wl}$	—	ns	
	t_{w2r}	HWE# rising edge to HRE# fall edge		20	—	ns	
HRE#	t_{r2w}	HRE# rising edge to HWE# fall edge		20	—	ns	
	t_{rc}	Read cycle		$t_{rl} + t_{rh}$	—	ns	
	t_{rl}	Pulse low duration		t_{rdv}	—	ns	
	t_{rh}	Pulse high duration		10	—	ns	
HD[15:0] (note3)	t_{dst}	Write data setup time		3	—	ns	
	t_{dht}	Write data hold time		5	—	ns	
	t_{rodh}	Read data hold time		1	—	ns	
	t_{rrdz}	HRE# rising edge to HD Hi-Z		—	10	ns	
	t_{rdv}	HRE# fall edge to HD active data		—	15	ns	
	t_{rdd}	HRE# fall edge to HD drive		5	—	ns	

Note

1. For REG[12h] bit 4 = 0b, when this spec is not satisfied, write buffer overflow of the memory controller occurs (REG[92h] bit 3).
2. For REG[12h] bit 4 = 1b, when this spec is not satisfied, write buffer overflow of the memory controller occurs (REG[92h] bit 3).
3. When CNF0=1, only HD[7:0] are used. When CNF0=0, HD[7:0] are used for all accesses except for the Memory Data Port when HD[15:0] are used.

8.4.2 Indirect ALE Bus



Note 1: The HD/C# input pin is used to distinguish between Address and Data. The HD/C# signal is latched by HALE rising edge.

Note 2: The register address will auto-increment in word increments for all register access except the memory data port. Writes to the memory data port will not increment the register address to support burst data write to memory.

Note 3: When CNF0=1, only HD[7:0] are used.
When CNF0=0, HD[15:0] are used for accesses to the Memory Data Port. HD[7:0] are used for all other accesses.

Figure 8-7: ALE Bus A.C. Characteristics

Table 8-10: ALE Bus A.C. Characteristics

Pin	Symbol	Parameter		Min	Max	Units	Note
HD/C#	t_{ast}	Address setup time (read/write)		1	—	ns	
	t_{wah}	Address hold time (write)		5	—	ns	
	t_{rah}	Address hold time (read)		5	—	ns	
HALE#	t_{alest}	Address setup time		5	—	ns	
	t_{aleh}	Address hold time		5	—	ns	
	t_{alel}	Pulse low duration		5	—	ns	
HCS#	t_{wcs}	Chip select setup time (write)		t_{wl}	—	ns	
	t_{rcs}	Chip select setup time (read)		t_{rl}	—	ns	
	t_{ch}	Chip select hold time (read/write)		0	—	ns	
	t_{csf}	Chip select wait time (read/write)		1	—	ns	
HWE#	t_{wc}	Write cycle for registers		30	—	ns	
		Write cycle for memory (REG[12h] bit 4 = 0b)	8-bit 16bpp mode	3.5 * ($1/f_{SDCLK}$)	—	ns	(note 1)
			8-bit 24bpp mode	2.5 * ($1/f_{SDCLK}$)	—	ns	(note 1)
			16-bit 16bpp mode	7 * ($1/f_{SDCLK}$)	—	ns	(note 1)
			16-bit 24bpp mode 1	5 * ($1/f_{SDCLK}$)	—	ns	(note 1)
			16-bit 24bpp mode 2	3.5 * ($1/f_{SDCLK}$)	—	ns	(note 1)
		Write cycle for memory (REG[12h] bit 4 = 1b)	8-bit 16bpp mode	7 * ($1/f_{SDCLK}$)	—	ns	(note 2)
			8-bit 24bpp mode	5 * ($1/f_{SDCLK}$)	—	ns	(note 2)
			16-bit 16bpp mode	14 * ($1/f_{SDCLK}$)	—	ns	(note 2)
			16-bit 24bpp mode 1	10 * ($1/f_{SDCLK}$)	—	ns	(note 2)
			16-bit 24bpp mode 2	7 * ($1/f_{SDCLK}$)	—	ns	(note 2)
	t_{wl}	Pulse low duration		10	—	ns	
	t_{wh}	Pulse high duration		t_{wc} - t_{wl}	—	ns	
	t_{w2r}	HWE# rising edge to HRE# fall edge		20	—	ns	
HRE#	t_{r2w}	HRE# rising edge to HWE# fall edge		20	—	ns	
	t_{rc}	Read cycle		t_{rl} + t_{rh}	—	ns	
	t_{rl}	Pulse low duration		t_{rdv}	—	ns	
	t_{rh}	Pulse high duration		10	—	ns	
HD[15:0] (note 3)	t_{dst}	Write data setup time		3	—	ns	
	t_{dht}	Write data hold time		5	—	ns	
	t_{rodh}	Read data hold time		1	—	ns	
	t_{rrdz}	HRE# rising edge to HD Hi-Z		—	10	ns	
	t_{rdv}	HRE# fall edge to HD active data		—	15	ns	
	t_{rdd}	HRE# fall edge to HD drive		5	—	ns	

Note

1. For REG[12h] bit 4 = 0b, when this spec is not satisfied, write buffer overflow of the memory controller occurs (REG[92h] bit 3).
2. For REG[12h] bit 4 = 1b, when this spec is not satisfied, write buffer overflow of the memory controller occurs (REG[92h] bit 3).
3. When CNF0=1, only HD[7:0] are used. When CNF0=0, HD[7:0] are used for all accesses except for the Memory Data Port when HD[15:0] are used.

8.4.3 Hi-Z Definition of transition time to Hi-Z state

Due to the difficulty of high impedance (Hi-Z) measurement for high speed signals, transition time from H/L to Hi-Z specified as follows.

- High to Hi-Z delay time: t_{pHZ}
  delay time when a gate voltage of final stage of the Pch-MOSFET turns to 0.8 x IOVDD (Pch-MOSFET is off).
  Total delay time to Hi-Z is calculated as following equation.
  Internal delay + t_{pHZ} (from High to Hi-Z)
- Low to Hi-Z delay time: t_{pLZ}
  delay time when a gate voltage of final stage of the Nch-MOSFET turn to 0.2 x IOVDD (Nch-MOSFET is off).
  Total delay time to Hi-Z is calculated as following equation.
  Internal delay time + t_{pLZ} (from Low to Hi-Z)

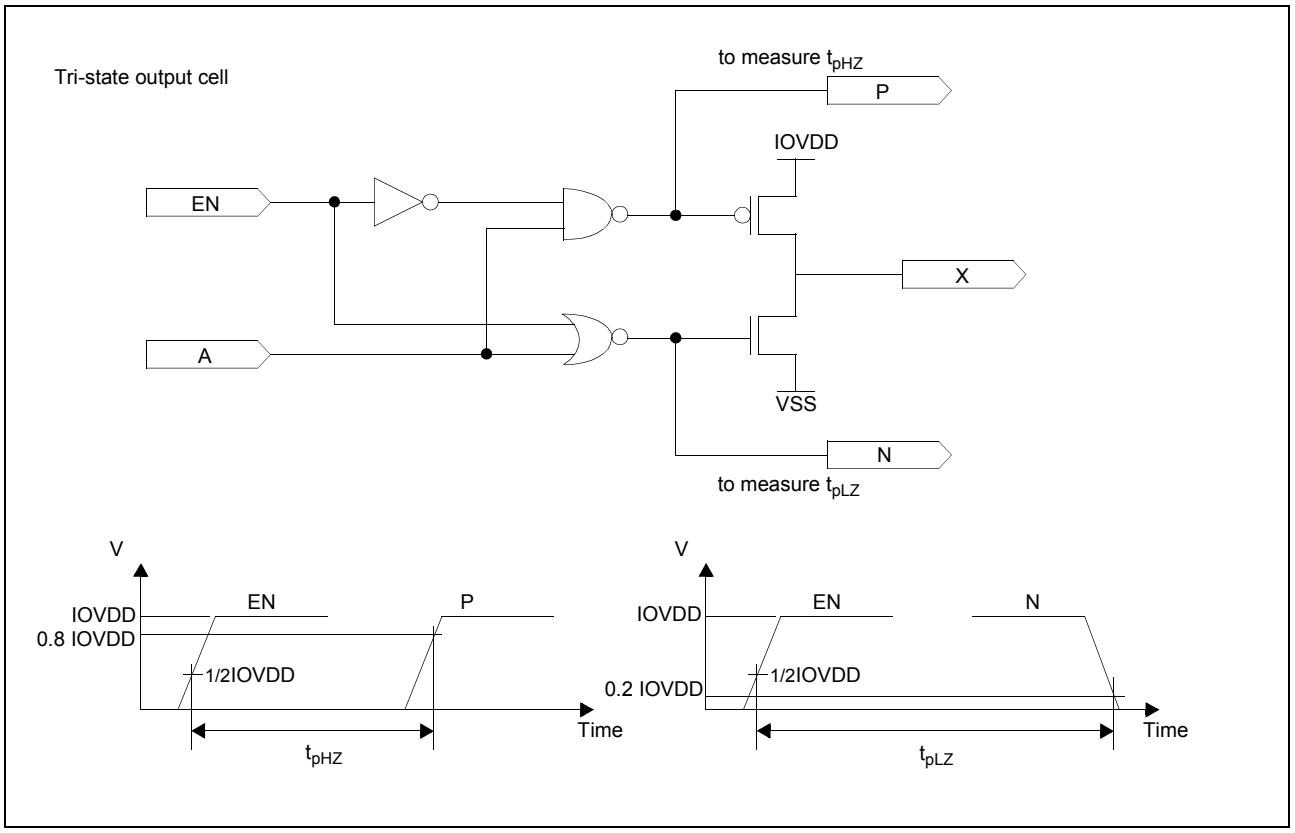


Figure 8-8: Hi-Z Definition of transition time to Hi-Z state

8.5 SDRAM Interface Timing

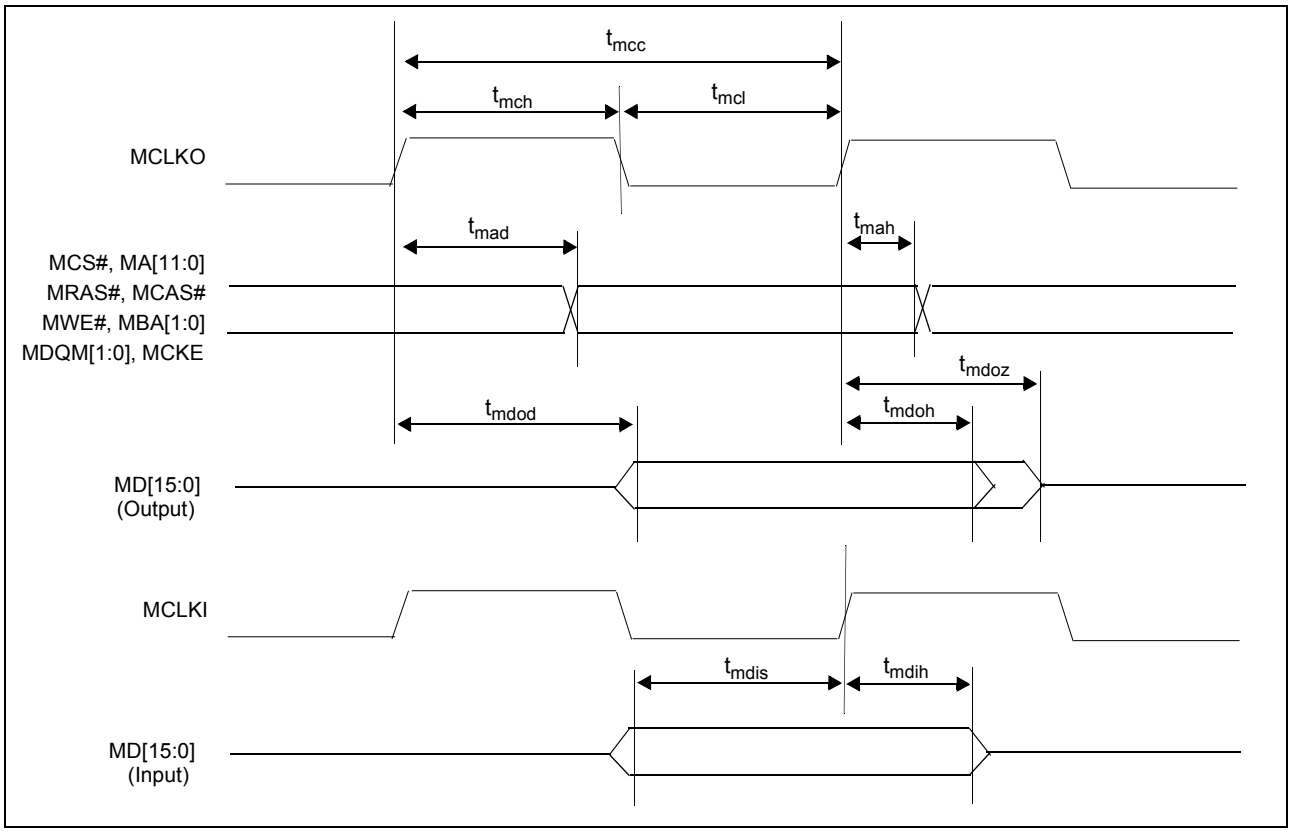


Figure 8-9: SDRAM Interface Timing

Table 8-11: SDRAM Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{mcc}	MCLKO period (note 1)	10	—	ns
t_{mcl1}	MCLKO Low pulse width	$0.3t_{mcc}$ - 2	—	ns
t_{mcl2}	MCLKO Low pulse width (note 2)	$0.5t_{mcc}$ - 2	—	ns
t_{mch1}	MCLKO High pulse width	$0.3t_{mcc}$ - 2	—	ns
t_{mch2}	MCLKO High pulse width (note 2)	$0.5t_{mcc}$ - 2	—	ns
t_{mad}	SDRAM control signals delay time	—	7	ns
t_{mah}	SDRAM control signals hold time	1	—	ns
t_{mdod}	SDRAM data signal delay time	—	7	ns
t_{mdoh}	SDRAM data signal hold time	1	—	ns
t_{mdoz}	SDRAM data output signal Hi-Z time	—	9	ns
t_{mdis}	SDRAM data input signal setup time	3	—	ns
t_{mdih}	SDRAM data input hold time	2	—	ns

Note

1. MCLKO period (MIN) = (1/PLL frequency) / 2 - 1ns - SS jitter width.
2. When REG[08h] bit 0 is set 1b, PLL output is divided to 1/2 clock.

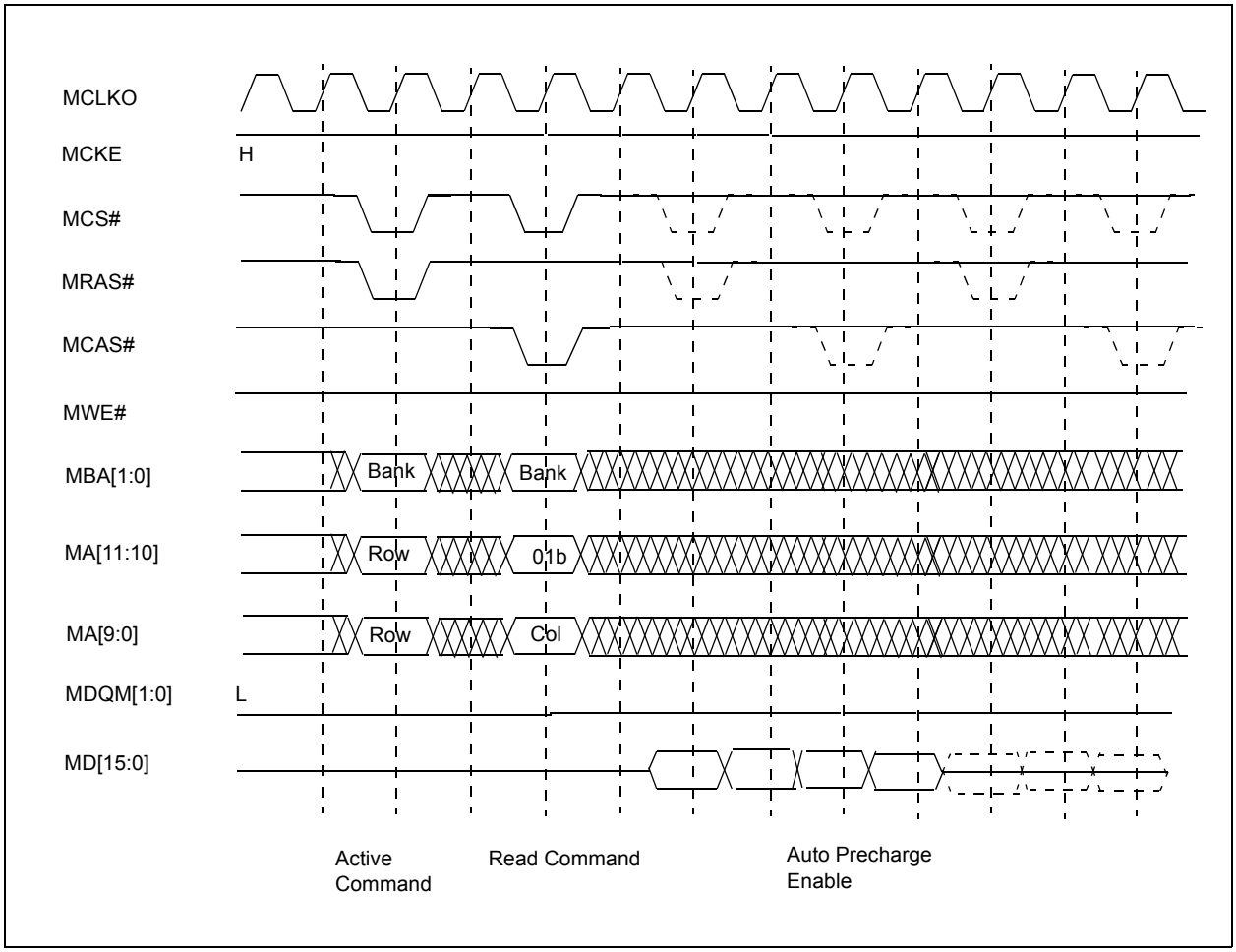


Figure 8-10: SDRAM Read Timing

Note
Burst length = 4 and CAS latency = 2 are fixed.

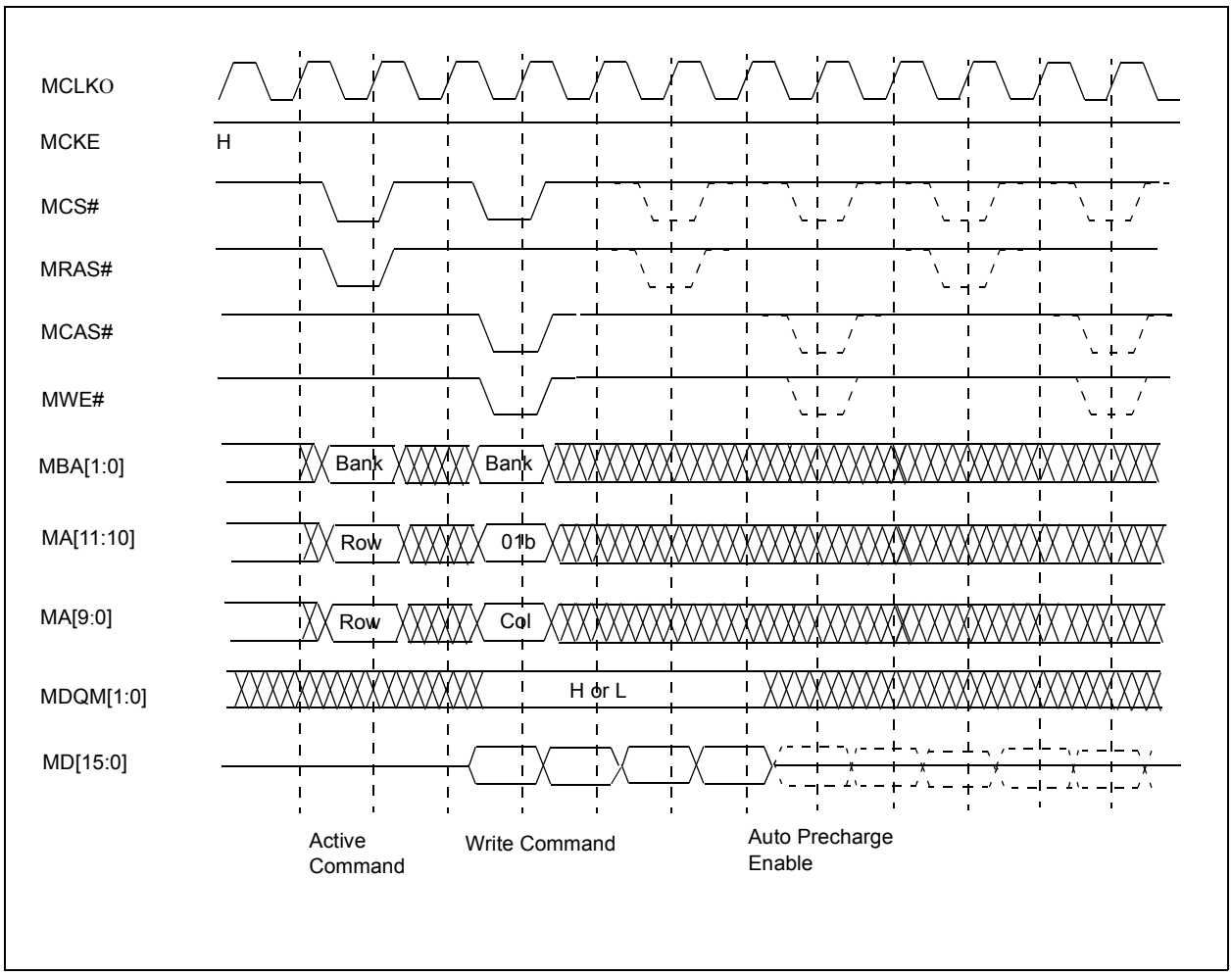


Figure 8-11: SDRAM Write Timing

Note
Burst Length = 4 is fixed.

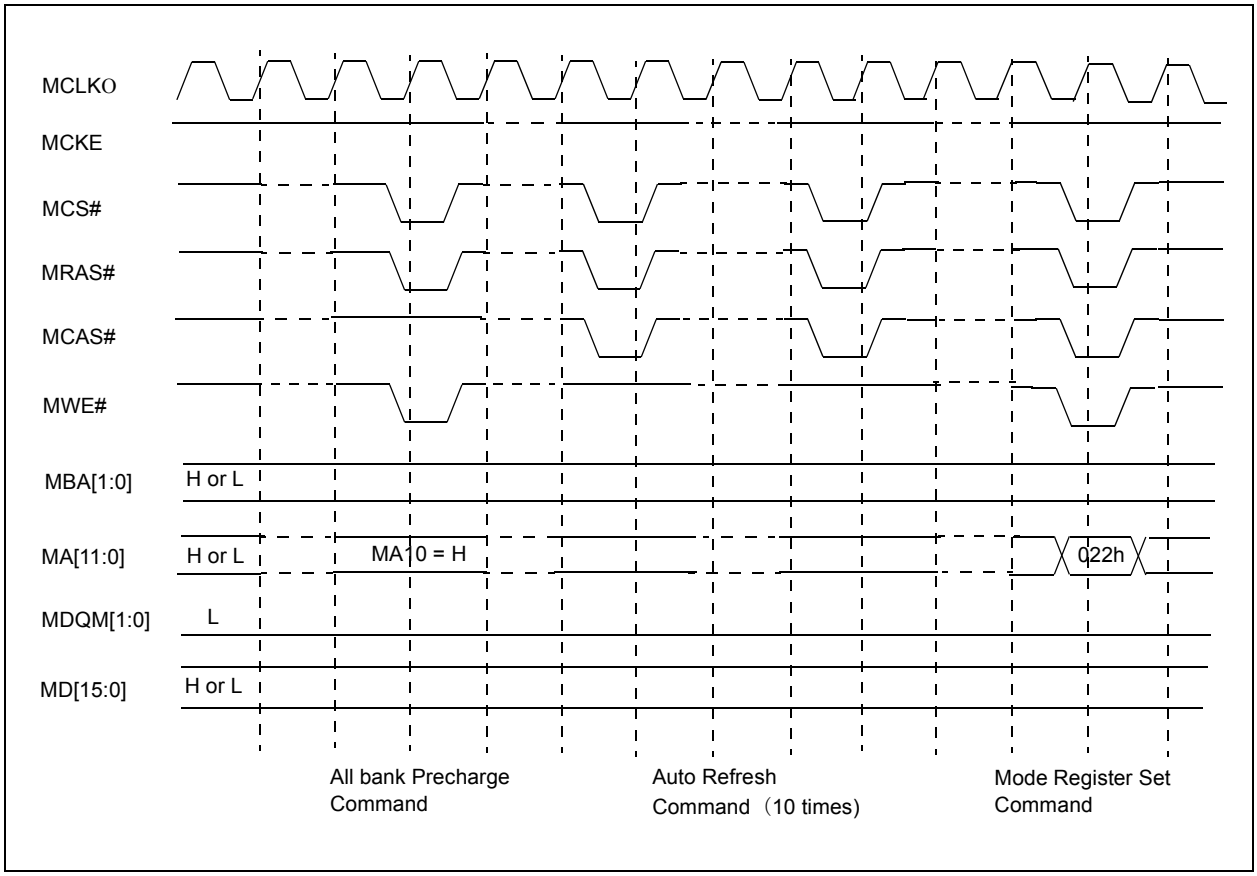


Figure 8-12: SDRAM Initialization Timing

Note

The initialization sequence is started by setting the SDRAM Initialization bit (REG[84h] bit 1 = 1b). After power-on/reset, the initialization sequence can be run only once. The initialization sequence requires 30,000 MCLKO cycles.

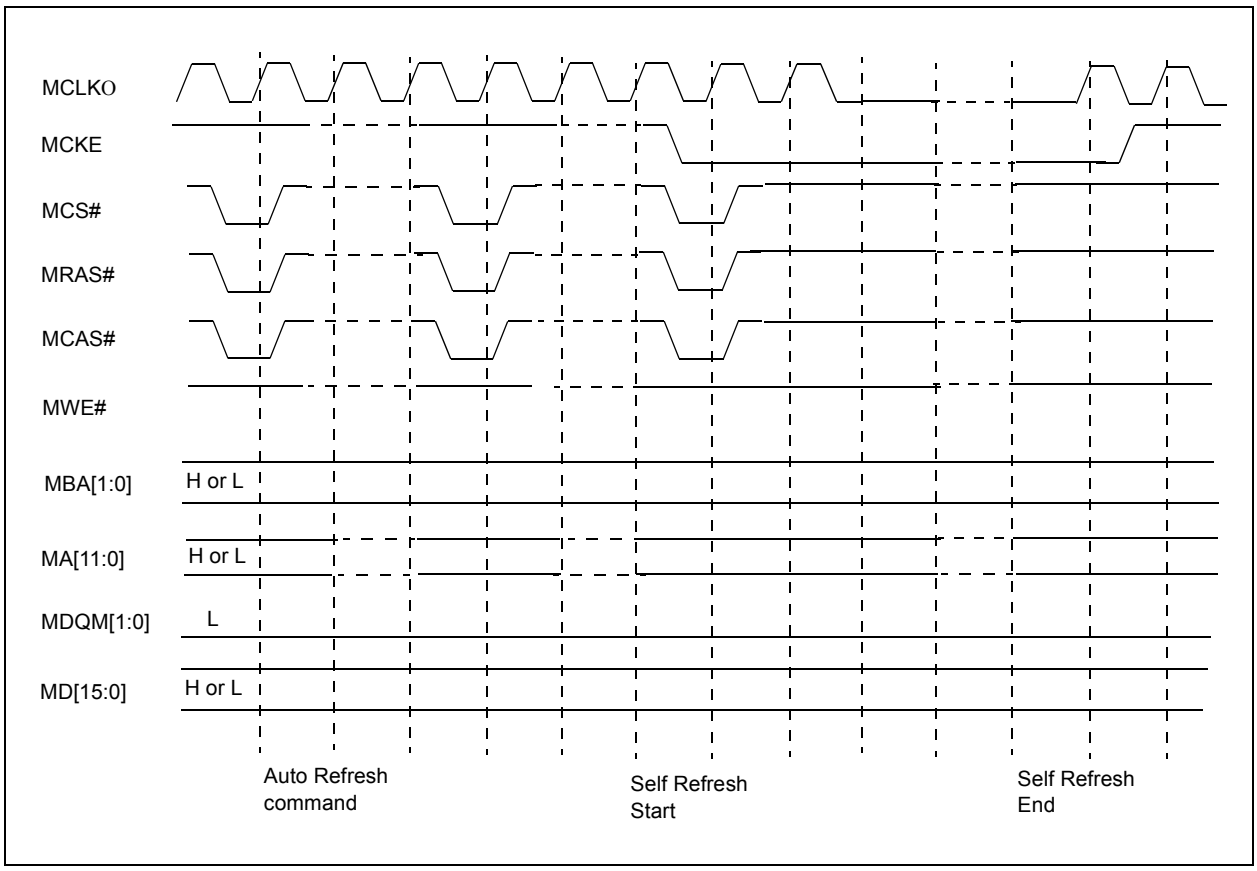


Figure 8-13: Auto Refresh / Self Refresh Timing

Note

Auto refresh time = (REG[8Eh], REG[8Ch] counter value) / f_{SDCLK}

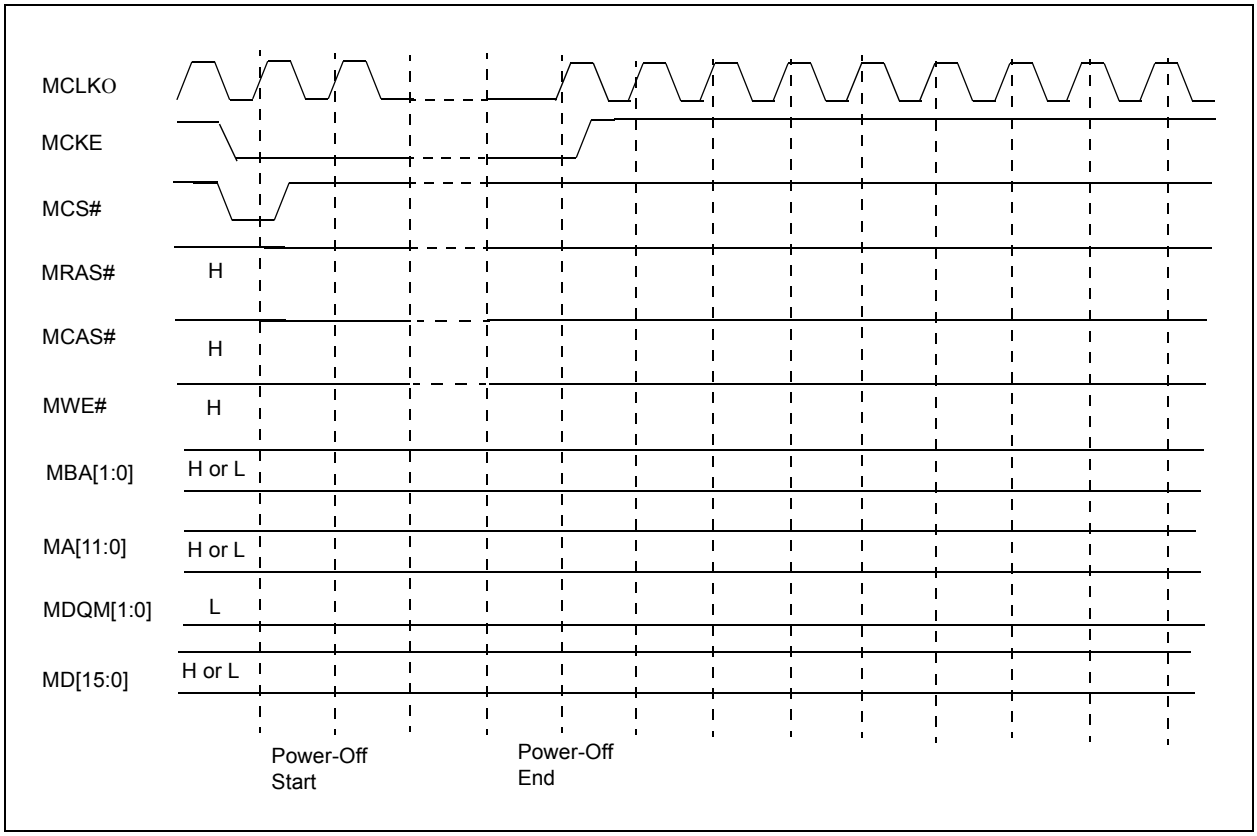


Figure 8-14: Power-Off Timing

Note
When the power-off mode is started, the control signals are forced to high level output so the SDRAM power is never shut down.

8.6 LCD Interface Timing

The timing parameters required to drive a flat panel display are shown below. Timing details for each supported panel type are provided in the remainder of this section.

Note
All timing measurements are taken to/from the 1/2*IOVDD level in the following display interface timing diagrams.

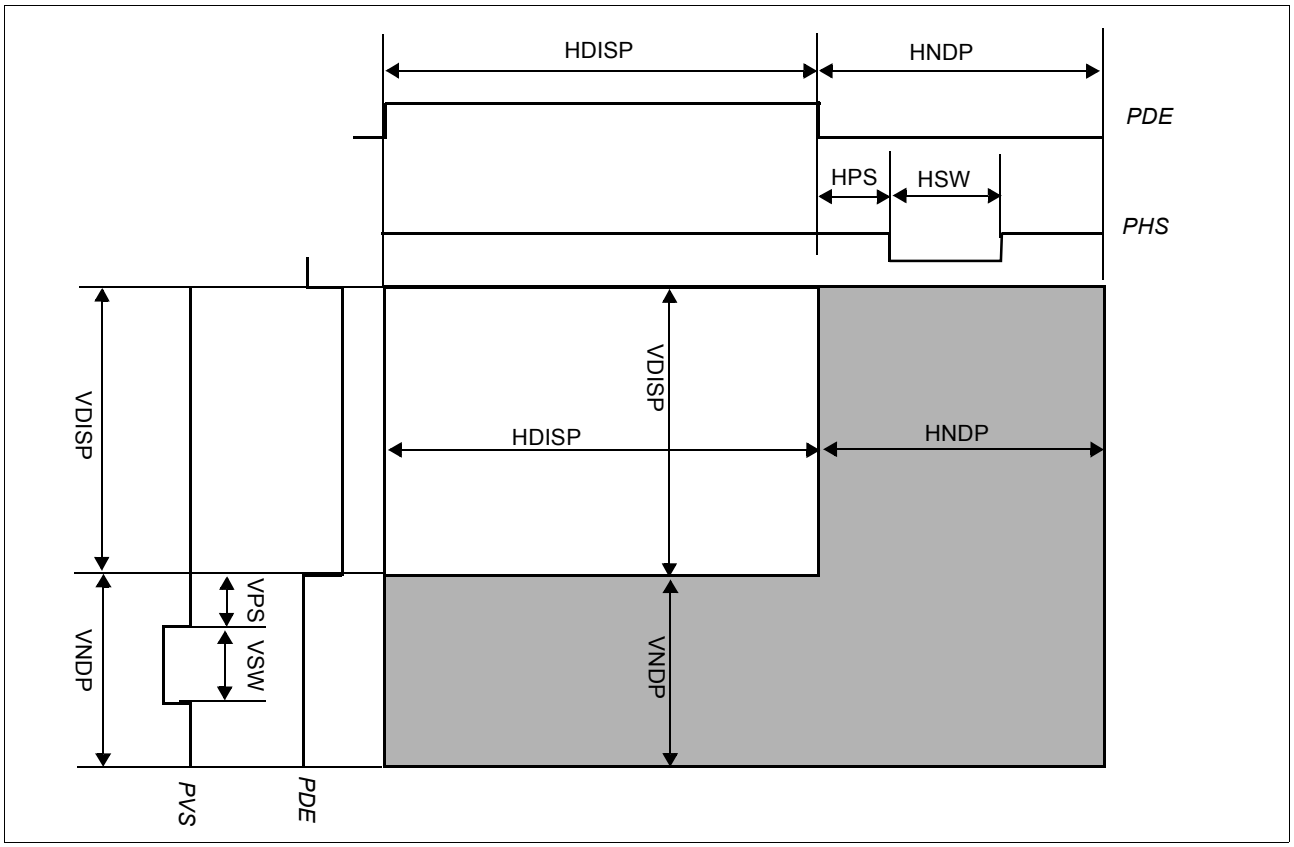


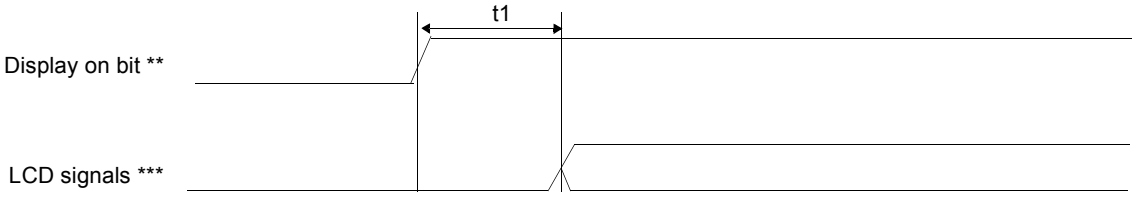
Figure 8-15: Panel Timing Parameters

Table 8-12: Panel Timing Parameters

Symbol	Description	Register	Min	Max	Units
HDISP	Horizontal Display Width	((REG[16h] bits 6-0) + 1) x 8	32	960	Ts (Note 1)
HNDP	Horizontal Non-Display Period	((REG[18h] bits 7-0) + 1) x 2	4	512	
HPS	PHS Pulse Start Position	(REG[22h] bits 6-0)	0	127	
HSW	PHS Pulse Width	(REG[20h] bits 6-0) + 1	1	128	
VDISP	Vertical Display Height	(REG[1Ch] bits 1-0, REG[1Ah] bits 7-0) + 1	32	960	Line
VNDP	Vertical Non-Display Period	((REG[1Eh bits 7-0) + 1) x 2	4	512	
VPS	PVS Pulse Start Position	(REG[26h] bits 7-0)	0	255	
VSW	PVS Pulse Width	(REG[24h] bits 5-0) + 1	1	64	

Note
Ts = 1/PCLK

8.6.1 LCD Panel Power-on Sequence



**The LCD power-on sequence is activated by programming the Display on bit（REG[2Ah] bit 0) from 0b to 1b.

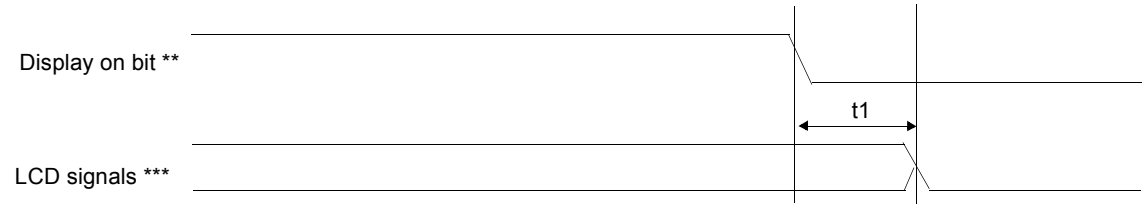
***LCD signals include: PDR[7:0], PDG[7:0], PDB[7:0], PCLK, PHS, PVS and PDE.

Figure 8-16: LCD Panel Power-on Sequence Timing

Table 8-13: LCD Panel Power-on Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Display on to LCD signals active	0	10	Ts

8.6.2 LCD Panel Power-off Sequence



** The LCD power-off sequence is activated by programming the Display on bit（REG[2Ah] bit0) from 1b to 0b.

*** LCD signals include: PDR[7:0], PDG[7:0], PDB[7:0], PCLK, PHS, PVS and PDE

Figure 8-17: LCD Panel Power-off Sequence Timing

Table 8-14: LCD Panel Power-off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Display off to LCD signals inactive	0	10	Ts

8.6.3 LCD Panel Timing

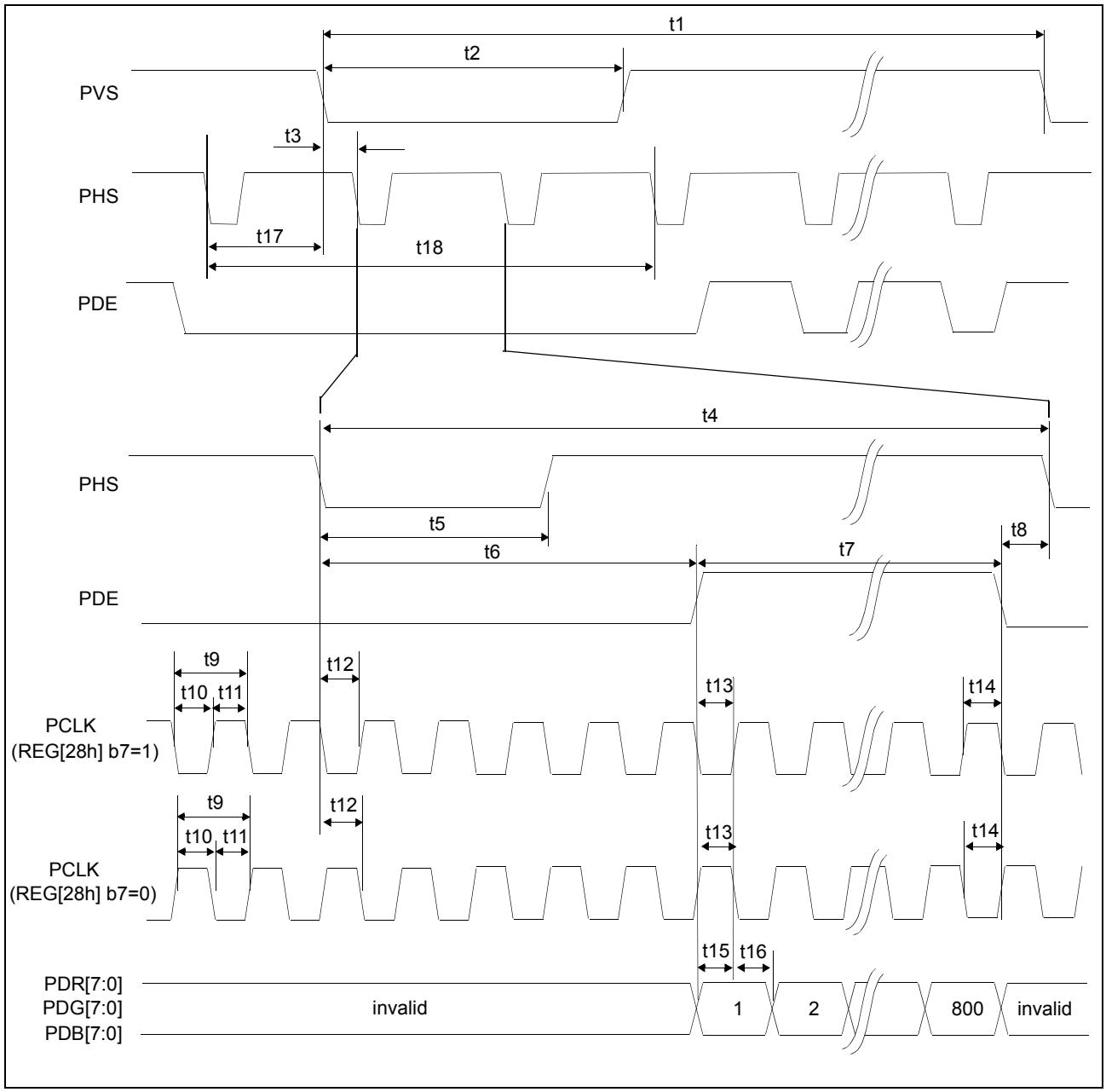


Figure 8-18: LCD Panel Timing

Note
PHS, PVS and PCLK have Polarity Select bits REG[20h] bit 7, REG[24] bit 7, and REG[28] bit 7 respectively.

Table 8-15: LCD Panel Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	PVS cycle time	—	VDISP + VNDP	—	Lines
t2	PVS pulse width Low	—	VSW	—	Lines
t3	PVS falling edge to PHS rising edge phase difference	—	HPS	—	Ts
t4	PHS cycle time	—	HDISP + HNDP	—	Ts
t5	PHS pulse width Low	—	HSW	—	Ts
t6	PHS falling edge to PDE active	—	HNDP - HPS	—	Ts
t7	PDE pulse width	—	HDISP	—	Ts
t8	PDE falling edge to PHS falling edge	—	HPS	—	Ts
t9	PCLK period	1	—	—	Ts
t10	PCLK pulse width Low	0.5	—	—	Ts
t11	PCLK pulse width High	0.5	—	—	Ts
t12	PHS setup to PCLK falling edge	0.5	—	—	Ts
t13	PDE to PCLK rising edge setup time	0.5	—	—	Ts
t14	PCLK rising edge to PDE hold time	0.5	—	—	Ts
t15	Data setup to PCLK rising edge	0.5	—	—	Ts
t16	PCLK rising edge to data hold time	0.5	—	—	Ts
t17	PDE stop setup to PVS start	—	VPS	—	Ts
t18	Vertical non-display period	—	VNDP	—	Ts

1. Ts = Pixel clock period

8.6.4 LCD Interface Timing

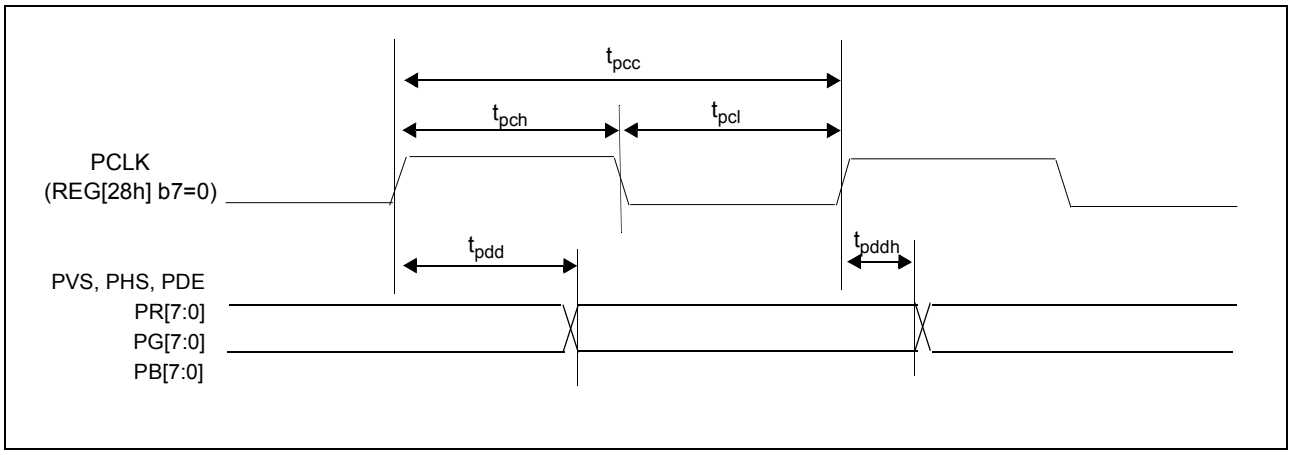


Figure 8-19: LCD Interface Timing

Table 8-16: LCD Interface Timing

Symbol	Parameter	MIN	MAX	Units
t_{pcc}	PCLK cycle time (note)	20	—	ns
t_{pcl}	PCLK pulse width Low	t_{pcc} * 0.4	—	ns
t_{pch}	PCLK pulse width High	t_{pcc} * 0.4	—	ns
t_{pdd}	LCD signals output delay time	—	5	ns
t_{pdh}	LCD signals output hold time	0	—	ns

Note
PCLK cycle time (MIN) = ((1/PLL frequency) / 2 - 1ns - SS jitter width) * 2 (or 3)

Chapter 9 Clocks

9.1 Clock Descriptions

An external clock is applied to the CLKI pin

The clock signal is applied to the CLKI pin. The clock to which are done with PLL is SDRAM clock (SDCLK). The clock that 1/2 dividing frequency or 1/3 dividing is system clocks (SYSYCLK) from SDCLK. Pixel clock (PCLK) becomes the same clock as SYSCLK.

Spread Spectrum modulation (SS) can be added to SDCLK or SYSCLK (however, the frequency range is limited to 31MHz ~ 80MHz.).

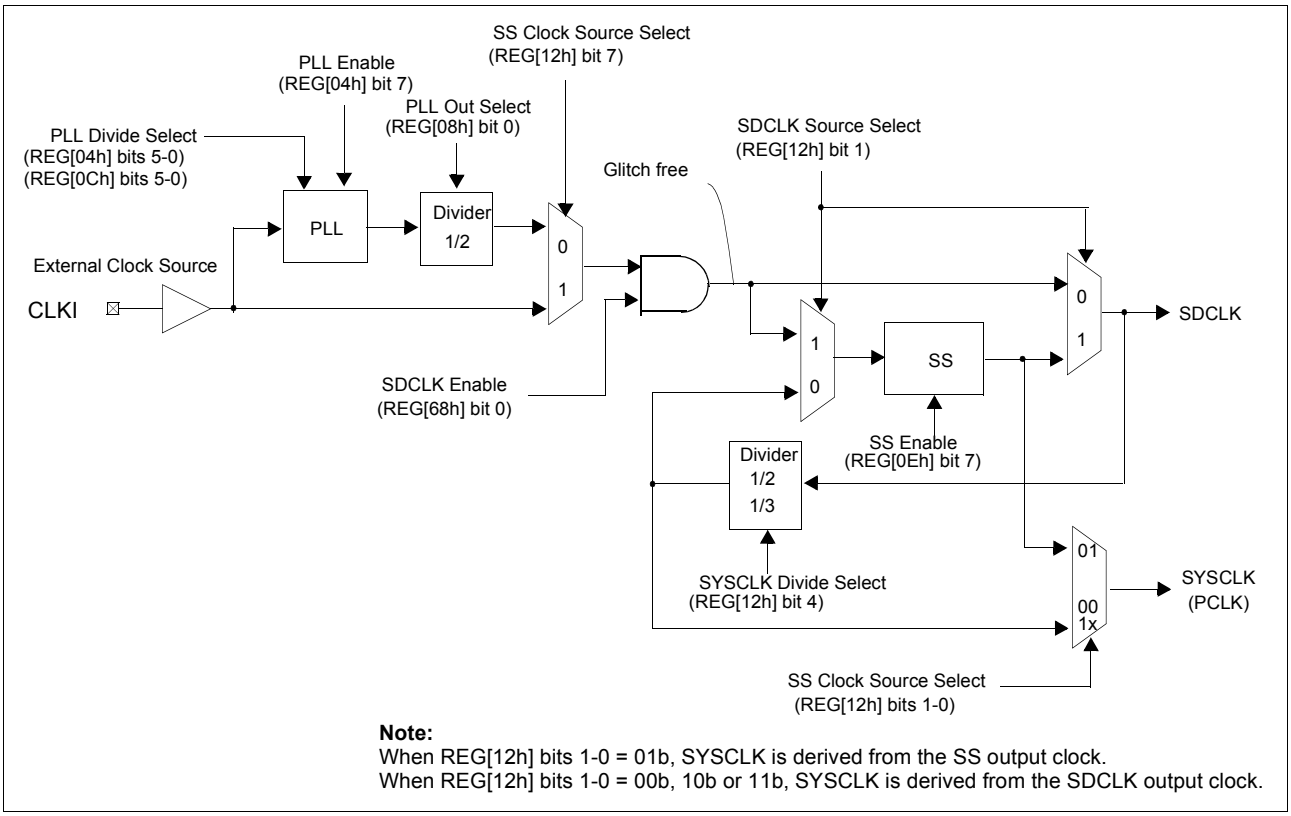


Figure 9-1: Clock Block Diagram

Table 9-1: Clock Selection

Selection	SDCLK : SYSCLK	SDCLK	SS (SDCLK)	SYSCLK (= PCLK)	SS (SYSCLK)
Selection 1	3:1	25~90MHz	not used	8.3~30MHz	not used
Selection 2	2:1	62~90MHz	not used	31~45MHz	used
Selection 3	3:1	32~80MHz	used	10.6~26.6MHz	used
Selection 4	2:1	32~80MHz	used	16~40MHz	used

9.2 Clock Function

The following table summarizes the internal clocks that are required for various S1D13517 functions.

Table 9-2: Clock Function

Function	CLKI Input	SYSCLK	SDCLK
Hardware reset	not required	not required	not required
Register access	not required	not required	not required
Memory access	required	required	required
LCD display	required	required	required
PWM output	required	required	not required
GPO output	not required	not required	not required
LCD display (Test color-bar)	required	required	not required

Note
Register accesses do not require an internal clock as the S1D13517 creates a clock from the bus cycle alone.

9.3 Clock Control

The internal clocks can be controlled by register settings.

Table 9-3: Clock Control

Register Setting	LCD	PWM	Alpha-Blend	Others
REG[68h] bit 0 = 0b	Stop	Stop	Stop	Stop
REG[2Ah] bit 0 = 0b	Stop	Run	Run	Run
REG[70h] bit 2 = 0b	Run	Stop	Run	Run
REG[9Eh] bit 7 = 0b	Run	Run	Stop	Run

Note
All internal clocks are dependant on SDCLK.
When REG[68h] bit 0 = 1b, SDCLK is enabled and all internal clocks may be also enabled.
When REG[68h] bit 0 = 0b, SDCLK is disabled and all internal clocks are stopped.

9.4 Software Reset

Internal sub-system blocks may be software reset from within REG[68h]. All registers are never reset.

Table 9-4: Software Reset

Register Setting	LCD	PWM	Memory Controller	SDRAM Controller	Alpha-Blend
REG[68h] bit 7 = 1b	Reset	-	-	-	-
REG[68h] bit 6 = 1b	-	Reset	-	-	-
REG[68h] bit 5 = 1b	-	-	Reset	-	-
REG[68h] bit 4 = 1b	-	-	-	Reset	-
REG[68h] bit 3 = 1b	-	-	-	-	Reset

Note
When REG[68h] bit 0 = 0b the S1D13517 is in power save mode. When returning from power save mode, REG[68h] bit 0 = 1b, reset the LCD sub-system, the PWM sub-system, the memory (SDRAM) controller sub-system and the Alpha-Blend sub-system to re-initialize the sub-systems. When the SDRAM controller is reset, it is necessary to re-initialize the controller.

Chapter 10 Registers

This section discusses how and where to access the S1D13517 registers. It also provides detailed information about the layout and usage of each register.

Burst data writes to the register space are supported for all register write accesses, except write accesses to the Memory Data Port (REG[66h] ~ REG[67h]). All writes to these registers will auto-increment the internal memory address only.

10.1 Register Mapping

All registers and memory are accessed via the Host interface. All accesses are 8-bit only except for the Memory Data Port (REG[66h] ~ REG[67h]) which is accessed according to the configuration of the CNF0 pin (16-bit for CNF0 = 0b, 8-bit for CFN0 = 1b). For further information on this setting, see Section 6.4, “Configuration Options” on page 23.

10.2 Register Set

The S1D13517 registers are listed in the following table.

Table 10-1: S1D13517 Register Set

Register	Pg	Register	Pg
Read-Only Configuration Registers			
REG[00h] Product Code Register	54	REG[02h] Configuration Readback Register	54
Clock Configuration Registers			
REG[04h] PLL D-Divider Register	55	REG[06h] PLL Setting Register 0	56
REG[08h] PLL Setting Register 1	56	REG[0Ah] PLL Setting Register 2	56
REG[0Ch] PLL N-Divider Register	57	REG[0Eh] SS Control Register 0	58
REG[10h] SS Control Register 1	58	REG[12h] Clock Source Select Register	59
Panel Configuration Registers			
REG[14h] LCD Panel Type Register	60	REG[16h] Horizontal Display Width Register (HDISP)	60
REG[18h] Horizontal Non-Display Period Register (HNDP)	61	REG[1Ah] Vertical Display Height Register 0 (VDISP)	61
REG[1Ch] Vertical Display Height Register 1 (VDISP)	61	REG[1Eh] Vertical Non-Display Period Register (VNDP)	61
REG[20h] PHS Pulse Width Register (HSW)	62	REG[22h] PHS Pulse Start Position Register (HPS)	62
REG[24h] PVS Pulse Width Register (VSW)	62	REG[26h] PVS Pulse Start Position Register (VPS)	63
REG[28h] PCLK Polarity Register	63		
Display Mode Registers			
REG[2Ah] Display Mode Register	64	REG[2Ch] PIP1 Display Start Address Register 0	65
REG[2Eh] PIP1 Display Start Address Register 1	65	REG[30h] PIP1 Display Start Address Register 2	65
REG[32h] PIP1 Window X Start Position Register	66	REG[34h] PIP1 Window Y Start Position Register 0	66
REG[36h] PIP1 Window Y Start Position Register 1	66	REG[38h] PIP1 Window X End Position Register	67
REG[3Ah] PIP1 Window Y End Position Register 0	67	REG[3Ch] PIP1 Window Y End Position Register 1	67
REG[3Eh] PIP2 Display Start Address Register 0	68	REG[40h] PIP2 Display Start Address Register 1	68
REG[42h] PIP2 Display Start Address Register 2	68	REG[44h] PIP2 Window X Start Position Register	68
REG[46h] PIP2 Window Y Start Position Register 0	69	REG[48h] PIP2 Window Y Start Position Register 1	69

Table 10-1: S1D13517 Register Set (Continued)

Register	Pg	Register	Pg
REG[4Ah] PIP2 Window X End Position Register	69	REG[4Ch] PIP2 Window Y End Position Register 0	70
REG[4Eh] PIP2 Window Y End Position Register 1	70	REG[50h] Display Control Register	71
Input Mode Registers			
REG[52h] Input Mode Register	72	REG[54h] Transparency Key Color Red Register	73
REG[56h] Transparency Key Color Green Register	73	REG[58h] Transparency Key Color Blue Register	74
REG[5Ah] Write Window X Start Position Register	74	REG[5Ch] Write Window Y Start Position Register 0	74
REG[5Eh] Write Window Y Start Position Register 1	74	REG[60h] Write Window X End Position Register	75
REG[62h] Write Window Y End Position Register 0	75	REG[64h] Write Window Y End Position Register 1	75
Memory Access Registers			
REG[66h] Memory Data Port Register 0	76	REG[67h] Memory Data Port Register 1	76
Miscellaneous Registers			
REG[68h] Power Save Register	77	REG[6Ah] Non-Display Period Control / Status Register	78
General Purpose Output Pins Registers			
REG[6Ch] General Purpose Output Register 0	79	REG[6Eh] General Purpose Output Register 1	79
PWM Registers			
REG[70h] PWM Control Register	80	REG[72h] PWM High Duty Cycle Register 0	81
REG[74h] PWM High Duty Cycle Register 1	81	REG[76h] PWM High Duty Cycle Register 2	81
REG[78h] PWM High Duty Cycle Register 3	81	REG[7Ah] PWM Low Duty Cycle Register 0	82
REG[7Ch] PWM Low Duty Register 1	82	REG[7Eh] PWM Low Duty Register 2	82
REG[80h] PWM Low Duty Register 3	82		
SDRAM Control Registers			
REG[82h] SDRAM Control Register	83	REG[84h] SDRAM Status Register 0	83
REG[86h] SDRAM Status Register 1	84	REG[88h] SDRAM MRS Value Register 0	85
REG[8Ah] SDRAM MRS Value Register 1	85	REG[8Ch] SDRAM Refresh Counter Register 0	85
REG[8Eh] SDRAM Refresh Counter Register 1	85	REG[90h] SDRAM Write Buffer Memory Size Register 0	86
REG[92h] SDRAM Debug Register	86		
Alpha-Blend Registers			
REG[94h] Alpha-Blend Control Register	87	REG[96h] is Reserved	87
REG[98h] Alpha-Blend Horizontal Size Register	88	REG[9Ah] Alpha-Blend Vertical Size Register 0	88
REG[9Ch] Alpha-Blend Vertical Size Register 1	88	REG[9Eh] Alpha-Blend Value Register	88
REG[A0h] Alpha-Blend Input Image 1 Start Address Register 0	89	REG[A2h] Alpha-Blend Input Image 1 Start Address Register 1	89
REG[A4h] Alpha-Blend Input Image 1 Start Address Register 2	89	REG[A6h] Alpha-Blend Input Image 2 Start Address Register 0	90
REG[A8h] Alpha-Blend Input Image 2 Start Address Register 1	90	REG[AAh] Alpha-Blend Input Image 2 Start Address Register 2	90
REG[ACh] Alpha-Blend Output Image Start Address Register 0	90	REG[AEh] Alpha-Blend Output Image Start Address Register 1	90
REG[B0h] Alpha-Blend Output Image Start Address Register 2	90		
Interrupt Registers			
REG[B2h] Interrupt Control Register	91	REG[B4h] Interrupt Status Register	92
REG[B6h] Interrupt Clear Register	92		

10.3 Register Descriptions

All reserved bits must be set to the default value. Writing a non-default value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. Unless specified otherwise, all register bits are set to 0b during power-on reset.

10.3.1 Read-Only Configuration Registers

REG[00h] Product Code Register
Default = B8h — Read Only

Product Code bits 5-0						Revision Code bits 1-0	
7	6	5	4	3	2	1	0

bits 7-2 Product Code bits [5:0] (Read Only)
These read-only bits indicate the product code. The product code for the S1D13517 is 101110b.

bits 1-0 Revision Code bits [1:0] (Read Only)
These read-only bits indicate the revision code. The revision code is 00b.

REG[02h] Configuration Readback Register
Default = XXh — Read Only

n/a					CNF2 Status	CNF1 Status	CNF0 Status
7	6	5	4	3	2	1	0

bits 2-0 CNF[2:0] Status (Read Only)
These read-only status bits return the status of the configuration pins CNF[2:0]. For details on CNF[2:0] functionality, see Section 6.4, “Configuration Options” on page 23.

10.3.2 Clock Configuration Registers

REG[04h] PLL D-Divider Register Default = 01h							Read/Write
PLL Enable	n/a	D-Divider bits 5-0					
7	6	5	4	3	2	1	0

bit 7 PLL Enable

This bit enables the PLL output.

When this bit = 0b, the PLL is disabled.

When this bit = 1b, the PLL is enabled.

Note

All other PLL registers must be set before enabling SS or PLL. SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of this bit. Do not change this bit while operating.

bits 5-0 D-Divider bits [5:0]

These bits determine the divide ratio between CLKI and the actual input clock to the PLL

Note

Depending on CLKI, these bits must be set such that the internal input clock to the PLL (PLLCLK) is between 1Mhz ~ 2MHz.

Table 10-2: PLL D-Divide Selection

REG[04h] Bits 5-0	D-Divide Ratio
0h	Reserved
01h	2:1 (Default)
02h	3:1
03h	4:1
• • •	• • •
3Eh	63:1
3Fh	64:1

REG[06h] PLL Setting Register 0
Default = 01h — Read/Write

n/a	VC bits 2-0			n/a	Reserved		
7	6	5	4	7	2	1	0

bits 6-4 VC bits [2:0]
These bits determine the frequency of the VCO.

Table 10-3: VC Selection

REG[06h] Bits 6-4	PLL Frequency
000b	50 ~ 100MHz
100b	102 ~ 140MHz
101b	142 ~ 180MHz

bits 2-0 Reserved
The default value for these bits are 001b.

REG[08h] PLL Setting Register 1
Default = 00h — Read/Write

n/a	Reserved						PLL Clock Divide By 2
7	6	5	4	3	2	1	0

bits 6-1 Reserved
The default value of these bits is 000000b.

bit 0 PLL Clock Divide By 2
This bit selects whether the PLL output is divided or not. See Chapter 9, “Clocks” on page 49 for a summary of the clock structure.
When this bit = 0b, PLL clock is not divided.
When this bit = 1b, the PLL clock is divided by 2.

REG[0Ah] PLL Setting Register 2
Default = 08h — Read/Write

n/a				Reserved			
7	6	5	4	3	2	1	0

This register must be programmed with the value 08h.

REG[0Ch] PLL N-Divider Register
Default = 00h Read/Write

Reserved	N-Counter bits 6-0						
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bits 6-0 N-Counter bits [6:0]
These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output =((N-Counter + 1) x 2) x PLLCLKI
= NN x PLLCLKI

Where:
PLL Output is the desired PLL output frequency (in MHz).
N-Counter is the value of this register (in decimal).
PLLCLKI is the internal input clock to the PLL (1MHz ~ 2MHz).

Note
1. The PLL output range is minimum 50MHz (REG[0Ch] = 18h), and maximum 180MHz (REG[0Ch] = 59h).
2. The composition of a recommended external low-pass filter changes depending on PLL output frequency. See Chapter 18, “PLL” on page 131 for further information.

Table 10-4 PLL Setting Example

Target Frequency (MHz)	NN	REG[06h]	REG[08h]	REG[0Ch]	CLKI Input Clock (MHz)	D-Divide Ratio	REG[04h]
60	60	01h	00h	1Dh	24	24:1	17h
66	66	01h	00h	20h	24	24:1	17h
80	80	01h	00h	27h	27	27:1	1Ah
90	90	01h	00h	2Ch	27	27:1	1Ah
60	120	41h	01h	3Bh	24	24:1	17h
66	132	41h	01h	41h	24	24:1	17h
80	160	51h	01h	4Fh	24	24:1	17h
90	180	51h	01h	59h	24	24:1	17h

REG[0Eh] SS Control Register 0
Default = 3Fh Read/Write

Spread Spectrum Enable	n/a	Reserved					
7	6	5	4	3	2	1	0

bit 7 Spread Spectrum Enable.
This bit controls Spread Spectrum (SS) modulation.
When this bit = 0b, SS modulation is disabled.
When this bit = 1b, SS modulation is enabled.

Note
Program the SS setting registers before enabling SS or PLL. Disable SDCLK (REG[68h] bit 0 = 0b) before changing the value of this bit. Do not change this bit while operating. The frequency for which SS can be used is 31MHz ~ 80MHz.

bits 5-0 Reserved
The default value for these bits is 11_1111b.

REG[10h] SS Control Register 1
Default = 41h Read/Write

Reserved	W-Counter bits 2-0			Reserved			
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bits 6-4 W-Counter bits [2:0]
These bits set the width of the SS output frequency change.

Table 10-5: W-Counter Selection

REG[10h] bits 6-4	Width of Frequency Change (TYP)
000b	+/- 0.25ns
001b	+/- 0.35ns
010b	+/- 0.45ns
011b	+/- 0.55ns
100b	+/- 0.65ns (default)
All Other Values	Reserved

bits 3-0 Reserved
The default value for these bits is 0001b.

REG[12h] Clock Source Select Register
Default = 00h Read/Write

SDCLK Source Select	n/a		SYSCLK DIvide Select	n/a		SS Clock Source Select bits 1-0	
7	6	5	4	3	2	1	0

bit 7 SDCLK Source Select

This bit selects the source of the external SDRAM clock (SDCLK) for the S1D13517. For details on the clock structure see Chapter 9, “Clocks” on page 49.
When this bit = 0b, the SDCLK source is the external CLKI input.
When this bit = 1b, the SDCLK source is the internal PLL.

Note
The PLL output will become stable after 10ms.

bit 4 SYSCLK Divide Select

This bit specifies the divide ratio of the internal system clock (SYSCLK) from the SDCLK. For details on the clock structure see Chapter 9, “Clocks” on page 49.
When this bit = 0b, the divide ratio of SYSCLK is 1:3.
When this bit = 1b, the divide ratio of SYSCLK is 1:2.

Note
SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of this bit. Please do not change this bit while operating. +

bits 1-0 SS Clock Source Select bits [1:0]

These bits select the source for the SS clock. For details on the clock structure see Chapter 9, “Clocks” on page 49.

Table 10-6: SS Clock Source Selection

REG[12h] bits 1-0	SS Clock Source
00b	SS is not used
01b	SYSCLK
1xb	SDCLK

Note
SDCLK must be disabled (REG[68h] bit 0 = 0b) before changing the value of these bits. Please do not change while operating.

Note
The frequency for which SS can be used is 31MHz ~ 80MHz.

10.3.3 Panel Configuration Registers

REG[14h] LCD Panel Type Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a					Input Image Format bits 1-0		Panel Data Width

bits 2-1 Input Image Format bits [1:0]
These bits select the input image format. For details on these formats see Section 11.2, “Color Formats” on page 98.

Table 10-7: Input Image Format Setting

REG[14h] bits 1-0	Input Image Format
00b	24bpp (RGB 8:8:8) mode 1
01b	24bpp (RGB 8:8:8) mode 2
1xb	16bpp (RGB 5:6:5)

Note
Input image data is always stored in memory as RGB 8:8:8. For details see Section 13.4, “Memory Data” on page 119.

bit 0 Panel Data Width
This bit specifies the data width for the LCD interface.
When this bit = 0b, the LCD interface is configured as 24-bit (1 pixel / clock).
When this bit = 1b, the LCD interface is configured as 18-bit (1 pixel / clock).

REG[16h] Horizontal Display Width Register (HDISP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a	Horizontal Display Width bits 6-0						

bits 6-0 Horizontal Display Width bits [6:0]
These bits specify the Horizontal Display Width (HDISP) for the LCD panel, in 8 pixel resolution (bytes).

HDISP in number of pixels = ((REG[16h] bits 6-0) + 1)× 8

Note
The minimum Horizontal Display Width is 32 pixels and the maximum is 960 pixels.

REG[18h] Horizontal Non-Display Period Register (HNDP)
Default = 00h Read/Write

Horizontal Non-Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Horizontal Non-Display Period bits [7:0]
These bits specify the Horizontal Non-Display Period (HNDP) for the LCD panel, in pixels.
HNDP in pixels = ((REG[18h] bits 7-0) + 1) x 2

Note
The minimum Horizontal Non-Display Period is 4 pixels and the maximum is 512 pixels.
HPS + HSW <= HNDP

REG[1Ah] Vertical Display Height Register 0 (VDISP)
Default = 01h Read/Write

Vertical Display Height bits 7-0							
7	6	5	4	3	2	1	0

REG[1Ch] Vertical Display Height Register 1 (VDISP)
Default = 00h Read/Write

n/a						Vertical Display Height bits 9-8	
7	6	5	4	3	2	1	0

REG[1Ch] bits 1-0
REG[1Ah] bits 7-0 Vertical Display Height bits [9:0]
These bits specify the Vertical Display Height (VDISP) for the LCD panel, in lines.
VDISP in lines = (REG[1Ch] bits 1-0, REG[1Ah] bits 7-0) +1

Note
The minimum Vertical Display Height is 32 lines and the maximum is 960 lines.

REG[1Eh] Vertical Non-Display Period Register (VNDP)
Default = 01h Read/Write

Vertical Non-Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Vertical Non-Display Period bits [7:0]
These bits specify the Vertical Non-Display Period (VNDP) for the LCD panel, in lines.
VNDP in lines = ((REG[1Eh] bits 7-0) + 1) x 2

Note
The minimum Vertical Non-Display Period is 4 lines and the maximum is 512 lines.

REG[20h] PHS Pulse Width Register (HSW)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PHS Pulse Polarity	PHS Pulse Width bits 6-0						

bit 7 PHS Pulse Polarity
This bit selects the polarity of the horizontal sync signal. This bit is set according to the horizontal sync signal of the panel.
When this bit = 0b, the horizontal sync signal is active low.
When this bit = 1b, the horizontal sync signal is active high.

bits 6-0 PHS Pulse Width bits [6:0]
These bits specify the width of the horizontal sync signal (HSW) for the LCD panel, in pixels. The horizontal sync signal is typically PHS, depending on the panel type.
HSW in pixels = (REG[20h] bits 6-0) + 1

REG[22h] PHS Pulse Start Position Register (HPS)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a	PHS Pulse Start Position bits 6-0						

bits 6-0 PHS Pulse Start Position bits [6:0]
These bits specify the start position of the horizontal sync signal with respect to the start of Horizontal Non-Display period, in pixels.
HPS in pixels = REG[22h] bits 6-0

REG[24h] PVS Pulse Width Register (VSW)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PVS Pulse Polarity	n/a	PVS Pulse Width bits 5-0					

bit 7 PVS Pulse Polarity
This bit selects the polarity of the vertical sync signal. This bit is set according to the vertical sync signal of the panel.
When this bit = 0b, the vertical sync signal is active low.
When this bit = 1b, the vertical sync signal is active high.

bits 5-0 PVS Pulse Width bits [5:0]
These bits specify the width of vertical sync signal (VSW) for the LCD panel, in lines. The vertical sync signal is typically PVS, depending on the panel type.
VSW in lines = (REG[24h] bits 5-0) + 1

REG[26h] PVS Pulse Start Position Register (VPS)
Default = 00h Read/Write

PVS Pulse Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PVS Pulse Start Position bits [7:0]
These bits specify the start position of the vertical sync signal with respect to the start of Vertical Non-Display period (VPS), in lines.
VPS in lines = REG[26h] bits 7-0

REG[28h] PCLK Polarity Register
Default = 00h Read/Write

PCLK Polarity	n/a				Reserved		
7	6	5	4	3	2	1	0

bit 7 PCLK Polarity
This bit selects the polarity of PCLK.
When this bit = 0b, data is output on the rising edge of PCLK.
When this bit = 1b, data is output on the falling edge of PCLK.

bits 2-0 Reserved
The default value for these bits is 000b.

10.3.4 Display Mode Registers

REG[2Ah] Display Mode Register
Default = 00h — Read/Write

Main Screen Display Buffer Select bits 3-0				Display Data Output Select bits 1-0			Display Interface Enable
7	6	5	4	3	2	1	0

All changes, except to bit 0, entered into this register are not loaded into internal registers until REG[50h] bit 7 has been written with a 1b. Bit 0 is not synchronized with REG[50h] bit 7.

bits 7-4 Main Screen Display Buffer Select bits [3:0]
When the double buffer display is not selected, these bits select the writing buffer from 16 buffers.
When the double buffer display is selected (REG[2Ah] bits 3-1 = 001b), these bit are ignored. (Buffer 1 and 2 are fixed)

Table 10-8: Main Screen Display Buffer Selection

REG[2Ah] bits 7-4	Main Screen Display Buffer
0000b	Buffer 1
0001b	Buffer 2
0010b	Buffer 3
0011b	Buffer 4
0100b	Buffer 5
0101b	Buffer 6
0110b	Buffer 7
0111b	Buffer 8
1000b	Buffer 9
1001b	Buffer 10
1010b	Buffer 11
1011b	Buffer 12
1100b	Buffer 13
1101b	Buffer 14
1110b	Buffer 15
1111b	Buffer 16

bits 3-1 Display Data Output Select bits [2:0]
These bits are selected the display data. These bits can be update on LCD running.

Table 10-9: Display Data Output Selection

REG[2Ah] bits 3-1	Display Data Output
000b	Single buffer display (default)
001b	Double buffer display
010b	PIP1 screen display
011b	PIP2 screen display
100b	PIP1 and PIP2 screen display
101b	Display blanked (all lows output)
110b	Display blanked (all highs output)
111b	Test color bar display

bit 0 Display Interface Enable
Changes to this bit are not synchronized with REG[50h] bit 7 and occur immediately.
When this bit = 0b, the LCD display interface is disabled.
When this bit = 1b, the LCD display interface is enabled. The SDCLK should be enabled (REG[68h] bit 0 = 1) before the LCD display interface is enabled.

REG[2Ch] PIP1 Display Start Address Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 7-3					n/a		

REG[2Eh] PIP1 Display Start Address Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 15-8							

REG[30h] PIP1 Display Start Address Register 2
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Display Start Address bits 23-16							

REG[30h] bits 7-0
REG[2Eh] bits 7-0
REG[2Ch] bits 7-3 PIP1 Display Start Address bits [23:3]
These bits specify the start address of the PIP1 window image in the display buffer. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Display Start Address [23:3] = (REG[30h] bits 7-0, REG[2Eh] bits 7-0, REG[2Ch] bits 7-3)

REG[32h] PIP1 Window X Start Position Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Window X Start Position bits 9-3							n/a

bits 7-1 PIP1 Window X Start Position bits [9:3]
These bits determine the X start position of the PIP1 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window X Start Position = (REG[32h] bits 7-0) x 4 + 1

Note

1. The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7).
2. The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[34h] PIP1 Window Y Start Position Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP1 Window Y Start Position bits 9-2							

REG[36h] PIP1 Window Y Start Position Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						PIP1 Window Y Start Position bits 1-0	

REG[34h] bits 7-0
REG[36h] bits 1-0 PIP1 Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP1 Window in relation to the origin of the panel, in lines. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window Y Start Position = (REG [34h] bits 7-0, REG [36h] bits 1-0) + 1

Note

The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[38h] PIP1 Window X End Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP1 Window X End Position bits 9-3							n/a

bits 7-1 PIP1 Window X End Position bits [9:3]

These bits determine the X end position of the PIP1 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Window X End Position = (REG[38h] bits 7-0) x 4 + 8

Note

1. The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)
2. The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[3Ah] PIP1 Window Y End Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PIP1 Window Y End Position bits 9-2							

REG[3Ch] PIP1 Window Y End Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						PIP1 Window Y End Position bits 1-0	

REG[3Ah] bits 7-0
REG[3Ch] bits 1-0 PIP1 Window Y End Position bits [9:0]

These bits determine the Y end position of the PIP1 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP1 Display Window Y End Position = (REG[3Ah] bits 7-0, REG[3Ch] bits 1-0) + 1

Note

The PIP1 window must be positioned such that it remains within the dimensions of the LCD display.

REG[3Eh] PIP2 Display Start Address Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 7-3					n/a		

REG[40h] PIP2 Display Start Address Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 15-8							

REG[42h] PIP2 Display Start Address Register 2
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Display Start Address bits 23-16							

REG[42h] bits 7-0
REG[40h] bits 7-0
REG[3Eh] bits 7-3 PIP2 Display Start Address bits [23:3]

These bits specify the start address of the PIP2 window image in the display buffer. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Display Start Address A [23:3] = (REG[42h] bits 7-0, REG[40h] bits 7-0, REG[3Eh] bits 7-3)

REG[44h] PIP2 Window X Start Position Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Window X Start Position bits 9-3							n/a

bits 7-1 PIP2 Window X Start Position bits [9:3]

These bits determine the X start position of the PIP2 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window X Start Position = (REG[44h] bits 7-0) x 4 + 1

Note

1. The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7)
2. The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[46h] PIP2 Window Y Start Position Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Window Y Start Position bits 9-2							

REG[48h] PIP2 Window Y Start Position Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						PIP2 Window Y Start Position bits 1-0	

REG[46h] bits 7-0
REG[48h] bits 1-0 PIP2 Window Y Start Position bits 7-0 [9:0]

These bits determine the Y start position of the PIP2 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window Y Start Position = (REG [46h] bits 7-0, REG [48h] bits 1-0) + 1

Note

The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[4Ah] PIP2 Window X End Position Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PIP2 Window X End Position bits 9-3							n/a

bits 7-1 PIP2 Window X End Position bits [9:3]

These bits determine the X end position of the PIP2 Window in relation to the origin of the panel, in 8 pixel resolution (bytes). The value entered into this register is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window X End Position = (REG [4Ah] bits 7-0) x 4 + 8

Note

1. The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)
2. The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[4Ch] PIP2 Window Y End Position Register 0
Default = 00h Read/Write

PIP2 Window Y End Position bits 9-2							
7	6	5	4	3	2	1	0

REG[4Eh] PIP2 Window Y End Position Register 1
Default = 00h Read/Write

n/a						PIP2 Window Y End Position bits 1-0	
7	6	5	4	3	2	1	0

REG[4Ch] bits 7-0
REG[4Eh] bits 1-0 PIP2 Window Y End Position bits [9:0]

These bits determine the Y end position of the PIP2 Window in relation to the origin of the panel, in pixels. The value entered into these registers is not loaded into internal registers until REG[50h] bit 7 has been written with a 1b.

PIP2 Window Y End Position = (REG[4Ch] bits 7-0, REG[4Eh] the bits 1-0) + 1

Note

The PIP2 window must be positioned such that it remains within the dimensions of the LCD display.

REG[50h] Display Control Register

Default = not applicable — Write Only

7	6	5	4	3	2	1	0
Display Setting Register Update (WO)	n/a						

bit 7 Display Setting Register Update (Write Only)
When the display registers (REG[2Ah] ~ REG[4Eh]) are changed, except REG[2Ah] bit 0, this bit must be written 1b to update the internal register values. Writing 0b to this bit has no effect.

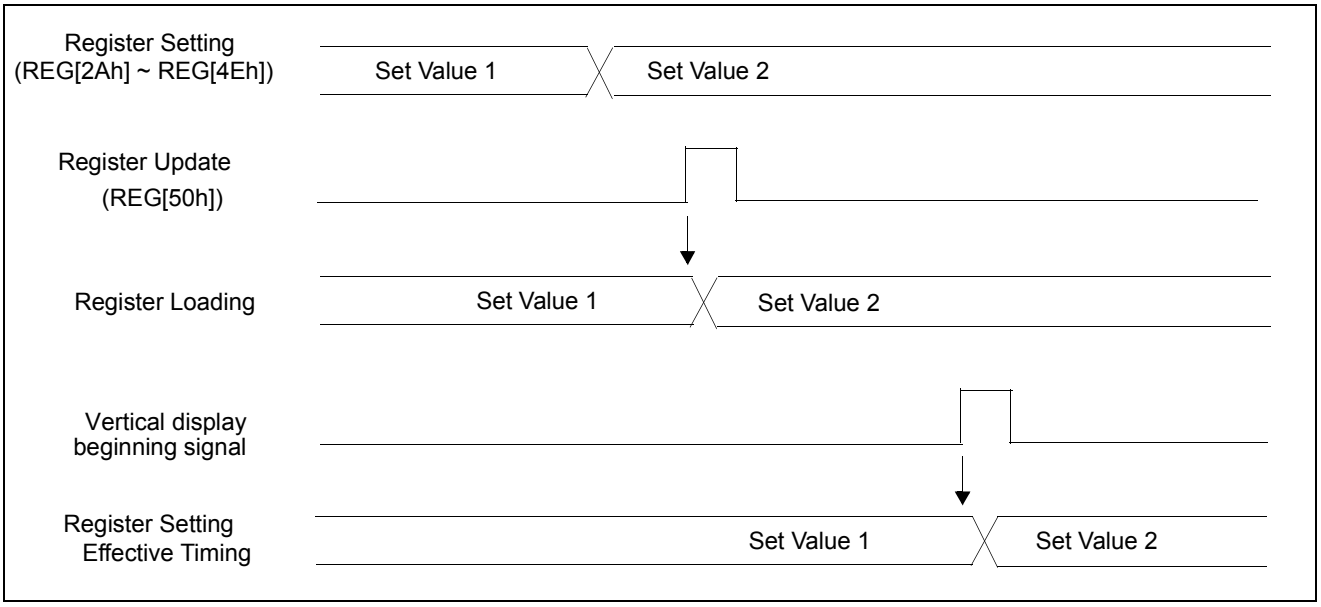


Figure 10-1: Display Setting Register Update Timing

10.3.5 Input Mode Registers

REG[52h] Input Mode Register
Default = 00h — Read/Write

Write Buffer Select bits 3-0				Transparency Enable	Reserved	Mirror Display Enable	Rotation Enable
7	6	5	4	3	2	1	0

bits 7-4 Write Buffer Select bits [3:0]

When double buffer display is not selected (REG[2Ah] bits 3-1 ≠ 001b), these bits select which write buffer will be written to by writes to the Memory Data Port registers (REG[66h] ~ REG[67h]). Up to 16 buffers are available based on the amount of memory and the Write Buffer Memory Size (see REG[90h]).

When the double buffer display is selected (REG[2Ah] bits 3-1 = 001b), these bits are ignored and Buffer 1 and 2 are fixed.

Table 10-10: Write Buffer Selection

REG[52h] bits 7-4	Write Buffer Selected
0000b	Buffer 1
0001b	Buffer 2
0010b	Buffer 3
0011b	Buffer 4
0100b	Buffer 5
0101b	Buffer 6
0110b	Buffer 7
0111b	Buffer 8
1000b	Buffer 9
1001b	Buffer 10
1010b	Buffer 11
1011b	Buffer 12
1100b	Buffer 13
1101b	Buffer 14
1110b	Buffer 15
1111b	Buffer 16

Note
These bits do not select the image data that is displayed. The display output (Main and PIP windows) is selected using the register settings in the Display Mode register (REG[2Ah])

bit 3 Transparency Enable

This bit controls whether the transparency function is enabled for writes to the write buffers. When transparency is enabled, image data that matches the transparency key color as defined by REG[54h] ~ REG[58h] will not be written to memory and the existing image data will remain. For further information on the transparency function, see Section 12.2, “Transparency” on page 106.

When this bit = 0b, the Transparency is disabled.
When this bit = 1b, the Transparency is enabled.

bit 2 Reserved
The default value of this bit is 0b.

bit 1 Mirror Display Enable
This bit controls whether the mirror display function is enabled for writes to the write buffers. When mirror display is enabled, the image data is "mirrored" in memory. For further information on the mirror display function, see Section 12.3.2, "Mirror" on page 107.
When this bit = 0b, the mirror display function is disabled.
When this bit = 1b, the mirror display function is enabled.

bit 0 Rotation Enable
This bit controls whether the rotation function is enabled for writes to the write buffers. When rotation is enabled, the image data is rotated by 180° (counter-clockwise) in memory. For further information on the rotation function, see Section 12.3.1, "180° Rotation" on page 106.
When this bit = 0b, the rotation function is disabled.
When this bit = 1b, the rotation function is enabled.

REG[54h] Transparency Key Color Red Register
Default = 00h Read/Write

Window Transparency Key Color Red bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Window Transparency Key Color Red bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit red component used to define the window transparency key color.

Bits 2-0 are not used for RGB5:6:5.

REG[56h] Transparency Key Color Green Register
Default = 00h Read/Write

Window Transparency Key Color Green bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Window Transparency Key Color Green bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit green component used to define the window transparency key color

Bits 1-0 are not used for RGB5:6:5.

REG[58h] Transparency Key Color Blue Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Window Transparency Key Color Blue bits 7-0							

bits 7-0 Window Transparency Key Color Blue bits [7:0]
These bits only have an effect when the transparency is enabled, REG[52h] bit 3 = 1b. These bits specify the 8-bit blue component used to define the window transparency key color

Bits 2-0 are not used for RGB5:6:5.

REG[5Ah] Write Window X Start Position Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window X Start Position bits 9-3							n/a

bits 7-1 Write Window X Start Position bits [9:3]
These bits determine the X start position of the write window in relation to the top left corner of the displayed image, in 8 pixel resolution (bytes). Even in a rotated orientation (see REG[52h] bit 0), the top left corner is still relative to the displayed image.

Write Window X Start Position = (REG[5Ah] bits 7-0) x 4 +1

Note
The value of this register is incremented by 8 pixels (1, 9, 17, 25, ..., horizontal size - 7)

REG[5Ch] Write Window Y Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Write Window Y Start Position bits 9-2							

REG[5Eh] Write Window Y Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Write Window Y Start Position bits 1-0	

REG[5Ch] bits 7-0
REG[5Eh] bits 1-0 Write Window Y Start Position bits [9:0]
These bits determine the Y start position of the window in relation to the top left corner of the displayed image, in pixels. Even in a rotated orientation (see REG[52] bit 0), the top left corner is still relative to the displayed image.

Write Window Y Start Position = (REG[5Ch] bits 7-0, REG[5Eh] bits 1-0) + 1

REG[60h] Write Window X End Position Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Write Window X End Position bits 9-3							n/a

bits 7-1 Write Window X End Position bits [9:3]
These bits determine the X end position of the window in relation to the top left corner of the displayed image, in 8 pixel resolution (bytes). Even in a rotated orientation (see REG[52h] bits 1-0), the top left corner is still relative to the displayed image.

Write Window X End Position = (REG[60h] bits 7-0) x 4 + 8

Note
The value of this register is incremented by 8 pixels (8, 16, 24, 32, ..., horizontal size)

REG[62h] Write Window Y End Position Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Write Window Y End Position bits 9-2							

REG[64h] Write Window Y End Position Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						Write Window Y End Position bits 1-0	

REG[62h] bits 7-0
REG[64h] bits 1-0 Write Window Y End Position bits [9:0]
These bits determine the Y end position of the window in relation to the top left corner of the displayed image, in pixels. Even in a rotated orientation (see REG[52h] bits 1-0), the top left corner is still relative to the displayed image.

Write Window Y End Position = (REG[62h] bits 7-0, REG[64h] bits 1-0) + 1

10.3.6 Memory Access Registers

REG[66h] Memory Data Port Register 0
Default = not applicable — Write Only

Memory Data Port bits 7-0 (WO)							
7	6	5	4	3	2	1	0

REG[67h] Memory Data Port Register 1
Default = not applicable — Write Only

Memory Data Port bits 15-8 (WO)							
7	6	5	4	3	2	1	0

REG[66h] bits 7-0 Memory Data Port bits [7:0] (Write Only)
These bits specify the lsb of the data word.

REG[67h] bits 7-0 Memory Data Port bits [15:8] (Write Only)
These bits specify the msb of the data word.

Note

1. If CNF0 = 1 (8-bit interface), REG[67h] is not used.
2. When the SDCLK is disabled (REG[68h] bit 0 = 0b), accesses to this register are invalid.
3. Burst data writes are supported through these registers. Register auto-increment is automatically disabled once reaching this address. All writes to this register will auto-increment the internal memory address only.

10.3.7 Miscellaneous Registers

REG[68h] Power Save Register
Default = 00h Read/Write

LCD Controller Reset	PWM Controller Reset	Memory Controller Reset	SDRAM Controller Reset	Alpha Blending Reset	Reserved		SDCLK Enable
7	6	5	4	3	2	1	0

bit 7 LCD Controller Reset
This bit controls the internal LCD controller block reset.
When this bit = 0b, the LCD controller block is operating normally.
When this bit = 1b, the LCD Controller block is reset.

bit 6 PWM Controller Reset
This bit controls the internal PWM controller block Reset.
When this bit = 0b, the PWM controller block is operating normally.
When this bit = 1b, the PWM controller block is reset.

bit 5 Memory Controller Reset
This bit controls the internal memory controller block reset.
When this bit = 0b, the memory controller block is operating normally.
When this bit = 1b, the memory controller block is reset.

bit 4 SDRAM Controller Reset
This bit controls the internal SDRAM controller block reset. After reset, the SDRAM must be initialized.
When this bit = 0b, the SDRAM controller block is operating normally.
When this bit = 1b, the SDRAM controller block is reset.

bit 3 Alpha Blending Controller Reset
This bit controls the internal alpha blending controller block reset.
When this bit = 0b, the alpha blending controller block is operating normally.
When this bit = 1b, the alpha blending controller block is reset.

bits 2-1 Reserved
The default value of these bits is 00b.

bit 0 SDCLK Enable
This bit controls the SDCLK.
When this bit = 0b, SDCLK is disabled and the S1D13517 is placed in power save mode.
When this bit = 1b, SDCLK is operating normally and the S1D13517 returns from power save mode.

Note
Disable SDCLK before changing PLL settings, SS settings, SYSCLK settings, or enabling PLL, enabling SS, or performing a software reset.

REG[6Ah] Non-Display Period Control / Status Register

Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Vertical Non-Display Period Status (RO)	Horizontal Non-Display Period Status (RO)	VDP OR'd with HDP Status (RO)	n/a			TE/INT Output Pin Function Select bits 1-0	

bit 7 Vertical Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a vertical non-display period (VNDP). VNDP is defined as the time between the last pixel on the last line of one frame to the first pixel on the first line of the next frame.
When this bit = 0b, the LCD panel output is in a Vertical Display Period.
When this bit = 1b, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Horizontal Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a horizontal non-display period (HNDP). HNDP is defined as the time between the last pixel in line n to the first pixel in line n+1.
When this bit = 0b, the LCD panel output is in a Horizontal Non-Display Period.
When this bit = 1b, the LCD panel output is in a Horizontal Display Period.

bit 5 VDP OR'd with HDP Status (Read Only)
This bit indicates whether the LCD panel is in a display period or a non-display period.
When this bit = 0b, the LCD panel is in a Display period.
When this bit = 1b, the LCD panel is in either a Horizontal or Vertical Non-Display period.

bits 1-0 TE/INT Output Pin Function Select bits[1:0]

Table 10-11: TE/INT Output Pin Function Selection

REG[6Ah] bits 1-0	TE/INT Output Function
00b	Horizontal Non-Display Period
01b	Vertical Non-Display Period
10b	HDP OR'd with VDP
11b	INT

10.3.8 General Purpose Output Pins Registers

Note
When 18-bit TFT is selected (REG[14h] bit 1 = 1b), GPO[9:4] are only available

REG[6Ch] General Purpose Output Register 0
Default = 00h Read/Write

n/a				Reserved		GPO9 Status	GPO8 Status
7	6	5	4	3	2	1	0

bits 3-2 Reserved
The default value of these bits is 00b.

bits 1-0 GPO[9:8] Status
Writing a 0b to this bit drives GPOx low.
Writing a 1b to this bit drives GPOx high.

REG[6Eh] General Purpose Output Register 1
Default = 00h Read/Write

GPO7 Status	GPO6 Status	GPO5 Status	GPO4 Status	GPO3 Status	GPO2 Status	GPO1 Status	GPO0 Status
7	6	5	4	3	2	1	0

bits 7-0 GPO[7:0] Status
Writing a 0b to this bit drives GPOx low.
Writing a 1b to this bit drives GPOx high.

10.3.9 PWM Registers

REG[70h] PWM Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWM Register Update (WO)	n/a				PWM Enable	PWM Output Select bits 1-0	

bit 7 PWM Register Update (Write Only)
When any PWM register (REG[72h] ~ REG[80h]) is changed, this bit must be written 1b to update the internal register values. Writing 0b to this bit has no effect.

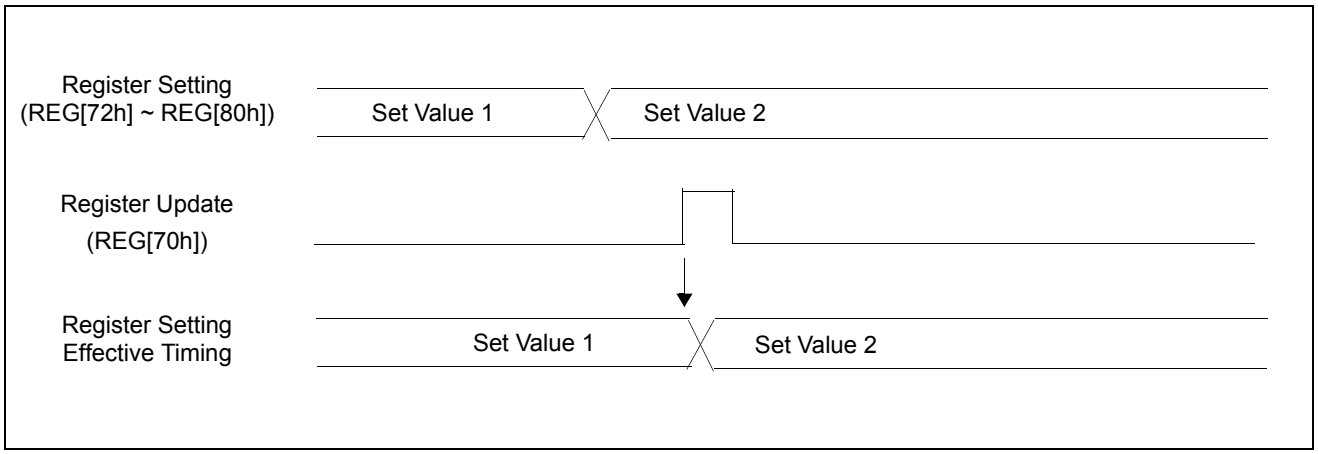


Figure 10-2: PWM Register Update Timing Sequence

bit 2 PWM Enable
This bit Pulse Width Modulation (PWM).
When this bit = 0b, PWM is disabled. When PWM is disabled, the PWM output is stopped at the current level and the may be High or Low. Use bits 1-0 of this register to set the desired output level before disabling PWM.
When this bit = 1b, PWM is enabled.

bits 1-0 PWM Output Select bits [1:0]

Table 10-12: PWM Output Select*ion*

REG[70h] bits 1-0	PWM Output Selected
00b	Low Output (Default)
01b	High Output
1xb	PWM Output

REG[72h] PWM High Duty Cycle Register 0
Default = 00h Read/Write

PWM High Duty Cycle bits 7-0							
7	6	5	4	3	2	1	0

REG[74h] PWM High Duty Cycle Register 1
Default = 00h Read/Write

PWM High Duty Cycle bits 15-8							
7	6	5	4	3	2	1	0

REG[76h] PWM High Duty Cycle Register 2
Default = 00h Read/Write

PWM High Duty Cycle bits 23-16							
7	6	5	4	3	2	1	0

REG[78h] PWM High Duty Cycle Register 3
Default = 00h Read/Write

PWM High Duty Cycle bits 31-24							
7	6	5	4	3	2	1	0

REG[72h] bits 7-0
REG[74h] bits 7-0
REG[76h] bits 7-0
REG[78h] bits 7-0 PWM High Duty Cycle bits [31:0]

These bits are the value for the PWM High duty cycle. The value entered into these registers is not loaded into internal registers until REG[70h] bit 7 has been written with a 1b.

REG[7Ah] PWM Low Duty Cycle Register 0
Default = 00h Read/Write

PWM Low Duty Cycle bits 7-0							
7	6	5	4	3	2	1	0

REG[7Ch] PWM Low Duty Register 1
Default = 00h Read/Write

PWM Low Duty Cycle bits 15-8							
7	6	5	4	3	2	1	0

REG[7Eh] PWM Low Duty Register 2
Default = 00h Read/Write

PWM Low Duty Cycle bits 23-16							
7	6	5	4	3	2	1	0

REG[80h] PWM Low Duty Register 3
Default = 00h Read/Write

PWM Low Duty Cycle bits 31-24							
7	6	5	4	3	2	1	0

REG[7Ah] bits 7-0
REG[7Ch] bits 7-0
REG[7Eh] bits 7-0
REG[80h] bits 7-0 PWM Low Duty Cycle bits [31:0]

These bits are the value for the PWM Low duty cycle. The value entered into these registers is not loaded into internal registers until REG[70h] bit 7 has been written with a 1b.

10.3.10 SDRAM Control Registers

REG[82h] SDRAM Control Register
Default = 02h — Read/Write

Reserved						SDRAM Memory Size Select bits 1-0	
7	6	5	4	3	2	1	0

bits 7-2 Reserved
The default value of these bits is 00_0000b

bits 1-0 SDRAM Memory Size Select bits [1:0]

Table 10-13: SDRAM Memory Size Selection

REG[82h] bits 1-0	SDRAM Memory Size Selected
0xb	16M Bits
10b	64M Bits (Default)
11b	128M Bits

REG[84h] SDRAM Status Register 0
Default = not applicable — Write Only

SDRAM Auto Refresh Enable (WO)	Reserved			SDRAM Self Refresh Enable (WO)	SDRAM Power Save Enable (WO)	SDRAM Initialization (WO)	Reserved
7	6	5	4	3	2	1	0

bit 7 SDRAM Auto Refresh Enable (Write Only)
This bit controls SDRAM Auto Refresh. This bit should be set at the same time as the SDRAM Initialization bit (bit 1 of this register).
When this bit is written 0b, SDRAM Auto Refresh is disabled.
When this bit is written 1b, SDRAM Auto Refresh is enabled.

bits 6-4 Reserved
The default value of these bits is 000b.

bit 3 Self Refresh Enable (Write Only)
This bit controls SDRAM Self Refresh
When this bit is written 0b, SDRAM Self Refresh is disabled.
When this bit is written 1b, SDRAM Self Refresh is enabled.

bit 2 SDRAM Power Save Enable (Write Only)
This bit controls SDRAM Power Save
When this bit is written 0b, SDRAM Power Save is disabled.
When this bit is written 1b, SDRAM Power Save is enabled.

bit 1 SDRAM Initialization (Write Only)
After power-on or reset, this bit is used to initialize the SDRAM.
When this bit is written 0b, the status bit is reset.
When this bit is written 1b, the SDRAM is initialized. This bit may only be written once after power-on/reset.

bit 0 Reserved
The default value of this bit is 0b.

REG[86h] SDRAM Status Register 1
Default = 00h Read Only

7	6	5	4	3	2	1	0
SDRAM Auto Refresh Status (RO)	Reserved			SDRAM Self Refresh Status (RO)	SDRAM Power Save Status (RO)	SDRAM Initialization Status (RO)	Reserved

bit 7 SDRAM Auto Refresh Status (RO)
This bit reflects the status of REG[84h] bit 7, SDRAM Auto Refresh Enable.
When this bit = 0b, SDRAM Auto Refresh is disabled.
When this bit = 1b, SDRAM Auto Refresh is enabled.

bits 6-4 Reserved
The default value of these bits is 000b.

bit 3 SDRAM Self Refresh Status (RO)
This bit reflects the status of REG[84h] bit 3, SDRAM Self Refresh Enable.
When this bit = 0b, SDRAM Self Refresh is disabled.
When this bit = 1b, SDRAM Self Refresh is enabled.

bit 2 SDRAM Power Save Status (RO)
This bit reflects the status of REG[84h] bit 2, SDRAM Power Save Enable.
When this bit = 0b, SDRAM Power Save is disabled.
When this bit = 1b, SDRAM Power Save is enabled.

bit 1 SDRAM Initialization Status (RO)
This bit reflects the status of the SDRAM Initialization sequence (REG[84h] bit 1 = 1b).
When this bit = 0b, the SDRAM Initialization is in progress.
When this bit = 1b, the SDRAM Initialization has finished.

bit 0 Reserved
The default value of this bit is 0b.

REG[88h] SDRAM MRS Value Register 0
Default = 22h — Read/Write

SDRAM MRS Value bits 7-0							
7	6	5	4	3	2	1	0

REG[8Ah] SDRAM MRS Value Register 1
Default = 00h — Read/Write

n/a				SDRAM MRS Value bits 11-8			
7	6	5	4	3	2	1	0

REG[8Ah] bits 3-0
REG[88h] bits 7-0 SDRAM MRS Value bits [11:0]
These bits are the MRS setting values for the SDRAM.
These bits must not be changed from the default value of 022h.

REG[8Ch] SDRAM Refresh Counter Register 0
Default = FFh — Read/Write

SDRAM Refresh Counter bits 7-0							
7	6	5	4	3	2	1	0

REG[8Eh] SDRAM Refresh Counter Register 1
Default = 03h — Read/Write

n/a				SDRAM Refresh Counter bits 11-8			
7	6	5	4	3	2	1	0

REG[8Eh] bits 3-0
REG[8Ch] bits 7-0 SDRAM Refresh Counter bits [11:0]
These bits are used to set the value of the refresh counter. The refresh counter issues the auto refresh command at the interval set by these registers. SDCLK is the input clock of the counter. The value of these registers must satisfy the following expression.

Refresh Counter = $(1/f_{SDCLK})$ x (value of these registers in decimal)
The resulting value must be less than the SDRAM refresh time.

For example, using the default value of 03FFh (1023), when SDRAM of 4096 refresh cycles /64ms is used with a 90MHz SDCLK,
set-up time of the counter = (1/90MHz) x 1023 = 11.36us
SDRAM refresh time = 64ms/4096 = 15.63us.
11.36us < 15.63us, so the value of 03FFh is good.

Using the same memory as above, but with a 66MHz SDCLK,
(1/66MHz) x 1023 = 15.50us
SDRAM refresh time = 64ms/4096 = 15.63us
15.50us < 15.63us, so the value of 03FFh is good.

REG[90h] SDRAM Write Buffer Memory Size Register 0
Default = 00h — Read/Write

SDRAM Write Buffer Memory Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 SDRAM Write Buffer Memory Size bits [7:0]
These bits determine the buffer memory size of each 16-buffers at the 16K byte units. Buffer 1 becomes the start address 0h fixing of SDRAM, the start address of buffer 2 is appointed at these bits. The buffer 3-16 is set at similar offset value. In case of initial value 00h, the start address of all buffers becomes the start addresses 0h of SDRAM.

The start address of buffer 2: A [23: 22] = 0
The start address of buffer 2: A [21: 14] = (REG [90h] bits 7-0)
The start address of buffer 2: A [13: 0] = 0

Table 10-14: SDRAM Write Buffer Memory Size Selection

LCD Panel Size	Buffer Size	REG[90h] Value
HVGA	512K byte	20h
VGA	1M byte	40h
WVGA	1.25M byte	50h
SVGA	1.5M byte	60h
QHD	1.75M byte	70h

REG[92h] SDRAM Debug Register
Default = 00h — Read Only

SDRAM Controller Debug Status (RO)							
7	6	5	4	3	2	1	0

bit 4 Memory Controller Read Buffer Empty (Read Only)
When this bit = 0b, the Read Buffer is not empty.
When this bit = 1b, the Read Buffer is empty.
This bit is cleared by resetting the Memory Controller.

bit 3 Memory Controller Write Buffer Overflow (Read Only)
When this bit = 0b, the Write Buffer is not full.
When this bit = 1b, the Write Buffer is full.
This bit is cleared by resetting the Memory Controller.

bits 2-0 SDRAM Controller Status (Read Only)
These three bits indicate the status of the SDRAM controller state machine as shown in the following table.

Table 10-15: SDRAM Controller Status

REG[92h] bits 2-0	Status
000b	Reset
001b	Initial
010b	Idle
011b	Read/Write
100b	Auto Refreshing
101b	MRS&PALL
110b	Self Refresh
111b	Power Save

10.3.11 Alpha-Blend Registers

REG[94h] Alpha-Blend Control Register
Default = not applicable — Write Only

7	6	5	4	3	2	1	0
n/a							Alpha-Blend Start (WO)

bit 0 Alpha-Blend Start (Write Only)
When this bit is written 0b, there is no effect.
When this bit is written 1b then 0b, Alpha-Blend is started.

REG[96h] is Reserved

This register is Reserved and should not be written.

REG[98h] Alpha-Blend Horizontal Size Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a	Alpha-Blend Horizontal Image Size bits 6-0						

bits 6-0 Alpha-Blend Horizontal Image Size bits [6:0]
These bits set the Alpha-Blend Horizontal Image Size in 8 pixel resolution (bytes).

Alpha-Blend Horizontal Image Size = ((REG[98h] bits 6-0) + 1) x 8

REG[9Ah] Alpha-Blend Vertical Size Register 0
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Vertical Image Size bits 7-0							

REG[9Ch] Alpha-Blend Vertical Size Register 1
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a						Alpha-Blend Vertical Image Size bits 9-8	

REG[9Ch] bits 1-0
REG[9Ah] bits 7-0 Alpha-Blend Vertical Image Size bits [9:0]
These bits set the Alpha-Blend Horizontal Image Size.

Alpha-Blend Vertical Image Size = (REG[9Ch] bits 1-0, REG[9Ah] bits 7-0) + 1

REG[9Eh] Alpha-Blend Value Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
Alpha-Blend Input Image Select bits 1-0		Alpha-Blend Value Select bits 5-0					

bits 7-6 Alpha-Blend Input Image Select bits [1:0]
These bits select the Alpha-Blend Input Image.

Table 10-16: Alpha-Blend Input Image Selection

REG[9Eh] bits 7-6	Alpha-Blend Input Image
0xb	Disabled (Default)
10b	Input Image 1 + Input Image 2
11b	Input Image 1

bits 5-0 Alpha-Blend Value Select bits [5:0]
These bits set the value of Alpha-Blend. When the Alpha-Blend input image setting is input image 1, the value of input image 2 becomes invalid.

Output image = (input image 1 x alpha setting value) * (input image 2 + x (one-alpha setting value)

Table 10-17: Alpha-Blend Value Selection

REG[9Eh] bits 5-0	Alpha Value
00h	0
01h	1/32
02h	2/32
03h	3/32
• • •	• • •
1Fh	31/32
2xh	1

REG[A0h] Alpha-Blend Input Image 1 Start Address Register 0
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 7-3					n/a		
7	6	5	4	3	2	1	0

REG[A2h] Alpha-Blend Input Image 1 Start Address Register 1
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 15-8							
7	6	5	4	3	2	1	0

REG[A4h] Alpha-Blend Input Image 1 Start Address Register 2
Default = 00h Read/Write

Alpha-Blend Input Image 1 Start Address bits 23-16							
7	6	5	4	3	2	1	0

REG[A4h] bits 7-0
REG[A2h] bits 7-0
REG[A0h] bits 7-3 Alpha-Blend Input Image 1 Start Address bits 7-[23:3]
These bits specify the memory start address of Alpha-Blend Input Image 1 in byte addresses.

Alpha-Blend Input Image 1 Start Address [23:3] = (REG[A4h] bits 7-0), (REG[A2h] bits 7-0), (REG[A0h] bits 7-3)

REG[A6h] Alpha-Blend Input Image 2 Start Address Register 0
Default = 00h Read/Write

Alpha-Blend Input Image 2 Start Address bits 7-3					n/a		
7	6	5	4	3	2	1	0

REG[A8h] Alpha-Blend Input Image 2 Start Address Register 1
Default = 00h Read/Write

Alpha-Blend Input Image 2 Start Address bits 15-8							
7	6	5	4	3	2	1	0

REG[AAh] Alpha-Blend Input Image 2 Start Address Register 2
Default = 00h Read/Write

Alpha-Blend Input Image 2 Start Address bits 23-16							
7	6	5	4	3	2	1	0

REG[AAh] bits 7-0
REG[A8h] bits 7-0
REG[A6h] bits 7-3 Alpha-Blend Input Image 2 Start Address bits[23:3]
These bits specify the memory start address of Alpha-Blend Input Image 2 in byte addresses.

Alpha-Blend Input Image 2 Start Address [23:3] = (REG[AAh] bits 7-0), (REG[A8h] bits 7-0), (REG[A6h] bits 7-3)

REG[ACh] Alpha-Blend Output Image Start Address Register 0
Default = 00h Read/Write

Alpha-Blend Output Image Start Address bits 7-3					n/a		
7	6	5	4	3	2	1	0

REG[AEh] Alpha-Blend Output Image Start Address Register 1
Default = 00h Read/Write

Alpha-Blend Output Image Start Address bits 15-8							
7	6	5	4	3	2	1	0

REG[B0h] Alpha-Blend Output Image Start Address Register 2
Default = 00h Read/Write

Alpha-Blend Output Image Start Address bits 23-16							
7	6	5	4	3	2	1	0

REG[B0h] bits 7-0
REG[AEh] bits 7-0
REG[ACh] bits 7-3 Alpha-Blend Output Image Start Address bits [23:3]
These bits specify the memory start address of Alpha-Blend Output Image in byte addresses.

Alpha-Blend Input Image 2 Start Address[23:3] = (REG[B0h] bits 7-0), (REG[AEh] bits 7-0), (REG[ACh] bits 7-3)

10.3.12 Interrupt Registers

The following Figure shows the block diagram of the Alpha-Blend interrupt circuit.

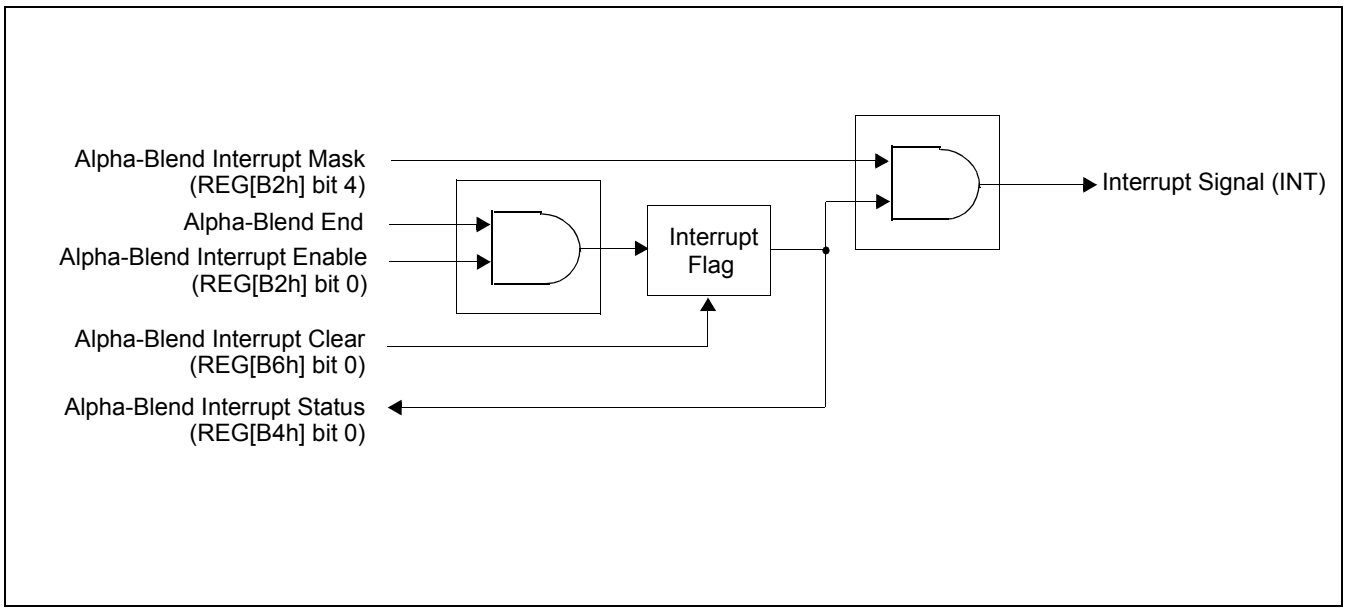


Figure 10-3: Alpha-Blend Interrupt Circuit Block Diagram

REG[B2h] Interrupt Control Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a	Reserved		Alpha-Blend Interrupt Mask Disable	n/a	Reserved		Alpha-Blend Interrupt Enable

bits 6-5 Reserved
The default value of these bits is 00b

bit 4 Alpha-Blend Interrupt Mask Disable
This bit disables the Alpha-Blend Interrupt Mask.
When this bit = 0b, the interrupt mask is enabled.
When this bit = 1b, the interrupt mask is disabled.

bits 2-1 Reserved
The default value of these bits is 00b

bit 0 Alpha-Blend Interrupt Enable
This bit enables the Alpha-Blend Interrupt.
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

REG[B4h] Interrupt Status Register
Default = 00h — Read Only

7	6	5	4	3	2	1	0
n/a					Reserved		Alpha-Blend Interrupt Status (RO)

bits 2-1 Reserved
The default value of these bits is 00b.

bit 0 Alpha-Blend Interrupt Status (Read Only)
This bit indicates the status of the Alpha-Blend interrupt.
When this bit = 0b, an interrupt has not been generated.
When this bit = 1b, an interrupt has been generated.

REG[B6h] Interrupt Clear Register
Default = not applicable — Write Only

7	6	5	4	3	2	1	0
n/a					Reserved		Alpha-Blend Interrupt Clear (WO)

bits 2-1 Reserved
The default value of these bits is 00b.

bit 0 Alpha-Blend Interrupt Clear (Write Only)
This bit clears the interrupt status bit.
When this bit is written 0b, there is no effect.
When this bit is written 1b then 0b, the Alpha-Blend interrupt status bit (REG[B4h] bit 0) is cleared.

Chapter 11 Host Interface

11.1 Indirect Interface

Accessing the S1D13517 through the asynchronous host interface is a multiple step process. All Registers and Memory are accessed through the register space.

Note
All Register accesses are 8-bit only, except for the Memory Data Port. If the Host interface is 16-bits wide (CNF0 = 0b), the lsbs (HD[7:0]) are used for all registers except the Memory Data Port.
For the Memory Data Port (REG[66h, 67h]), both registers are used when the host interface is 16-bits wide (CNF0 = 0b) and only REG[66h] is used when it is 8-bits wide (CNF0 = 1b).

First, perform a single "Address Write" to setup the register address. Next, perform a "Data Read/Write" to specify the data to be stored or read from the registers or memory specified in the "Address Write" cycle. Subsequent data read/writes without an Address Write to change the register address, will automatically "auto" increment the register address, or the internal memory address if accessing the Memory Data Port (REG[66h], REG[67h]).

To write display data to a Window Aperture, specify the Window coordinates followed by burst data writes to the Memory Data Port to fill the window. In this sequence, the internal memory addressing is automatic (see examples). The Memory Data Port is located directly following the Window coordinates to minimize the number of Address Writes.

Note
Memory read function is not supported

11.1.1 Register Write Procedure

1. Perform an address write to setup register address bits 7-0.
2. Perform a data write to update the register.
3. Additional data writes can be performed as the register addresses will be auto-incremented.

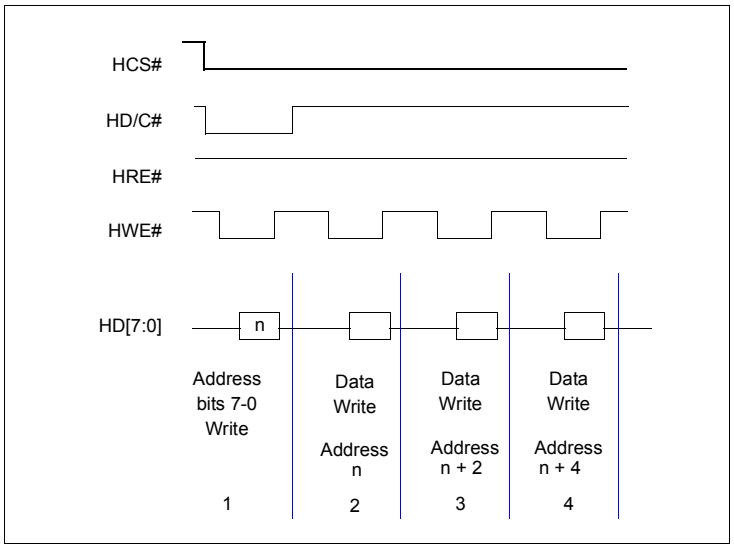


Figure 11-1: Register Write Example Procedure

11.1.2 Register Read Procedure

1. Perform an address write to setup register address bits 7-0.
2. Perform a data read to get the register value.
3. Additional data reads can be performed as the register addresses will be auto-incremented.

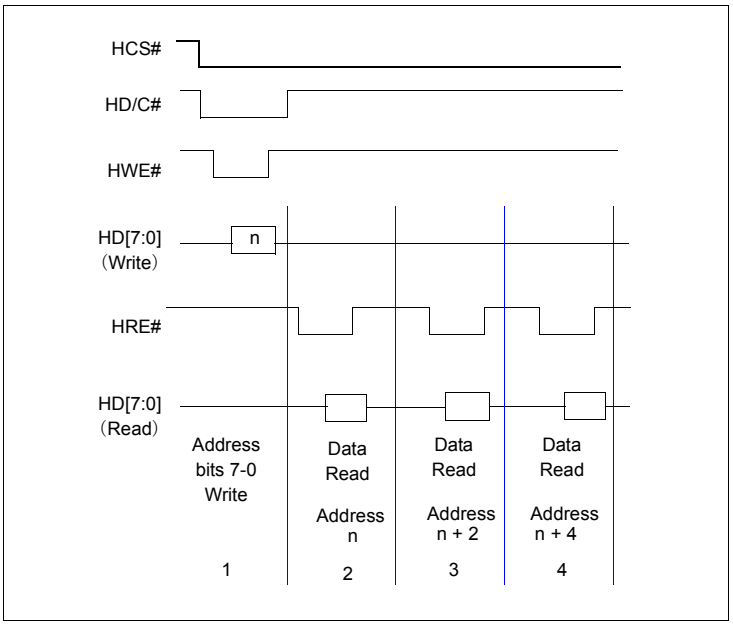


Figure 11-2: Register Read Example Procedure

11.1.3 Memory Write (New Window) Procedure

The S1D13517 has a special procedure to minimize setup accesses when bursting window data.

1. Set the panel dimension registers before writing any window data.
2. Perform an address write to point to the first window register (Window X Start Position Register 0, REG[5Ah]).
3. Perform "data" writes to the next six, 8-bit registers (REG[5Ah] ~ REG[64h]). This will setup all the window coordinates.

Note
The register addresses will be auto-incremented after each data write and will point at Memory Data Port Register 0 (REG[66h]) when done.

4. Perform burst data writes to fill the window (the register address will already be pointing at the Memory Data Port).

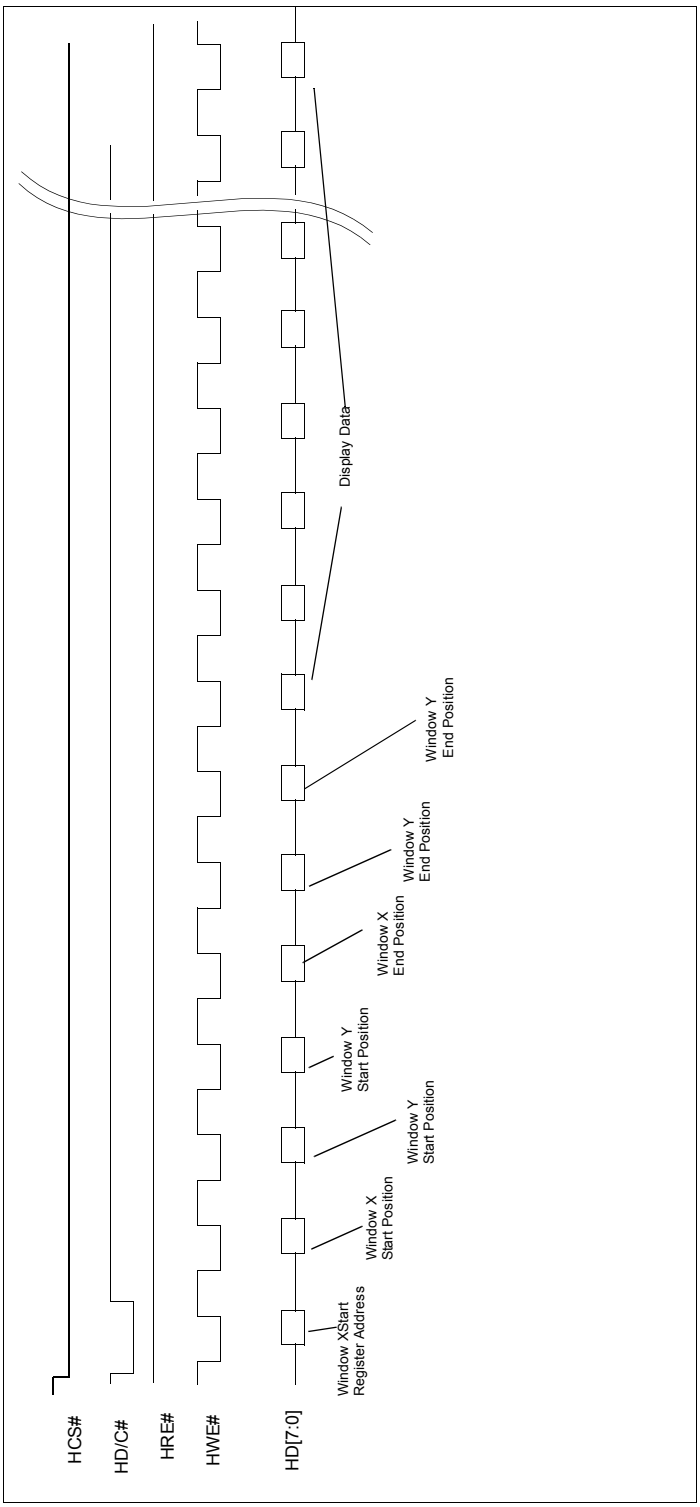


Figure 11-3: Sequential Memory Write Example

11.1.4 Memory Write (Update Window) Using Existing Window Coordinates

1. Perform an address write to point to Memory Data Port Register 0 (REG[66h]).
2. Perform burst data writes to fill the window.

Note
In this case, the previous coordinates of the Window Aperture are used. Each write to the Memory Data Port will auto-increment the internal memory address only.

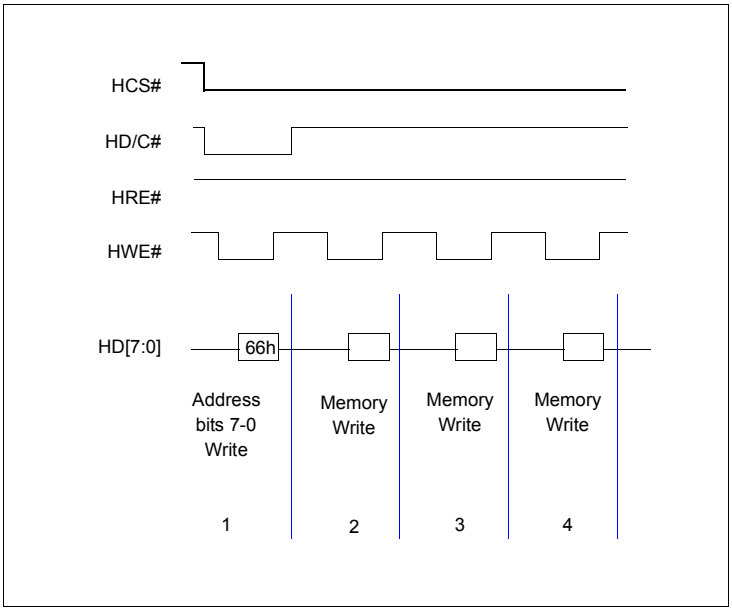


Figure 11-4: Burst Memory Write

11.2 Color Formats

11.2.1 8-bit 16bpp mode (RGB 5:6:5)

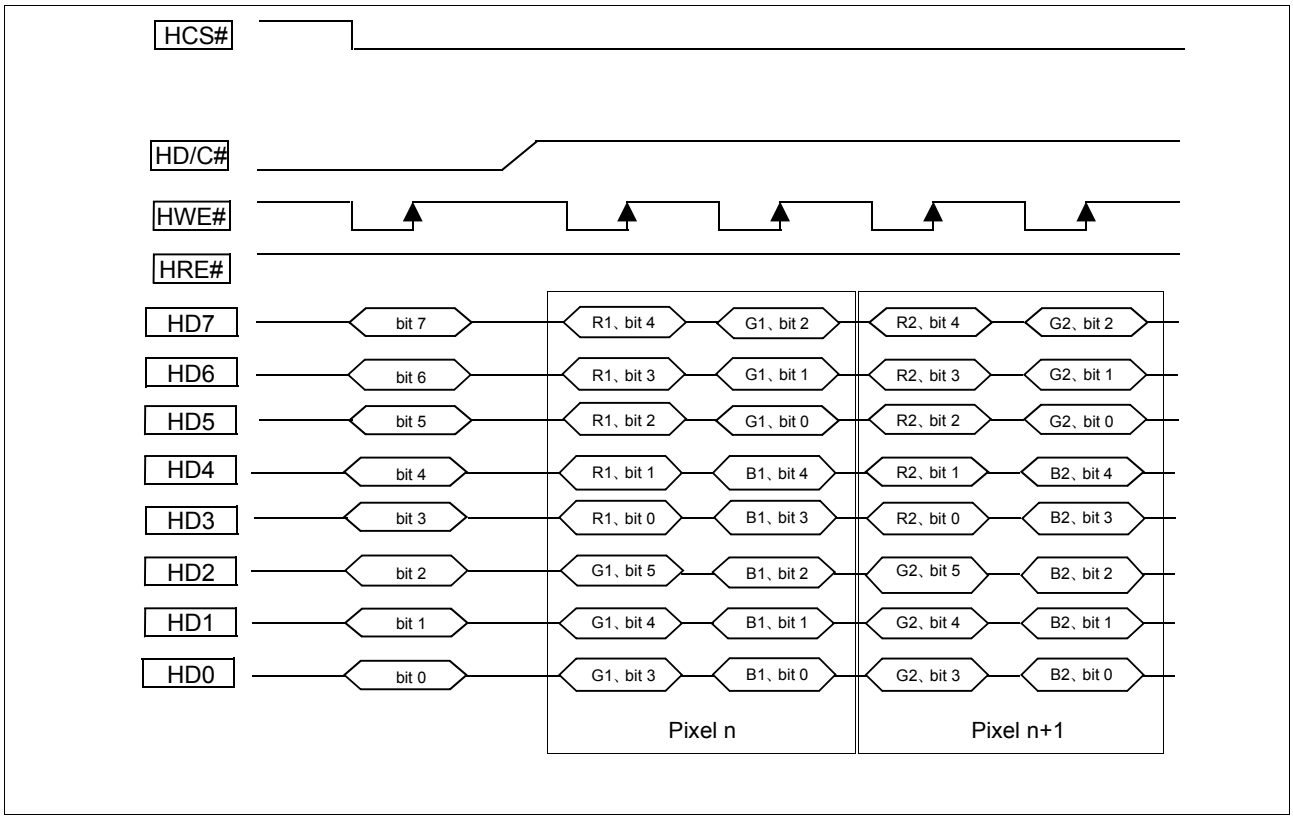


Figure 11-5: 8-bit 16bpp mode (RGB 5:6:5)

11.2.2 8-bit 24bpp mode (RGB 8:8:8)

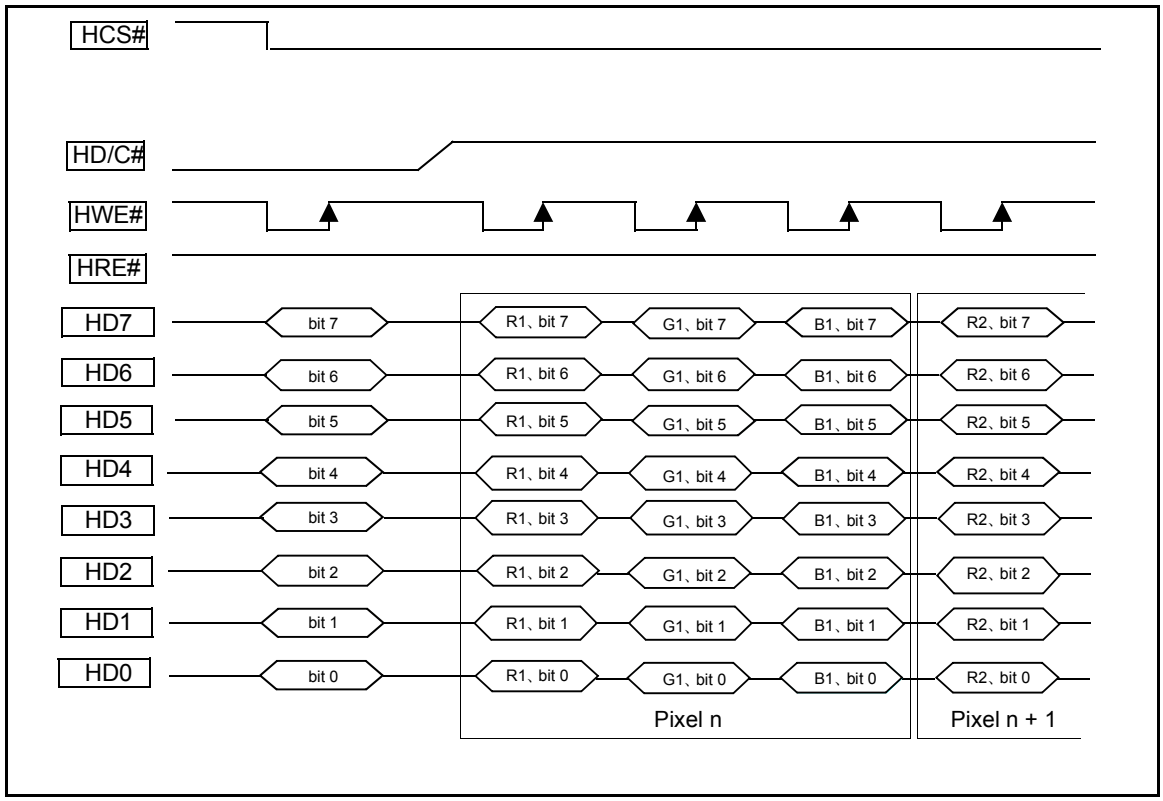


Figure 11-6: 8-bit 24bpp mode (RGB 8:8:8)

11.2.3 16-bit 16bpp mode (RGB 5:6:5)

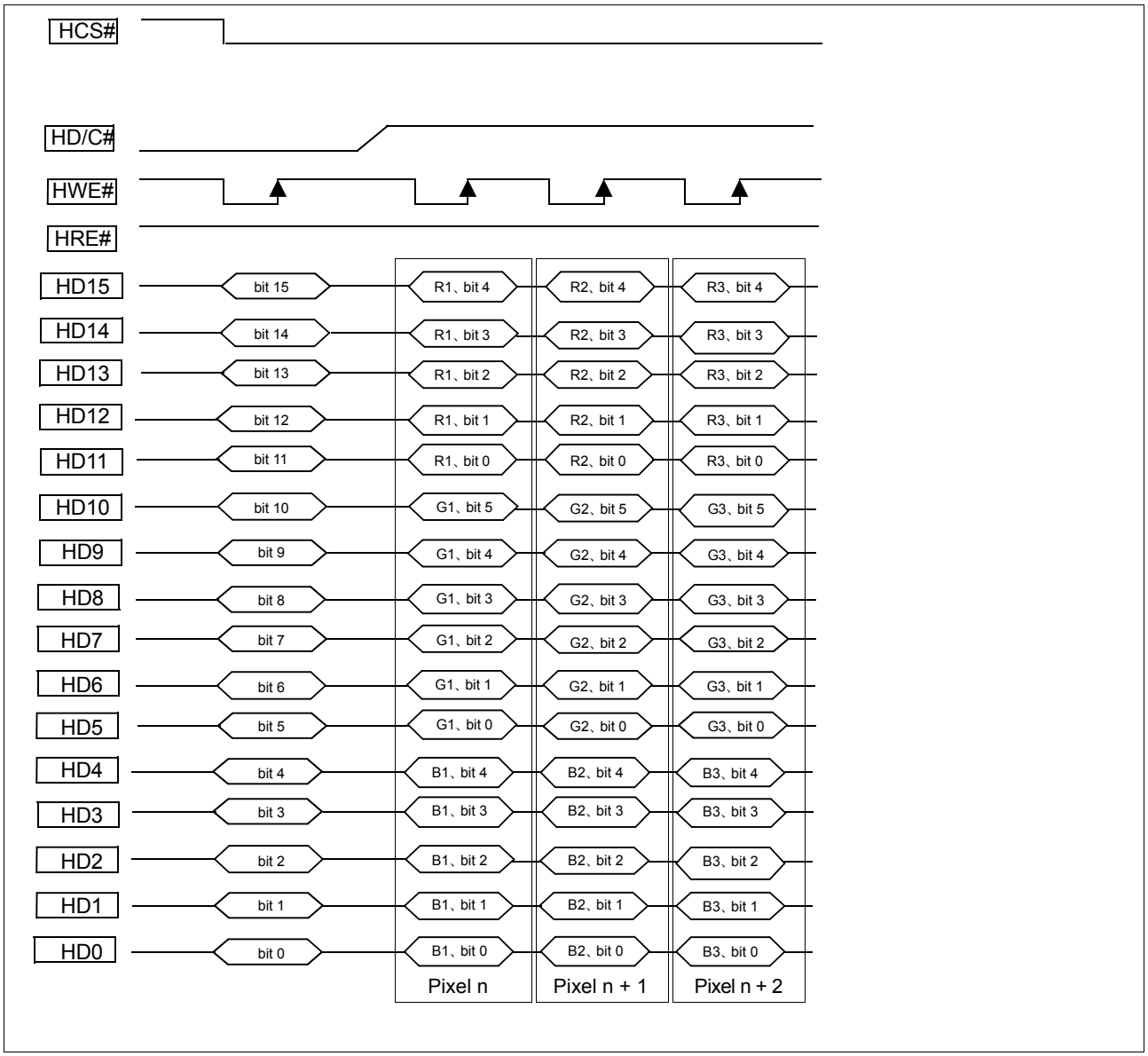


Figure 11-7: 16-bit 16bpp mode (RGB 5:6:5)

11.2.4 16-bit 24bpp mode 1 (RGB 8:8:8)

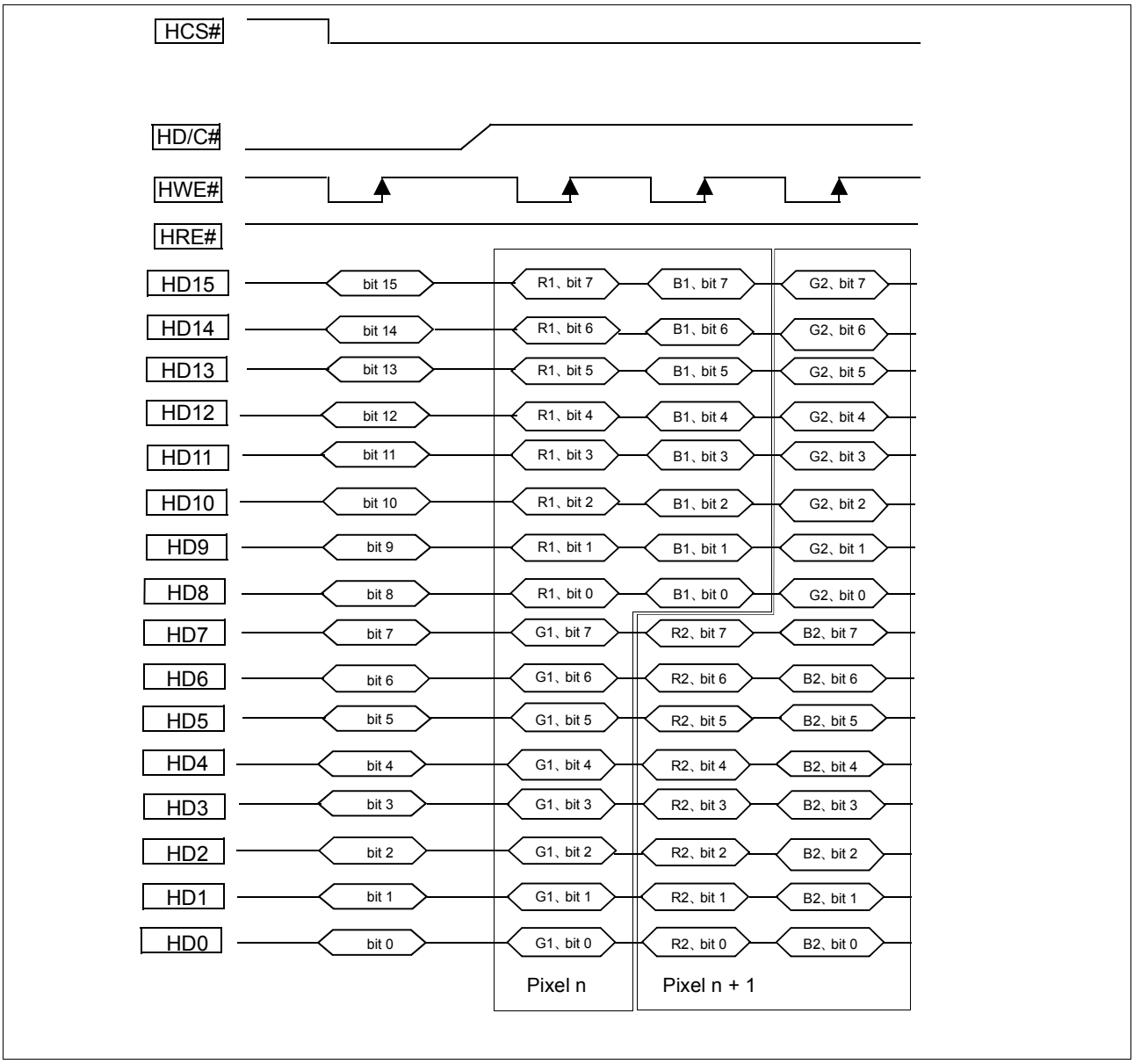


Figure 11-8: 16-bit 24bpp mode 1 (RGB 8:8:8)

11.2.5 16-bit 24bpp mode 2 (RGB 8:8:8)

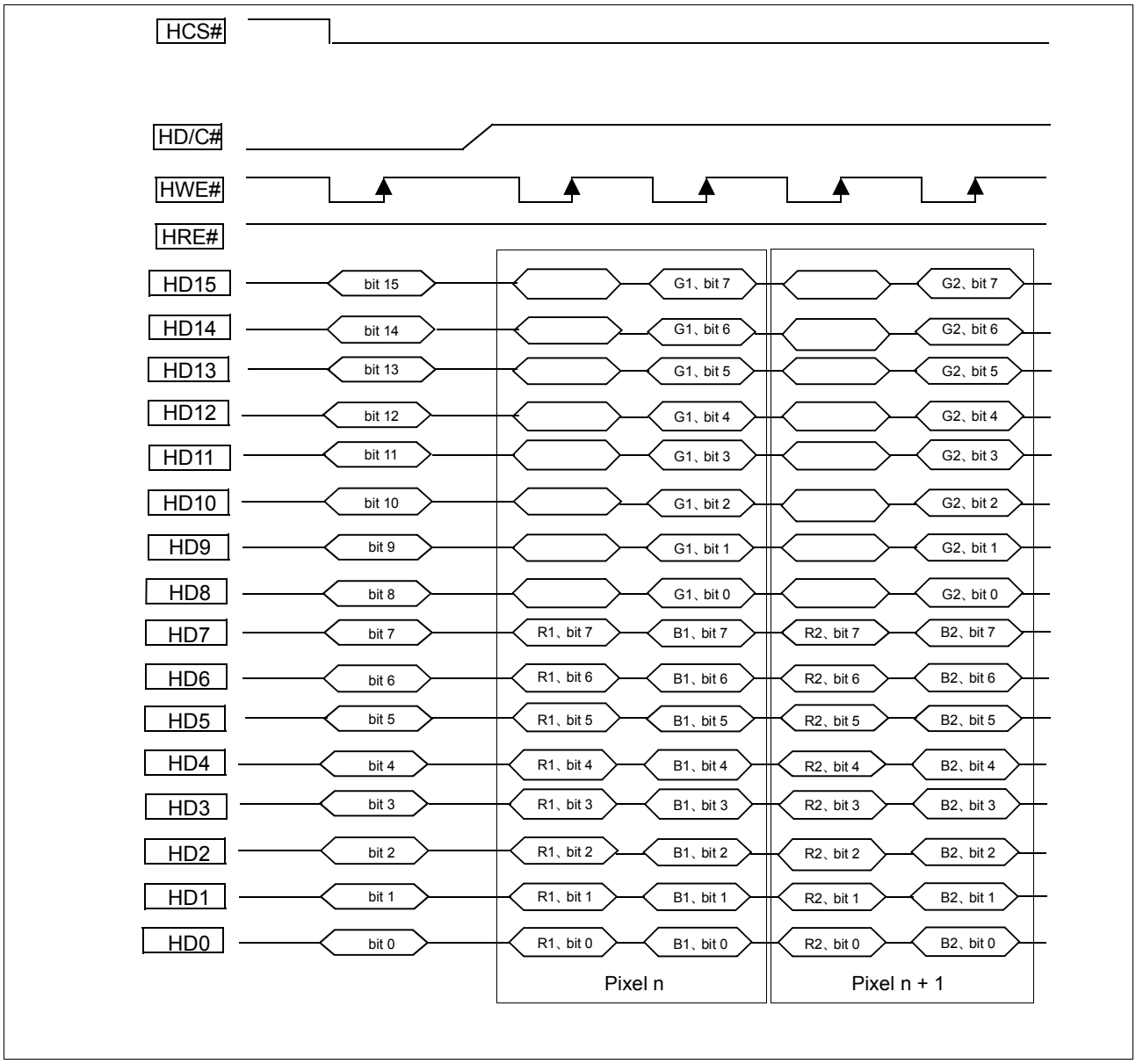


Figure 11-9: 16-bit 24bpp mode 2 (RGB 8:8:8)

11.3 PCLK vs. Input Data Rate

The input image data rate from the host interface is shown.

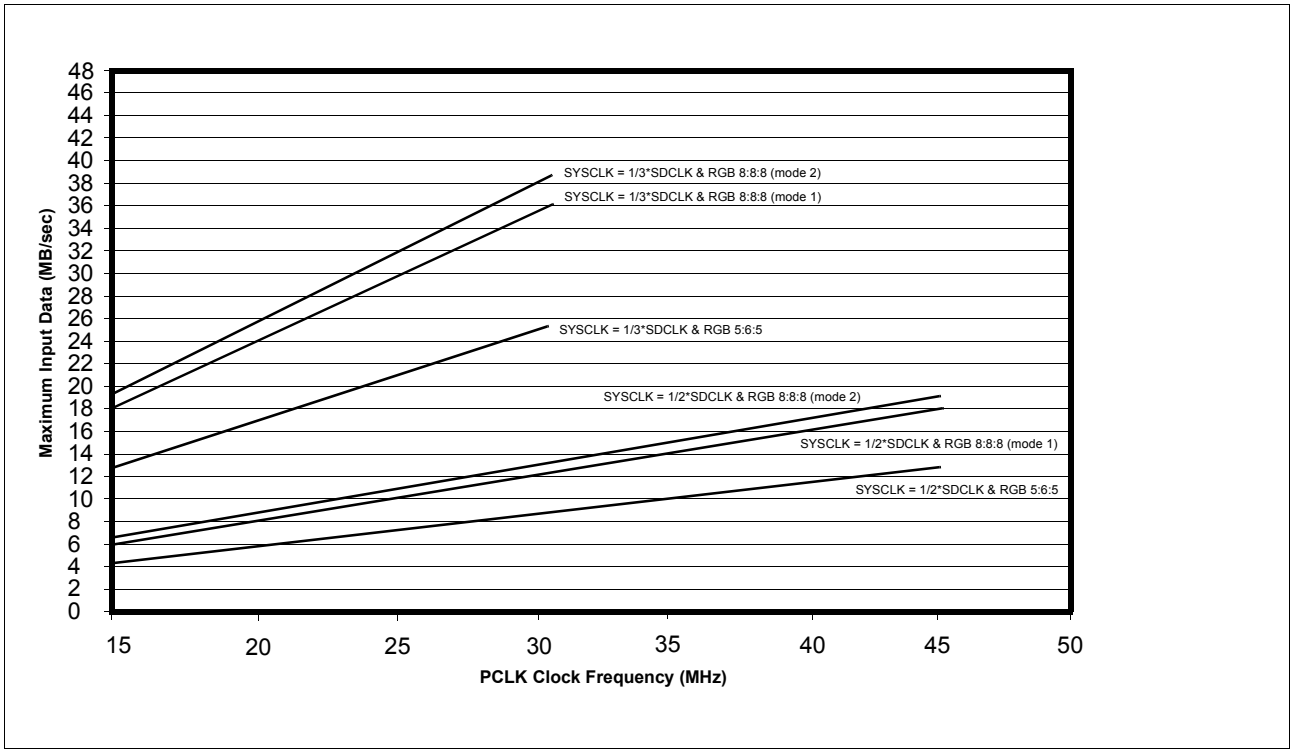


Figure 11-10: PCLK vs. Input Data Rate

Chapter 12 Display Functions

12.1 Display Window

The S1D13517 display window is defined by the size of the LCD display (see REG[16h] and REG[1Ah] ~ REG[1Ch]). All updates to the display window are done through a write window which allows rectangular writes to the selected write buffer (see REG[52h] bits 7-4). The write window is configured based on X/Y Start/End positions (REG[5Ah] ~ REG[64h]) relative to the origin of the display window. Once the write window is configured, all image data is written to the display buffer using the Memory Data Port registers, REG[66h] ~ REG[67h].

The write window X/Y Start/End positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). All window coordinates are referenced to top left corner of the display window (even when rotation or mirror are enabled no host side translation is required).

The display window source can be selected from any of the available write buffers (REG[2Ah] bits 7-4). All display updates can have independent mirror, rotation, and transparency settings.

12.1.1 Display Buffer Configuration

The Display Buffer is divided into a maximum of 16 write buffer areas. The number of write buffers is limited by the memory size and the write buffer memory size specified in REG[90h]. The write buffers can be used to store image data for the display window, PIP window, or Alpha-Blend image data.

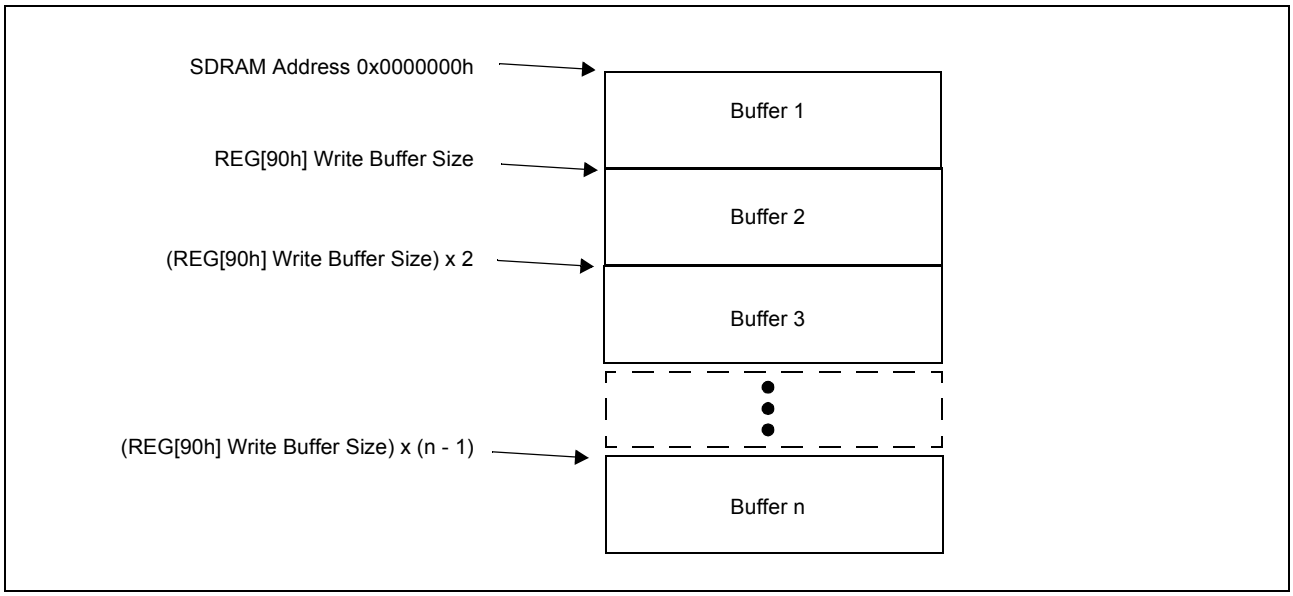


Figure 12-1: Display Buffer Configuration

12.1.2 Write Window Settings

Image data is stored in the display buffer using the write window. The write window can be configured for either a "full screen" or "partial" update according to the setting of the Write Window X/Y Start/End position registers. All position parameters are relative to the origin of the display. Horizontal position (X) must be set in eight pixel resolution. Vertical position (Y) is set in one line resolution.

The destination write buffer and other write options, such as Transparency, Mirror, and Rotation, can be selected using REG[52h]. All writes to a write buffer are "destructive" writes.

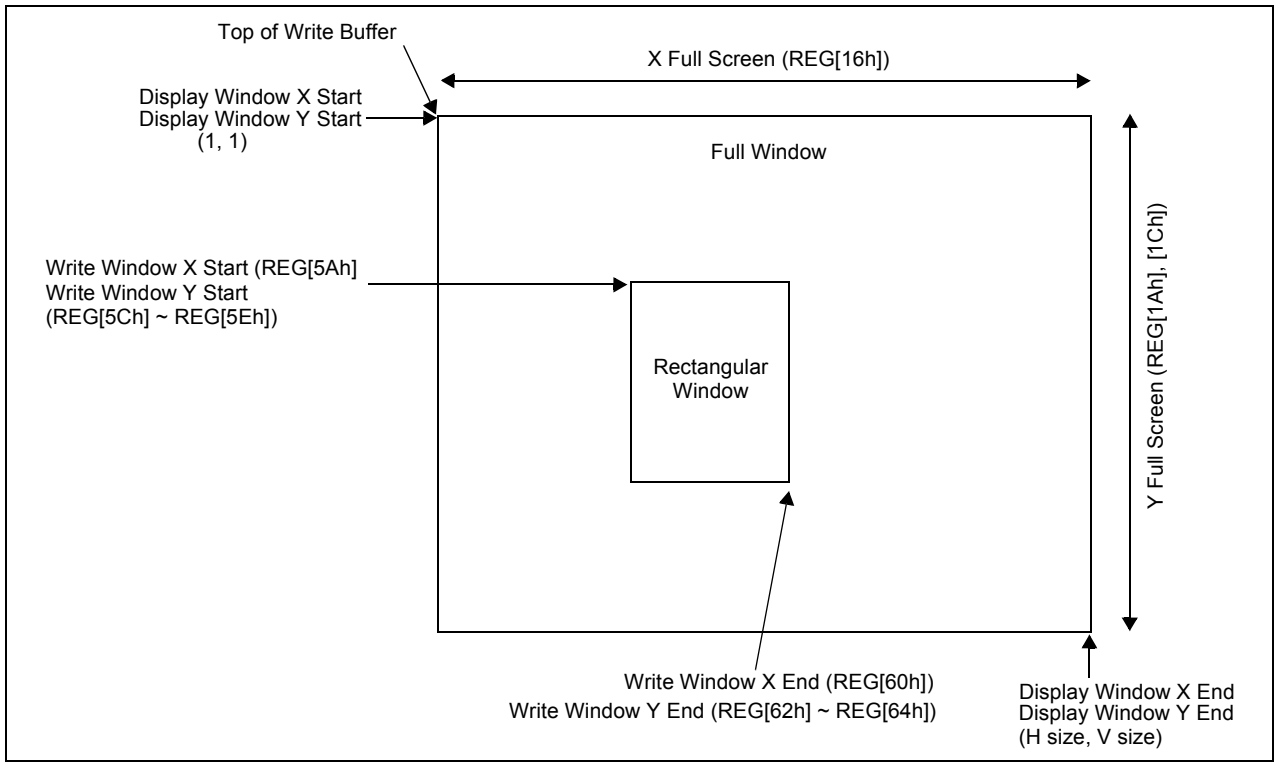


Figure 12-2: Write Window Settings

The following example shows a rectangular write window being written to a write buffer with a previously input "full screen" image.

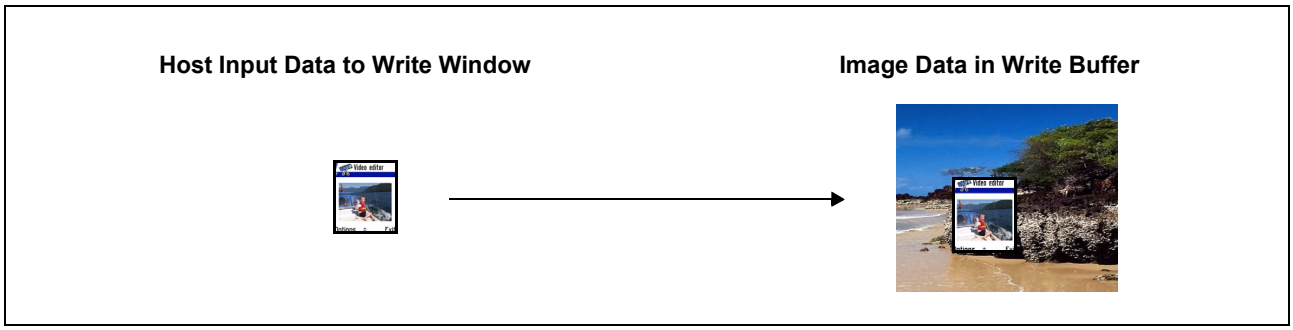


Figure 12-3: Display Window Example

12.2 Transparency

When image data is written to a write buffer, a transparency key color can be specified using REG[54h] ~ REG[58h]. When the Transparency function is enabled (REG[52h] bit 3 = 1b), pixels of the specified key color are not written to the write buffer. This function can be used to overwrite text and icons in display data.

The following example shows an example where the transparency function is enabled for the Write Window. In this case the key color is black so the black pixels are not written to the write buffer.

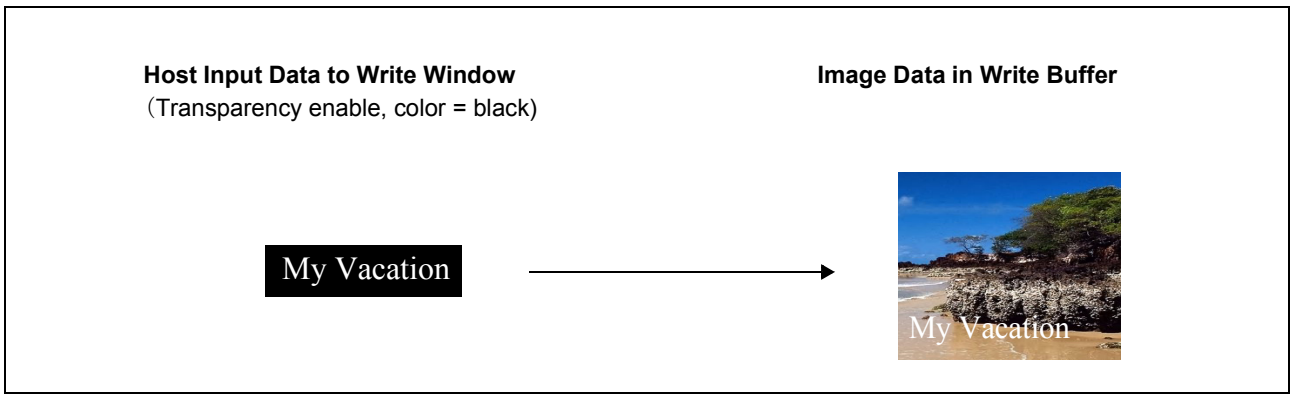


Figure 12-4: Transparency Example

12.3 Rotation and Mirror

Most computer displays are refreshed in landscape orientation - from left to right and top to bottom. Computer images are stored in the same manner.

Rotation is designed to rotate the displayed image by 180° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user. It is accomplished by rotating the image data during display writes (see REG[52h] bit 0). By processing the rotation in hardware, there is a performance advantage over software rotation of the displayed image.

Mirror is designed “mirror” the displayed image from right to left. Mirror is done in the hardware and is transparent to the user. The mirror function is done during display writes (see REG[52h] bit 1). Mirroring the image in hardware, also offers a performance advantage over software mirroring of the same image.

12.3.1 180° Rotation

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when 180° rotation is enabled (REG[52h] bit 0 = 1b). The application image is written to the S1D13517 as A-B-C-D. However, it is stored in the write buffer as D-C-B-A and the LCD display is refreshed as D-C-B-A.

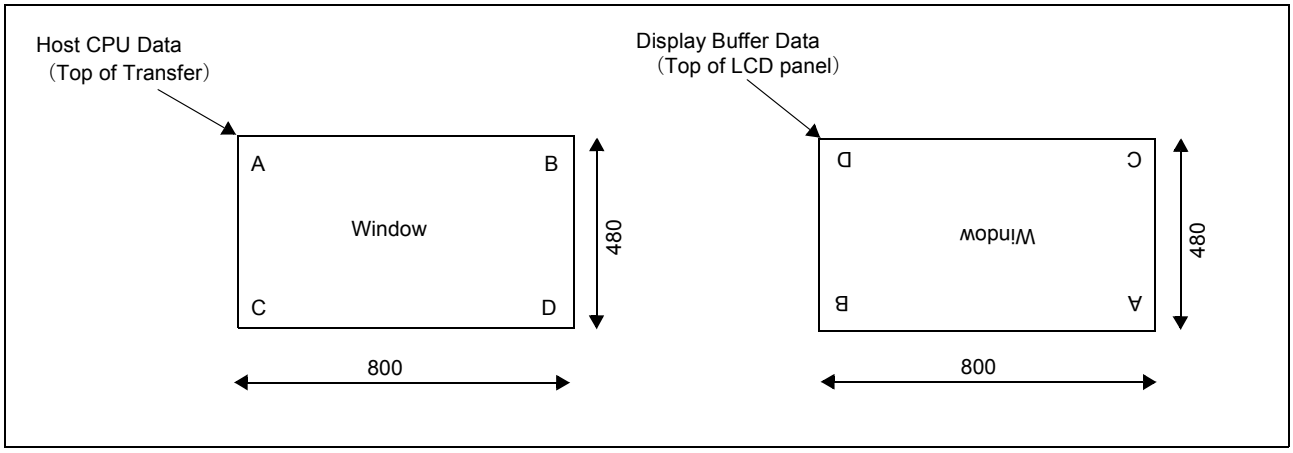


Figure 12-5: 180° Rotation Example

12.3.2 Mirror

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when Mirror is enabled (REG[52h] bit 1 = 1b). The application image is written to the S1D13517 as A-B-C-D. However, it is stored in the write buffer as B-A-D-C and the LCD display is refreshed as B-A-D-C.

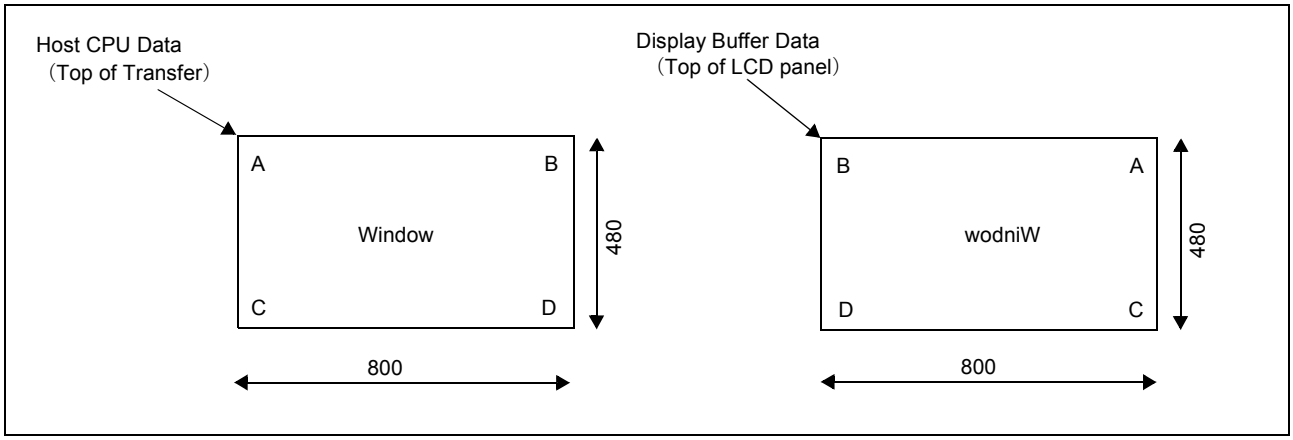


Figure 12-6: Mirror Example

12.3.3 180° Rotation and Mirror

The following figure shows the relationship between the image sent by the Host and the image as displayed on the LCD panel when both Mirror and Rotation are enabled (REG[52h] bits 1-0 = 11b). In this case, the image is rotated by the rotation function after the mirror function takes place. The application image is written to the S1D13517 as A-B-C-D. However, it is stored in the write buffer as C-D-A-B and the LCD display is refreshed as C-D-A-B.

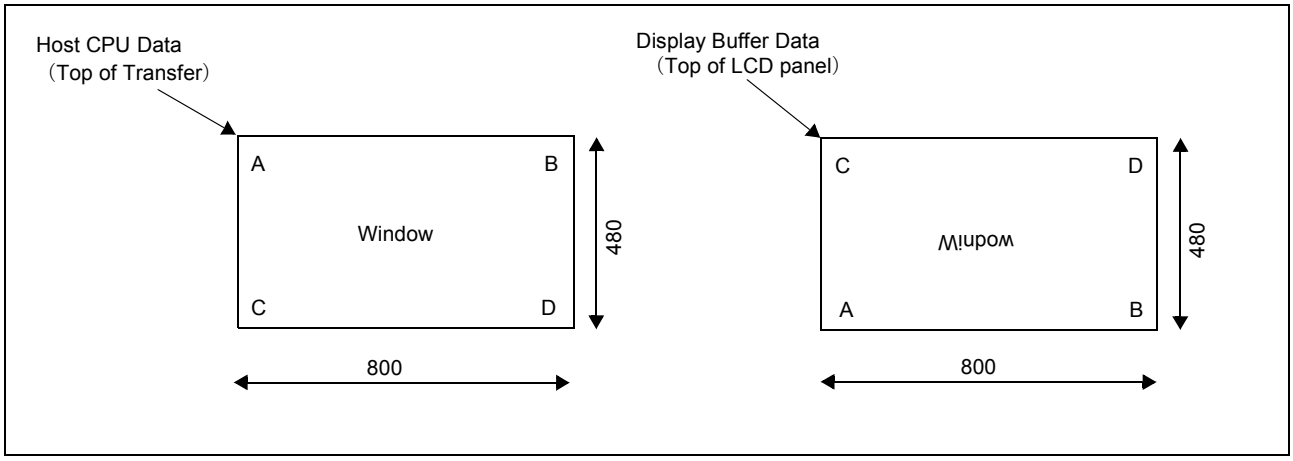


Figure 12-7: 180° Rotation and Mirror Example

12.4 Picture-in-Picture

The S1D13517 can display up to two PIP (Picture-in-Picture) windows that overlap the main display window. The PIP windows do not support transparent overlays, but provide windows that can be enabled/disabled without overwriting the display window image data.

The image data for the PIP windows must be input using the write window in the same manner as for the Display Window (see Section 12.1, "Display Window" on page 104). Typically, the PIP window image data is written to unused write buffers and the PIP1/PIP2 Display Start Address registers (REG[2Ch] ~ REG[30h] or REG[3Eh] ~ REG[42h]) are set to the beginning of selected write buffer. The PIP window position and size are configured using X/Y Start/End positions relative to the origin of the display.

If the PIP1 and PIP2 windows are overlapped, the PIP1 window appears "on top" of the PIP2 window.

12.4.1 Picture-in-Picture Window Settings

A PIP window size and position is specified using X/Y Start/End position registers. Each PIP window has it's own set of registers (PIP1: REG[32h] ~ REG[3Ch], PIP2: REG[44h] ~ REG[4Eh]). The PIP Window X/Y Start/End positions are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical).

Note

The PIP window must be positioned such that it remains within the dimensions of the LCD display.

The PIP window display start address is set to the beginning of the PIP window image data in the appropriate write buffer. The display start address can also be used to scroll PIP window image or provide basic animation. For more information on using the display start address in this manner, see Section 12.4.2, "Picture-in-Picture Window Display Start Address" on page 110.

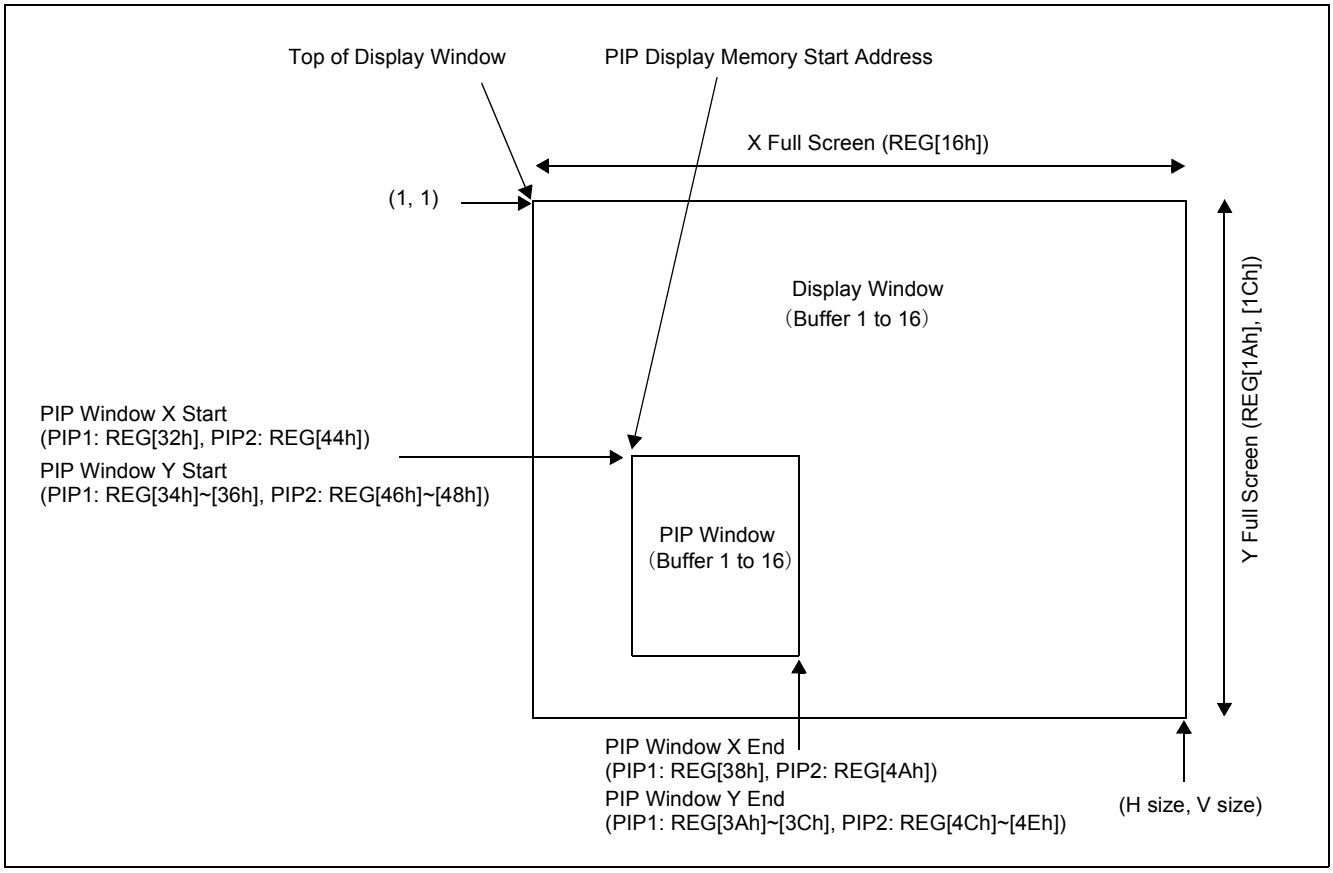


Figure 12-8: Picture-in-Picture Window Settings

The following example shows a PIP window overlapping a Display window.

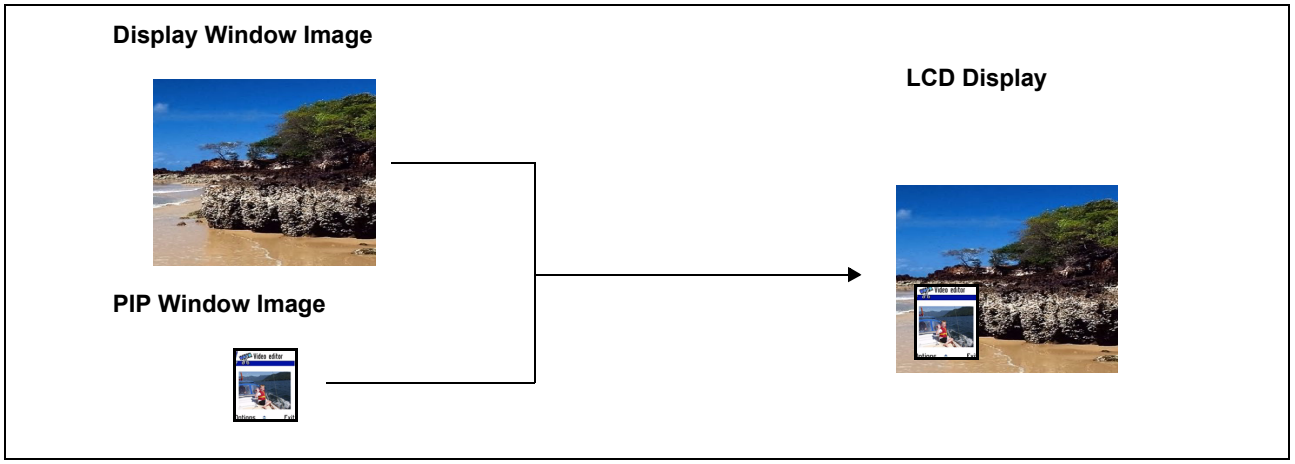


Figure 12-9: Picture-in-Picture Window Example

12.4.2 Picture-in-Picture Window Display Start Address

The PIP window display start addresses can changed to allow scrolling within an image larger than the PIP window or basic animation by changing the start address between a series of images. This method does not alter the image data in the write buffer, but simply changes the image data that is displayed within the PIP window.

For further information on calculating memory addresses, see <cross-ref to section 13.5>.

The following example shows a display window with a single PIP window. The write buffer containing the PIP window image data includes 4 separate images at DSA1, DSA2, DSA3, and DSA4. The PIP window images are "animated" by changing the PIP window display start address.

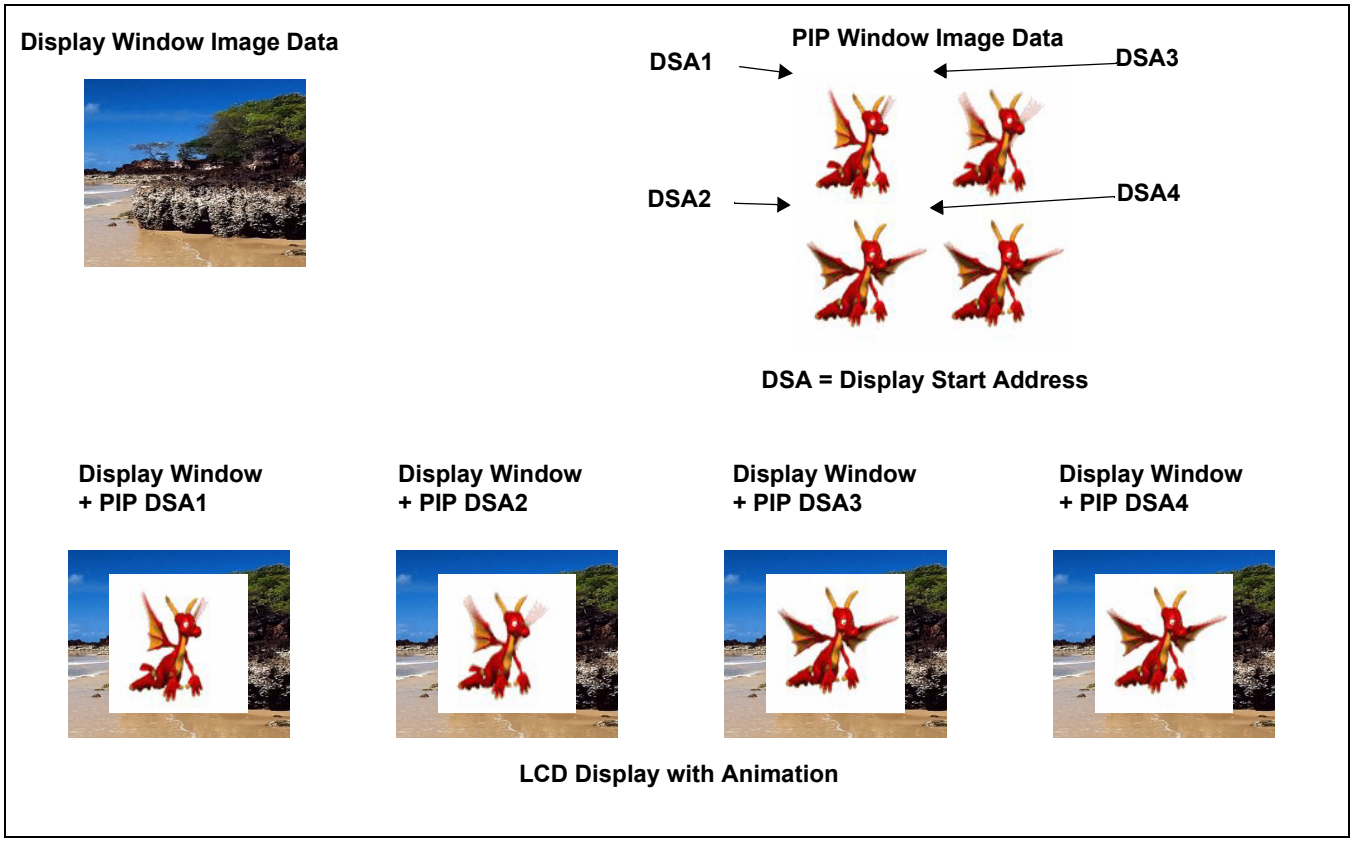


Figure 12-10: Animation Display Example

12.5 Double Buffer Display

The S1D13517 provides a display output mode which provides double buffering to prevent image tearing for streaming input. When this mode is selected (REG[2Ah] bits 3-1 = 001b), the display buffer is managed automatically. Image data is written to the write window as if a single buffer is being used. When the streaming image data is being input, the first frame is written to Buffer 1 and second frame is written to Buffer 2. Buffer 1 and 2 are fixed.

The buffer read/write pointers can only switch once per frame, at the beginning of the vertical non-display period. The pointers only switch if an animation frame has completed being updated within the last output frame period, and no new animation frame is currently being written. Because of this, each time the user finishes writing a frame of animation data, they should wait until the next vertical non-display period before writing the next frame. This can be accomplished by using the TE pin or by polling the Vertical Display Period Status (REG[6Ah] bit 7). Alternatively, if the user can guarantee that the maximum input animation data frame rate is 1/2 the LCD frame rate and that the burst length for writing a animation frame is less than one LCD frame period, then no checking for the vertical non-display period is required. However, if attention is not paid to allowing the pointers to switch, frames may be dropped.

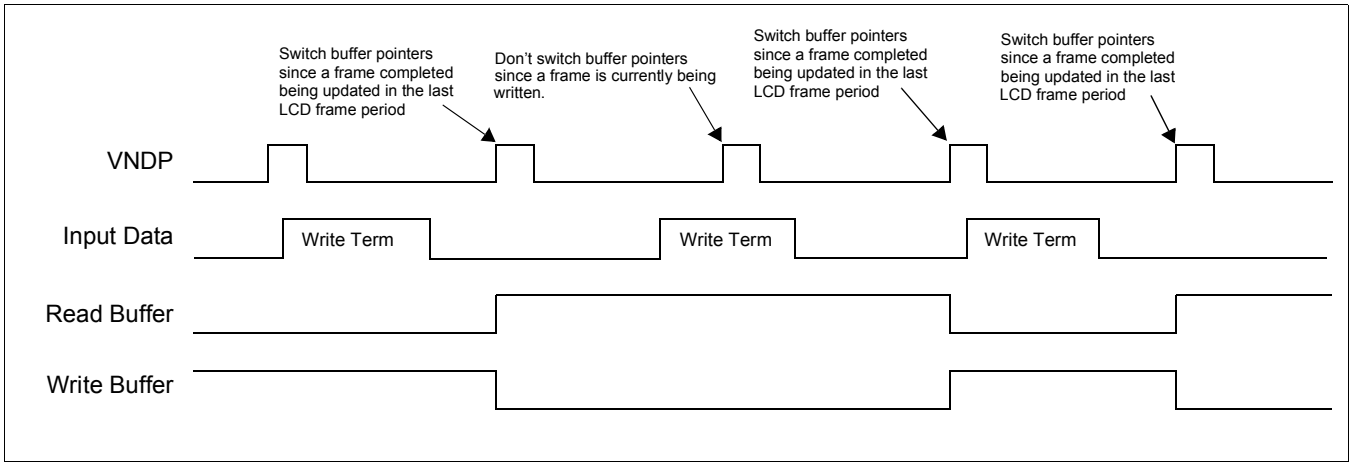


Figure 12-11: Double Buffer Switching

12.6 Alpha-Blend

Alpha-Blending is used in computer graphics to create the effect of transparency. This technique is useful for graphics that feature glass or liquid objects and is done by combining a translucent foreground with a background color to create a blend. It can also be used for animation, where one image gradually fades into another image.

The Alpha-Blend function blends either one or two images stored in the display buffer according to the selected alpha value. The output is written back to the display buffer again, and returned. Time is required to create the composite image and then write it back to the display buffer using the interval of the display cycle. An interrupt is available which signals the end of the Alpha-Blend and can be used to inform the host CPU.

12.6.1 Alpha-Blend (2 Input Mode)

In Alpha-Blend 2 Input Mode (REG[9Eh] bits 7-6 = 10b), the output window image is generated by blending the images from input windows 1 and 2. Either of the two input windows may overwrite the blended image by setting the desired input window to be the output window. All three windows must be the same size.

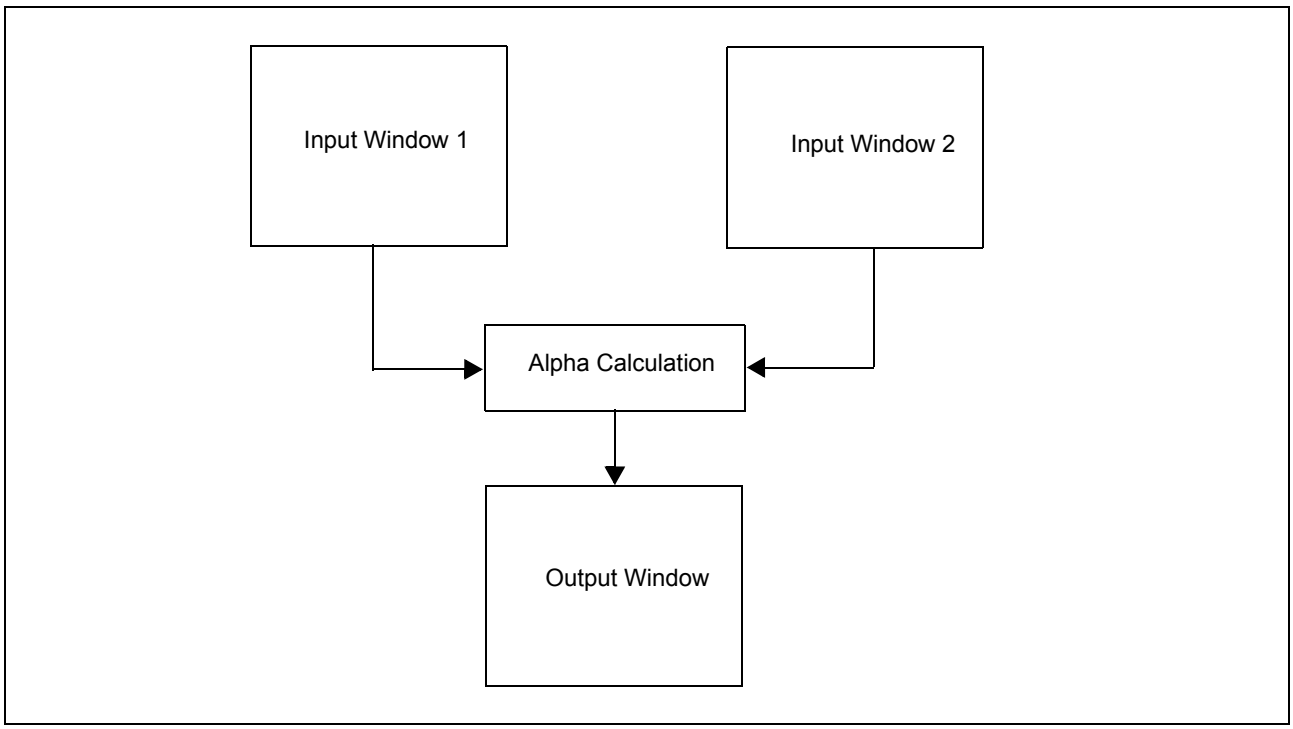


Figure 12-12: Alpha-Blend Data Flow (2 Input Mode)

The following shows an example of a 2 Input Mode Alpha-Blend.

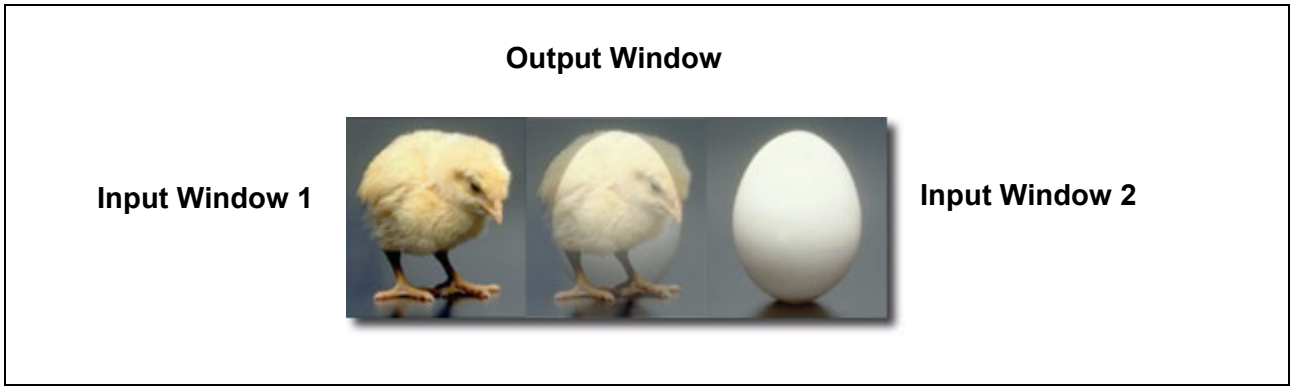


Figure 12-13: Alpha-Blend Example

12.6.2 Alpha-Blend (1 Input Mode)

When 1 Input Mode is selected (REG[9Eh] bits 7-6 = 11b), the Alpha-Blend function creates the output image from only input image 1. It is possible to make the output image a copy of input image 1 by specifying an alpha value of 32/32. The size of two images should be made the same.

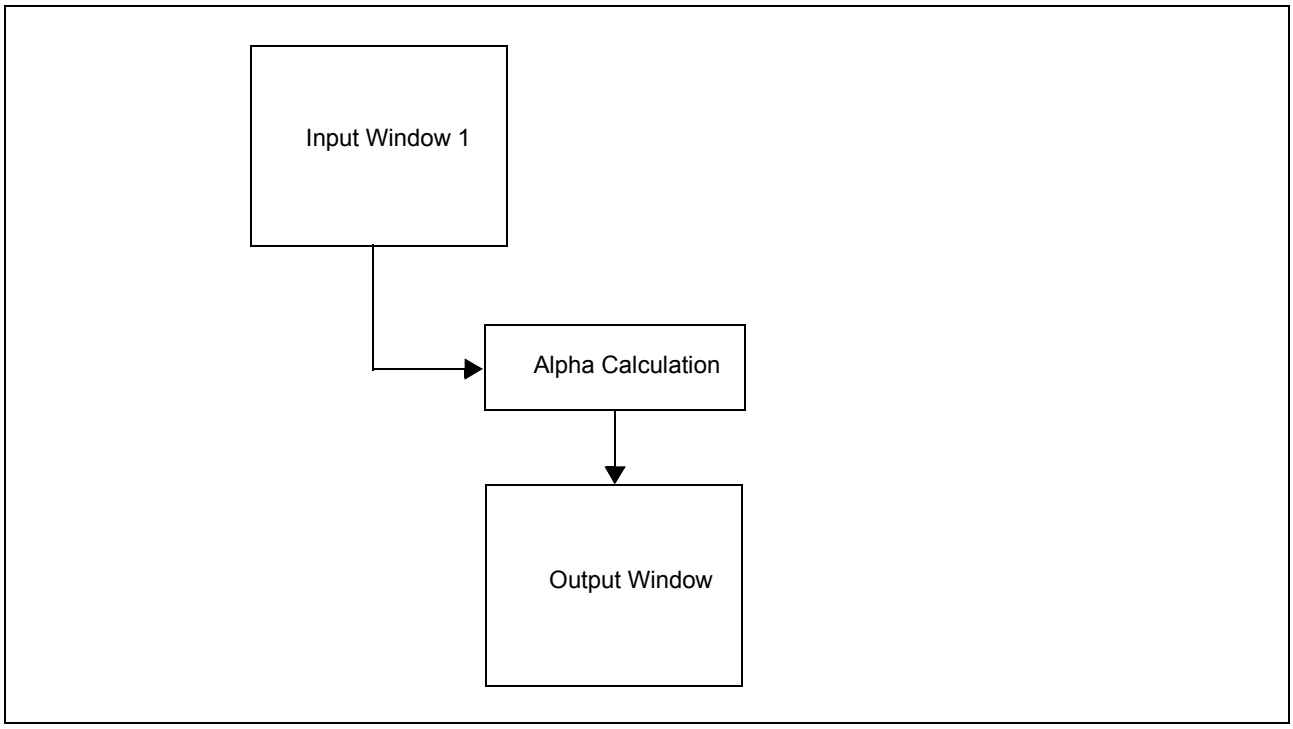


Figure 12-14: Alpha-Blend Data Flow (1 Input Mode)

12.6.3 Alpha-Blend Window Settings

The size of the Alpha-Blend input/output images is set using Horizontal Size (REG[98h]) and Vertical Size (REG[9Ah] ~ REG[9Ch]) registers. The horizontal size is set in 8 pixel resolution and the vertical size is set in 1 line resolution. The input/output image start addresses must be set in eight pixel/one line resolution depending on the address of SDRAM.

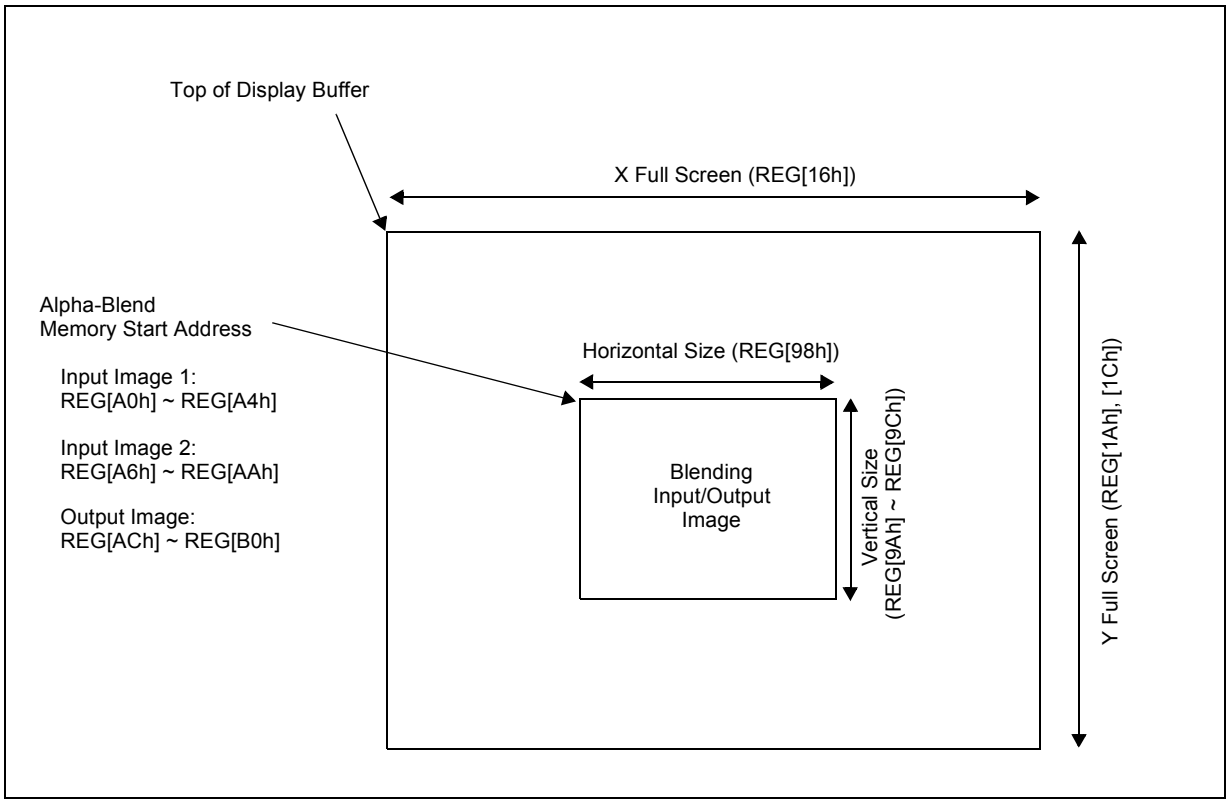


Figure 12-15: Alpha-Blend Window Settings

12.6.4 Alpha-Blend Processing Time

The Alpha-Blend processing time changes depending on the SDCLK frequency and the Alpha-Blend image size because the Alpha-Blend function operates by using the SDRAM memory.

12.6.5 Alpha-Blend Programming Sequence

The following sequence should be used to setup and perform and Alpha-Blend. The sequence assumes that the input images are already loaded into the display buffer.

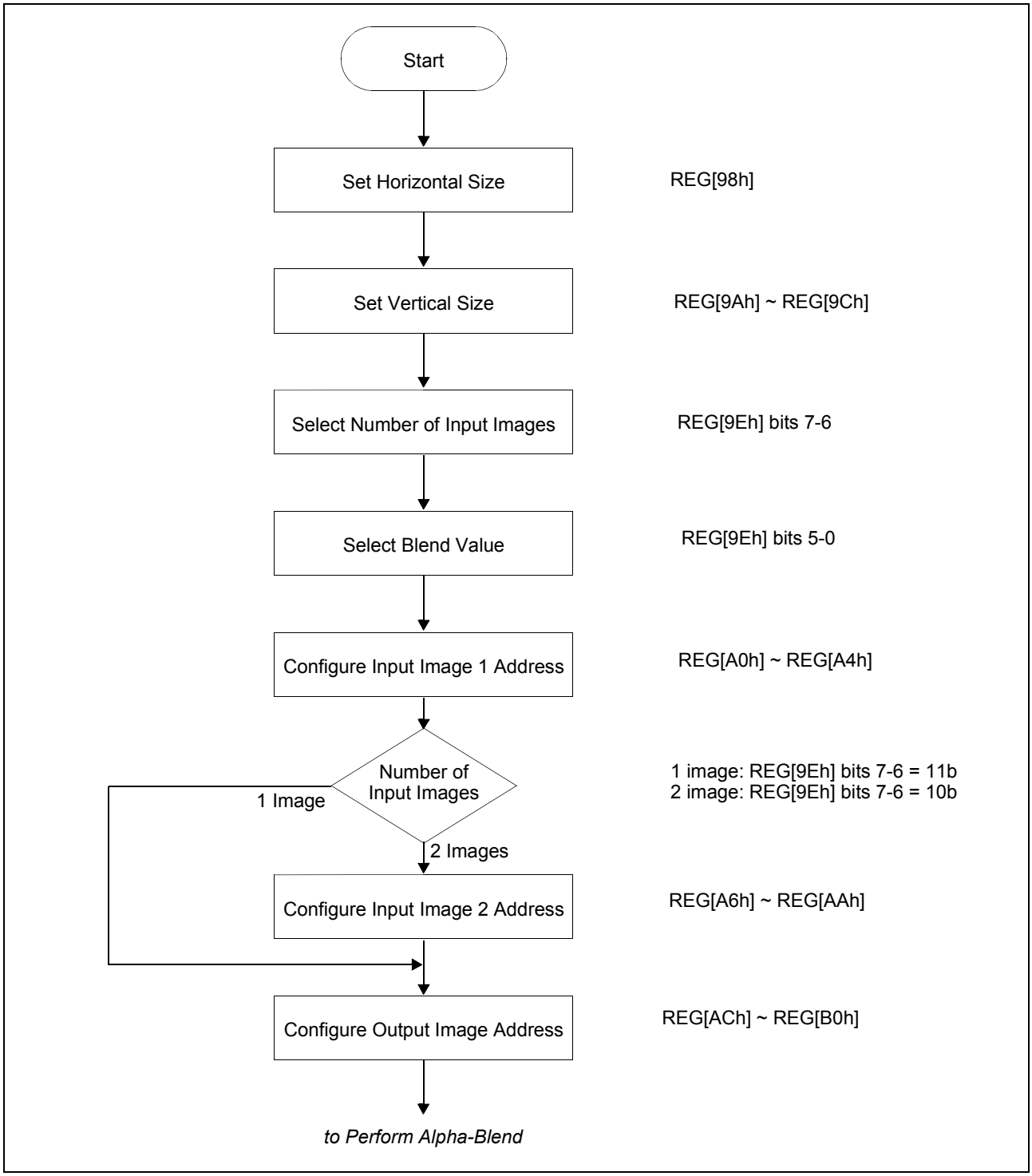


Figure 12-16: Alpha-Blend Setup Sequence

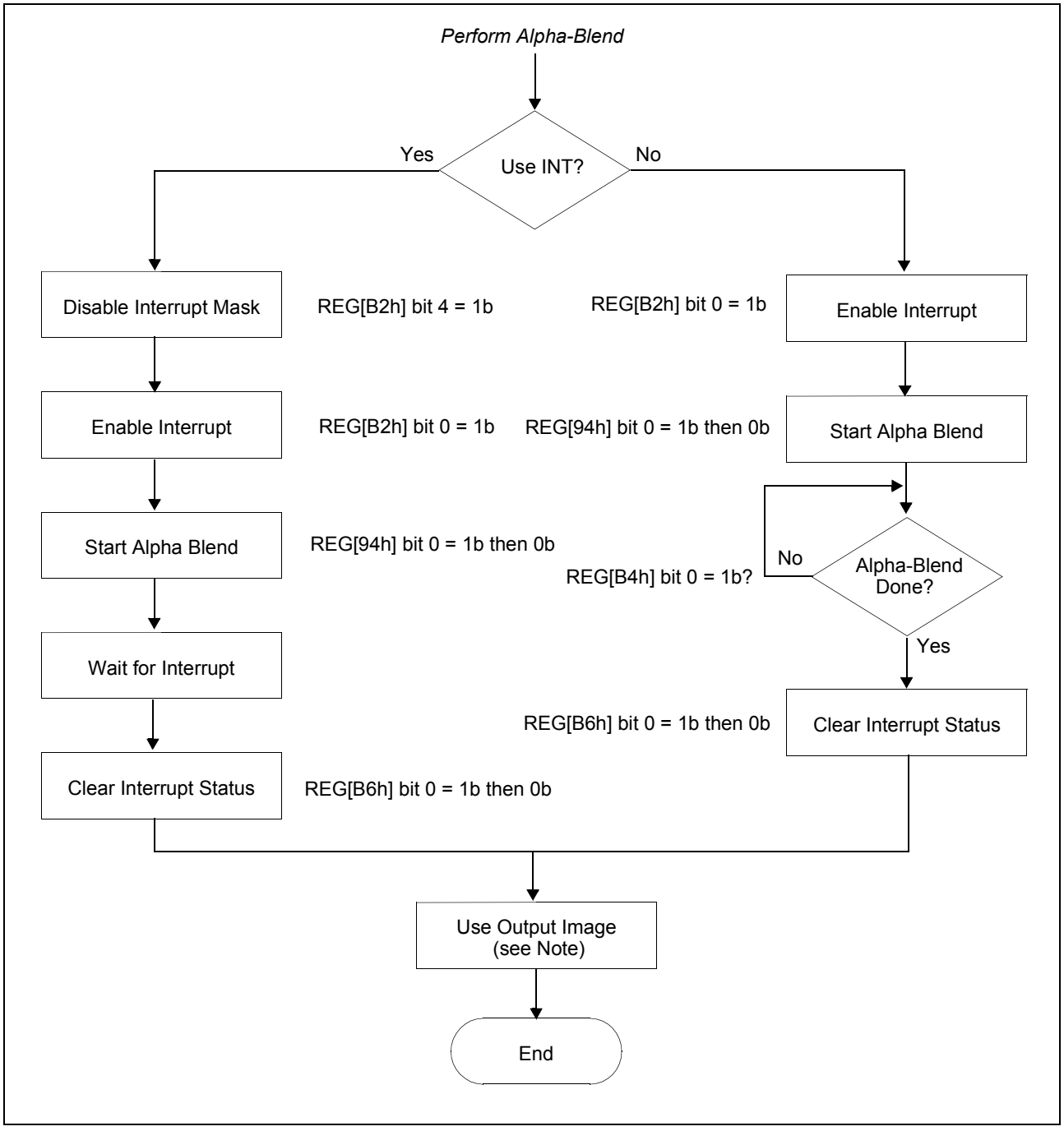


Figure 12-17: Perform Alpha-Blend Sequence

Note

One method of using the Alpha-Blend output image is setting the output image address to a PIP window and enabling the PIP window once the Alpha-Blend is complete.

Chapter 13 SDRAM Interface

The SDRAM interface accesses external 16/64/128 Mbit single data rate SDRAM effectively by using bank interleave. The initialization sequence and the auto refresh cycle are executed with hardware.

13.1 SDRAM Initialization

SDRAM must be initialized after resetting hardware. After hardware is reset, an initialization command can be executed only once. The command is ignored after initialization.

The initialization sequence is as follows.

1. Set the size setting register (REG[82h] bits 1-0) according to the memory size of SDRAM used.
2. Set the refresh counter (REG[8Ch] ~ REG[8Eh]) according to the clock frequency of SDRAM used (change from default value is unnecessary for 66MHz or higher).
3. Set the Auto Refresh Enable bit (REG[84h] bit 7) to 1b and the SDRAM Initialization bit (REG[84h] bit 1) to 1b.

Steps 4 through 7 are automatically executed in hardware.

4. Wait for SDRAM initialization start.
5. Precharge all commands are issued.
6. The auto refresh command is issued ten times.
7. The MRS command is issued. (The setting of the MRS register is unnecessary.)
8. Poll the initialization status bit (REG[86h] bit 1) with software until the bit = 1b (initialization end) or wait the processing time of steps 4 through 7 (30,000 clocks of SDCLK).
9. SDRAM can now be used.

13.2 SDRAM Connection

When a 16M bit SDRAM is used, the MBA0 pin is connected to the bank signal of the SDRAM.

When the MBA0 and MA11 pins are not used, they must be left unconnected.

13.3 SDRAM Commands

This section explains the SDRAM interface commands.

13.3.1 MRS Command

The setting of the mode register of SDRAM command (MRS) is automatically executed by hardware in the initialization sequence. S1D13517 is set as follows.

Table 13-1: MRS Setting

MRS	Setting Value
Burst Length	4
Lap Type	Sequential
CAS Latency	2
Option	All “0”

13.3.2 Read / Write Command

Read/Write of SDRAM is accessed respectively by the bank interleave every four bursts. Auto precharge is always enabled (MA10 = Low), and the CAS latency is fixed to two.

13.3.3 Auto Refresh Command

Auto refreshing of SDRAM is automatically executed by hardware by an internal refreshing counter. Set the value of the refresh cycle counter according to the clock frequency of SDRAM used. When the clock frequency is 66MHz or higher, it is not necessary to change the register from the default value.

13.3.4 Self Refresh Command

The SDRAM self-refresh is enabled/disabled with the SDRAM Self Refresh Enable bit (REG[84h] bit 3) by software. This command must be set when SDRAM controller is idle status (REG[86h] bit 6 = 1).

13.3.5 Power Down Command

The SDRAM power save can be enabled/disabled by the SDRAM Power Save Enable bit (REG[84h] bit 2) by software. This command must be set when SDRAM controller is idle status (REG[86h] bit 6 = 1).

13.3.6 Controller Status

The status of the SDRAM controller is indicated by bit REG[86h] bit 6. If the SDRAM controller is move to the idle status (REG[86h] bit 6 = 1), it is necessary to stop the access to SDRAM with disabling LCD display (REG[2Ah] bit 0 = 0) and Alpha-Blend (REG[9Eh] bit 7 = 0). Please put the SDRAM controller into power save state before disabling SDCLK for power saving (REG[68h] bit 0 = 0).

13.4 Memory Data

The input image is stored in memory as 24bpp. If the image data is RGB 5:6:5 format, it is converted into RGB 8:8:8 format before being stored, as shown in Table 13-3:, “16bpp (RGB 5:6:5) Input Display Data”.

The data format stored in SDRAM is as follows.

Table 13-2: 24bpp (RGB 8:8:8) Input Display Data

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
0004h	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0
0006h	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0

Table 13-3: 16bpp (RGB 5:6:5) Input Display Data

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^7	G_0^6	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^7	B_0^6	B_0^5
0002h	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^7	B_1^6	B_1^5	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^7	R_0^6	R_0^5
0004h	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^7	R_1^6	R_1^5	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^7	G_1^6
0006h	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	G_2^7	G_2^6	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	B_2^7	B_2^6	B_2^5

13.5 Memory Address

If the memory address of an image in SDRAM must be entered into the registers to use the display or the Alpha-Blend function, the following method should be used to calculate the memory address.

Image data is arranged in SDRAM using three bytes for each pixel (see <cross-reference to section 13.4>). To determine the address of an image, the top left corner of the image must be calculated based on the X/Y start coordinates of the image data using the following formula. The memory address must be specified as a byte address.

Image address = buffer n + (Ystart x HDW x 3 bytes) + (Xstart x 3 bytes)

Where:

- Buffer n is the memory start address of the write buffer containing the image data. The address is calculated based on the SDRAM Write Buffer Memory Size in REG[90h]
- Ystart is the Y coordinate of the start of the image data relative to the start of write buffer n
- HDW is the horizontal display width as defined by REG[16h]
- Xstart is the X coordinate of the start of the image data relative to the start of write buffer n

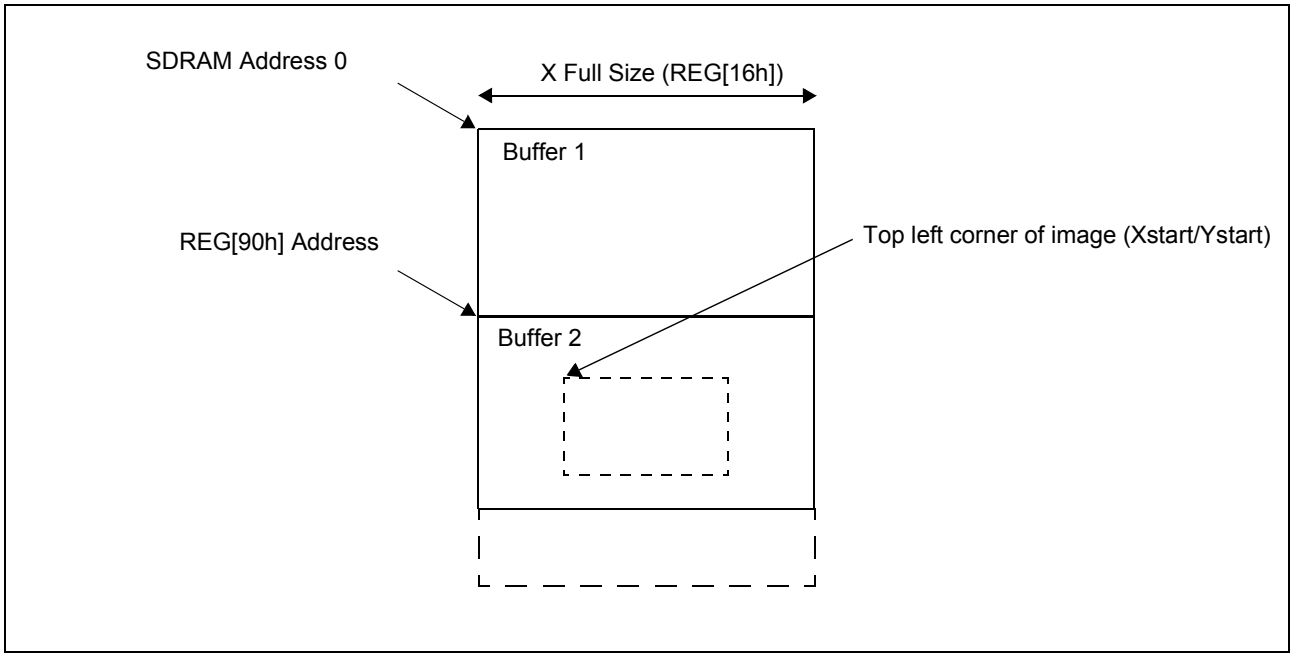


Figure 13-1: Image Address in Memory

Chapter 14 PWM Output

The PWM output can be used for the backlight control of the LCD panel. A high pulse width and the row pulse width are set to system clock (SYSCLK) with 32 bit counter. There is a bit (REG 70h bit 7) that updates the register in bulk though the PWM setting register has divided into two or more addresses.

Please make it to disabling (REG[70h] bit 2 = 0b) after it makes it to a logical of hope output by the register (REG[70h] bits 1-0) when you stop the PWM output.

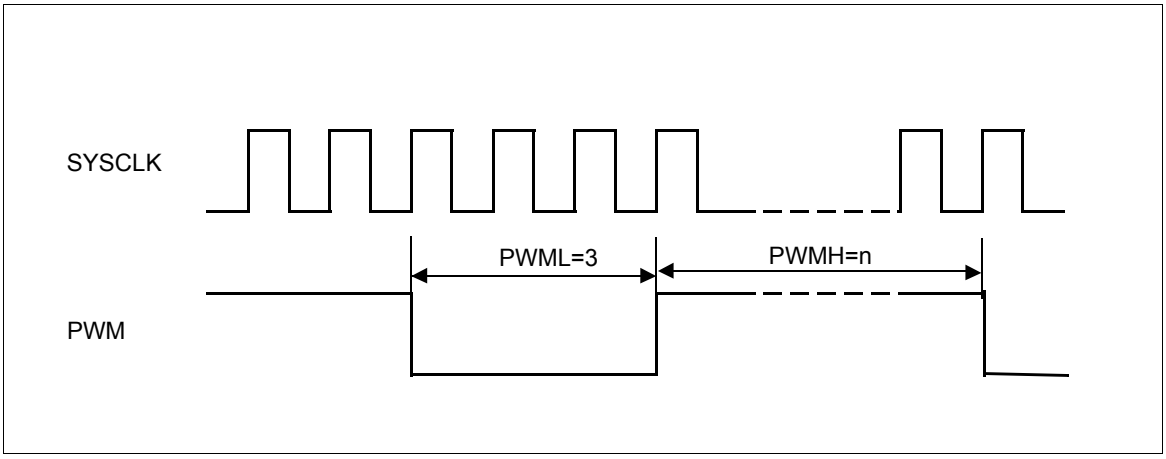


Figure 14-1: Example PWM Timing

Chapter 15 Color Bar Display Test

The test color bar display does not use the SDRAM memory and is selected when REG[2Ah] bits 3-1 = 111b

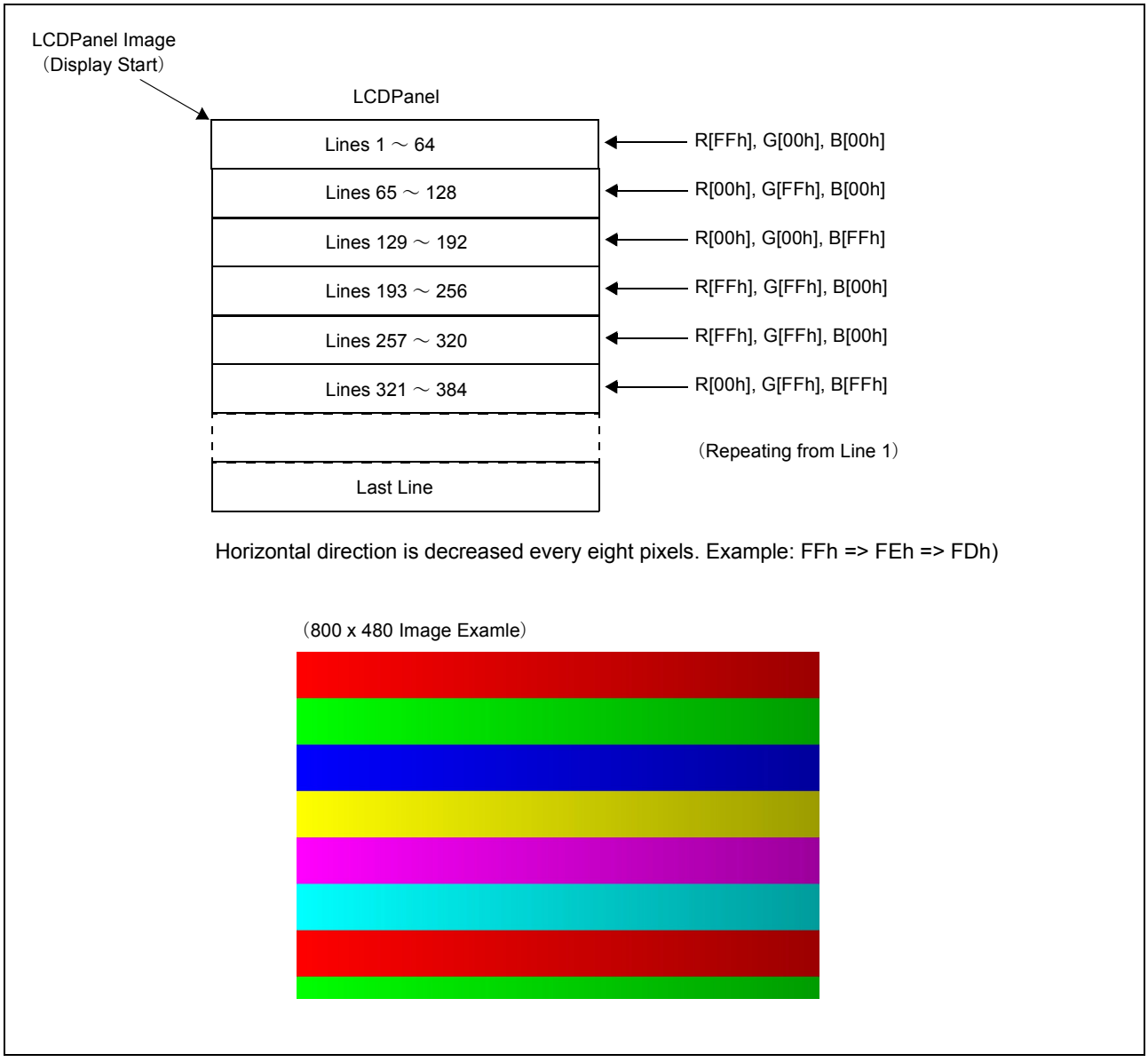


Figure 15-1: Color Bar Display Test

Chapter 16 Power Save

S1D13517 can control power with software. The operation sequence is shown as follows.

16.1 Sleep Mode

While in sleep mode all internal clocks are disabled including the PLL. On return from sleep mode, the PLL needs 10ms to stabilize. Memory cannot be accessed while in sleep mode. All registers are accessible while in sleep mode.

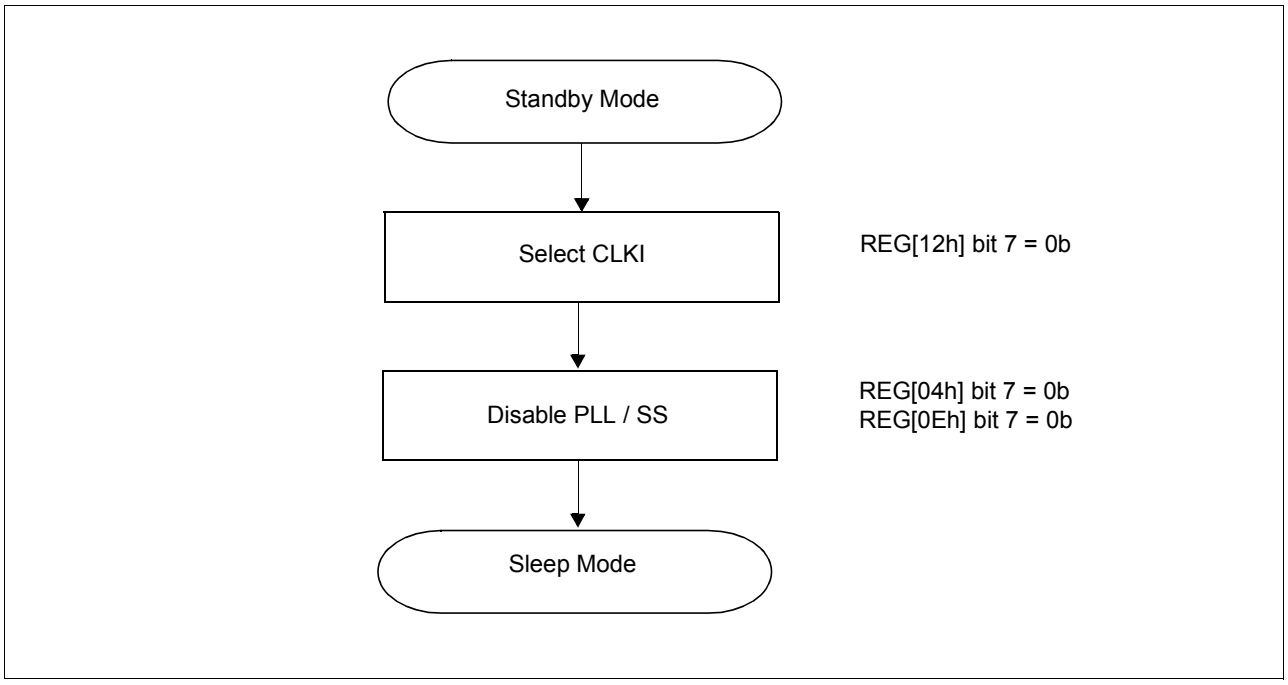


Figure 16-1: Recommended Procedure for Entering Sleep Mode

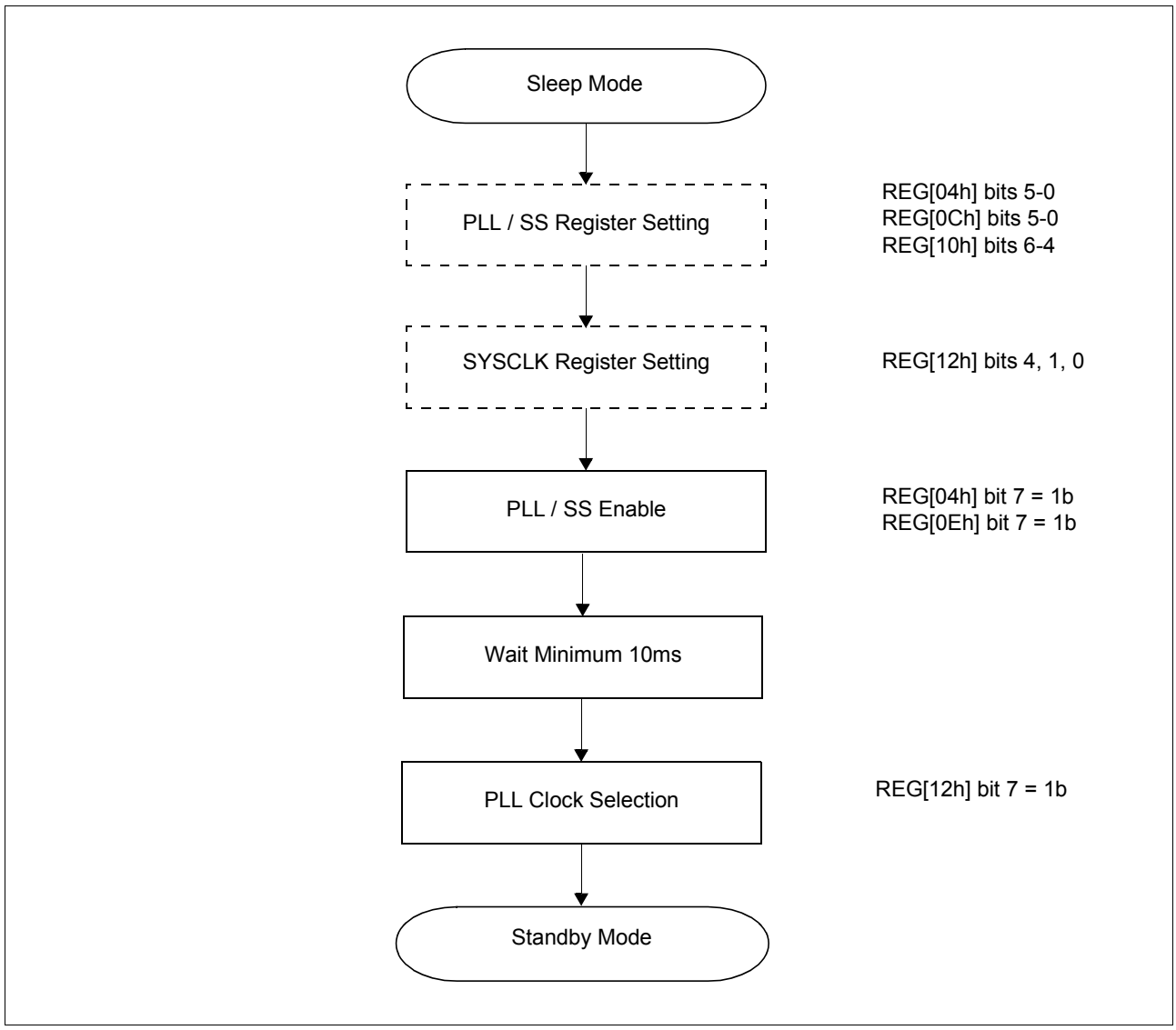


Figure 16-2: Recommended Procedure for Exiting Sleep Mode

16.2 Standby Mode

In the standby mode, all internal clocks except the PLL are disabled. Image data can be input immediately after this mode is exited. Registers can be accessed while in standby mode.

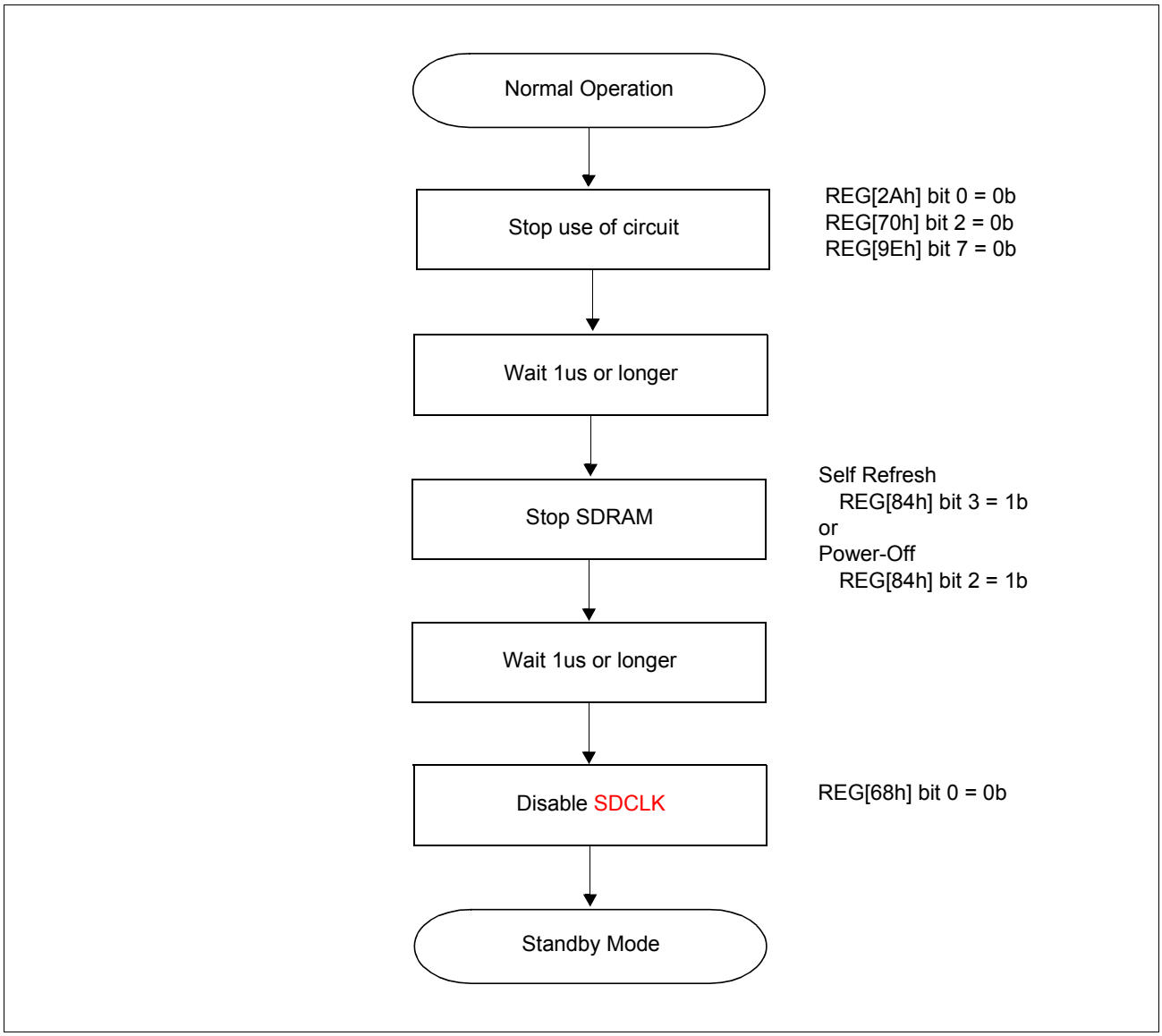
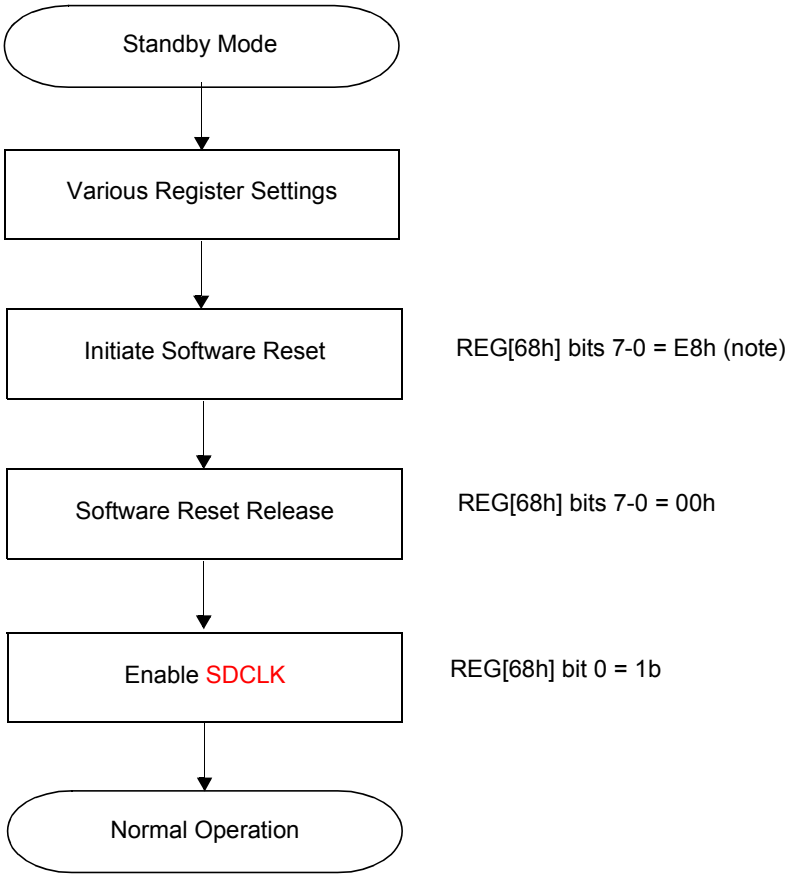


Figure 16-3: Recommended Procedure for Entering Standby Mode



Note
SDRAM must be initialized (see Section 13.1, “SDRAM Initialization” on page 117).

Figure 16-4: Recommended Procedure for Exiting Standby Mode

Chapter 17 Use Case Examples

17.1 Initialization Sequence

The following steps are required to initialize S1D13517.

- Set the PLL frequency.
- Set the system clock (SYSCLK).
- Set up the timing and the polarity of signals to the LCD panel.
- Set the SDRAM type.
- Return from sleep mode to standby mode.
- Return from the standby mode to normal operation.

The example on the following page is for a WVGA panel.

Conditions:

- CLKI: 24MHz
- PCLK: 30MHz
- SDRAM clock: 90MHz
- LCD panel: 800x480 (24bpp)
- SDRAM: 64 Mbit
- SS: is enabled.

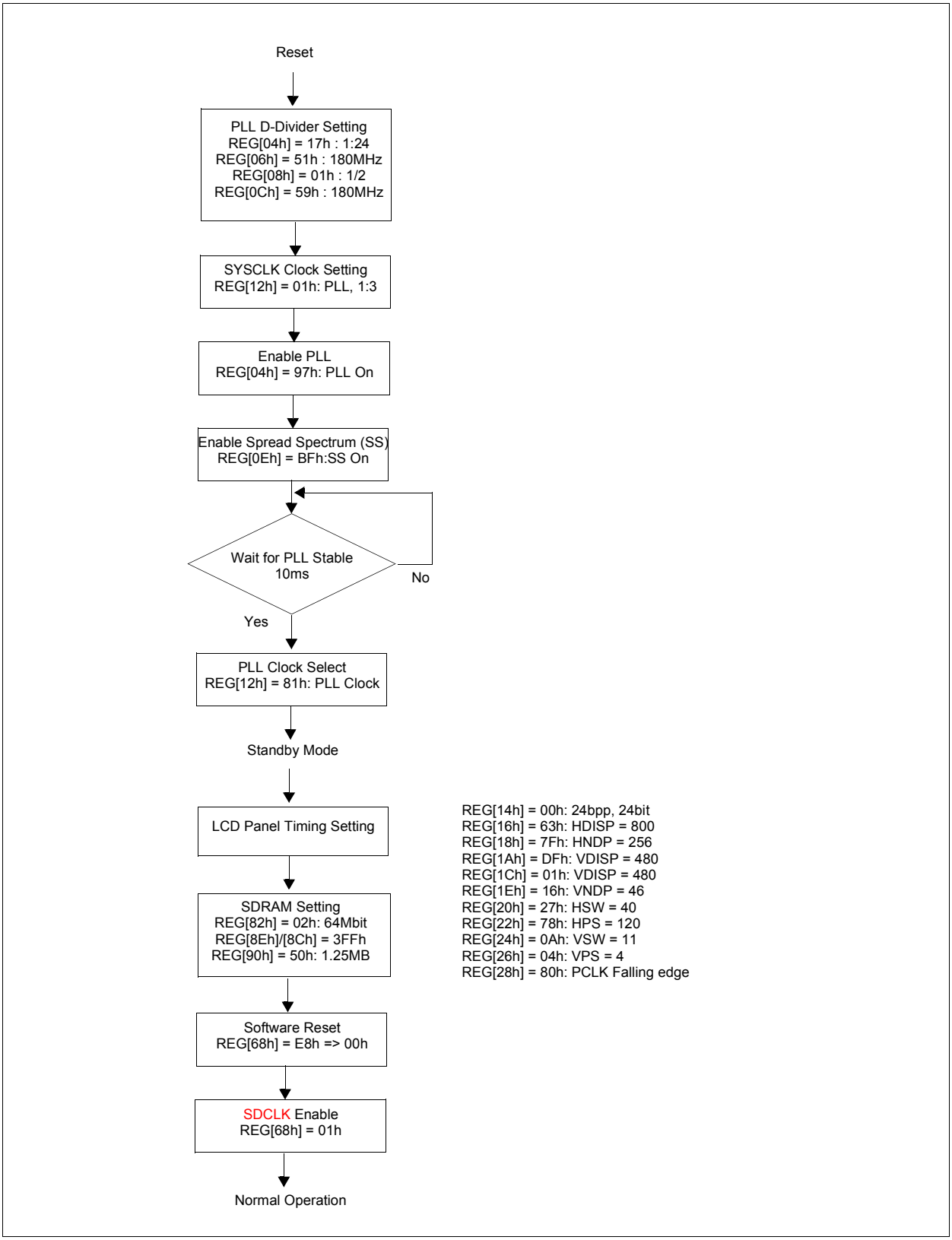


Figure 17-1: Typical S1D13517 Initialization Sequence

17.2 Display Initialization Sequence

The following steps are required to initialize the S1D13517 Display.

- Initialize the SDRAM
- Set the display mode
- Set the image window size
- The image data is Burst Write
- Enable the LDC display
- Write the image data (repeat if necessary)

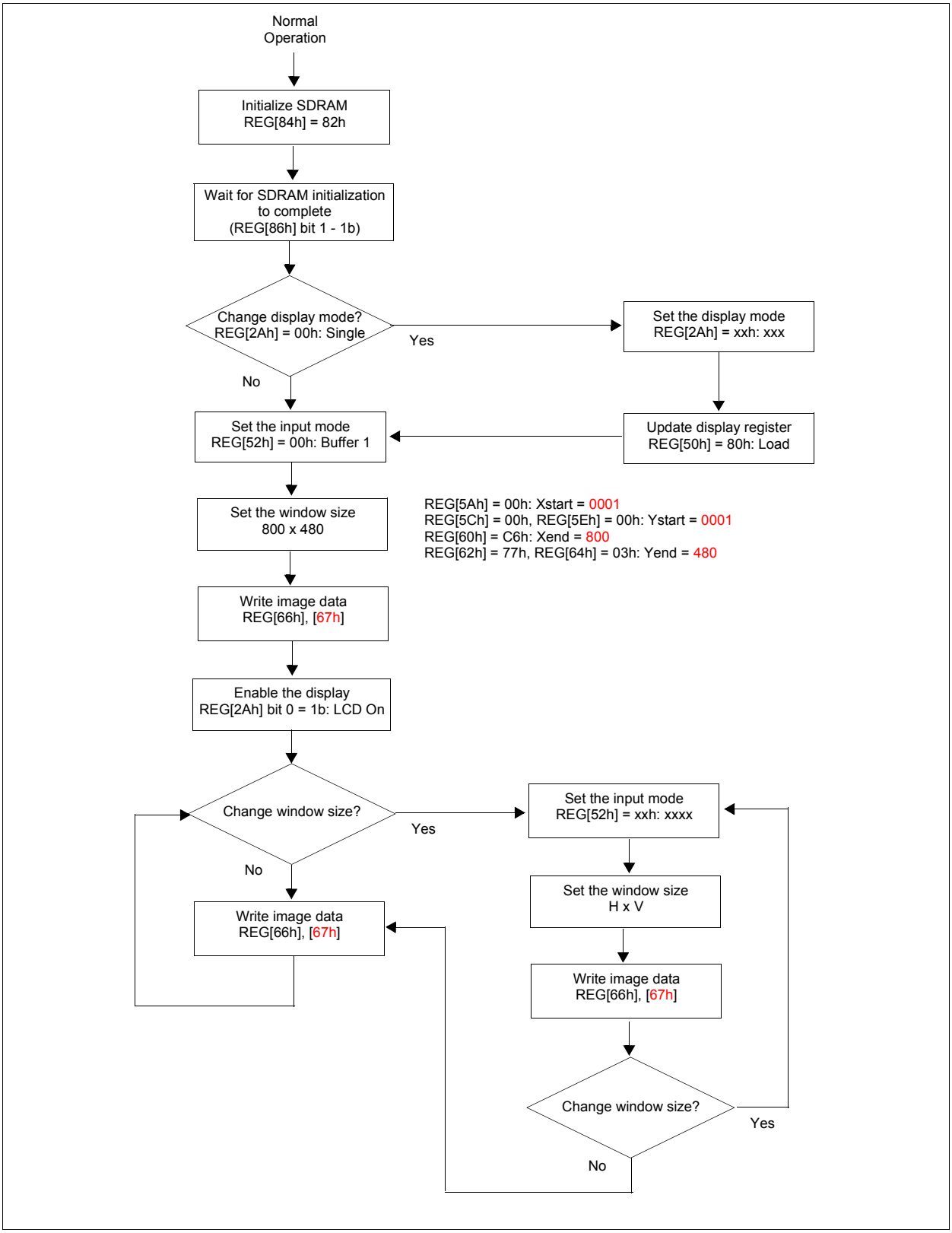


Figure 17-2: Typical Display Initialization

Chapter 18 PLL

18.1 PLL External Low-Pass Filter

The following external low-pass filter is recommended for use with the PLL.

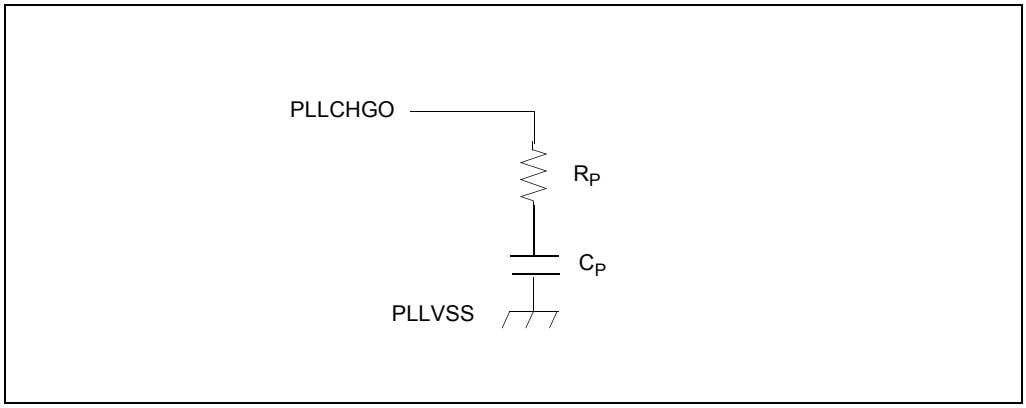


Figure 18-1: PLL external low-pass filter recommendation parts

Table 18-1: Recommended Values for R_P and C_P

PLL Frequency	R_P	C_P
50~74MHz	1KΩ	2000pF
76~100MHz	2KΩ	2000pF
102~180MHz	3KΩ	2000pF

18.2 Guidelines for PLL Power Layout

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL, resulting in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

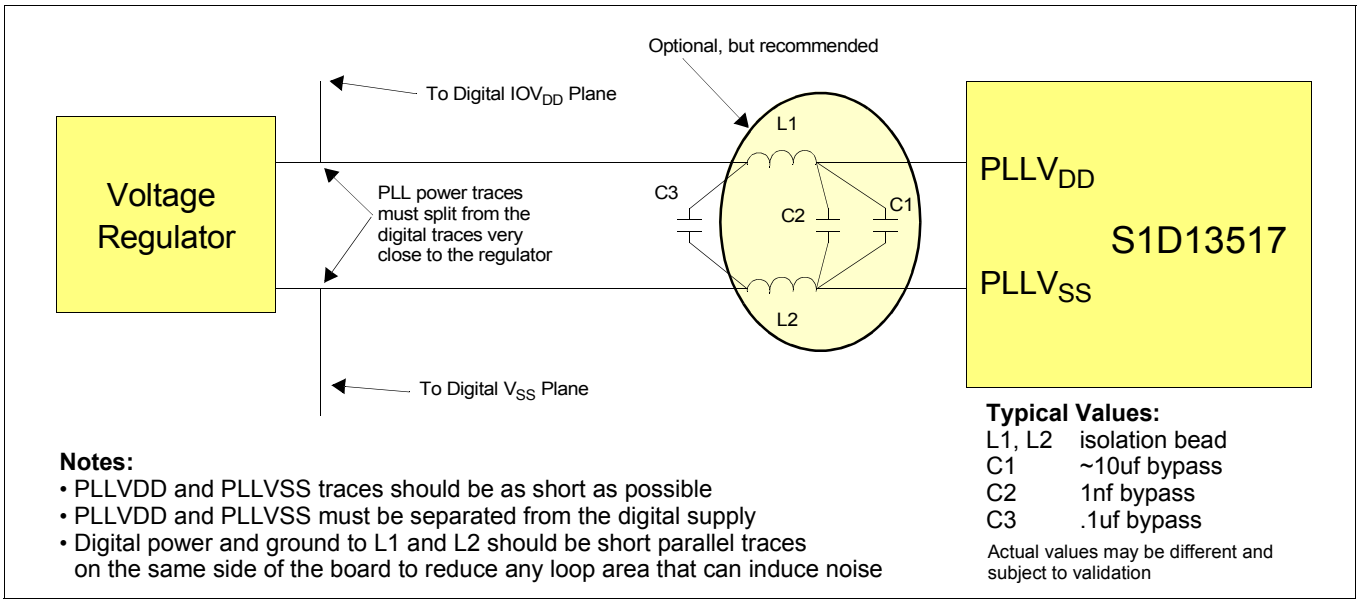


Figure 18-2: PLL Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the MGE ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.

- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

Chapter 19 Mechanical

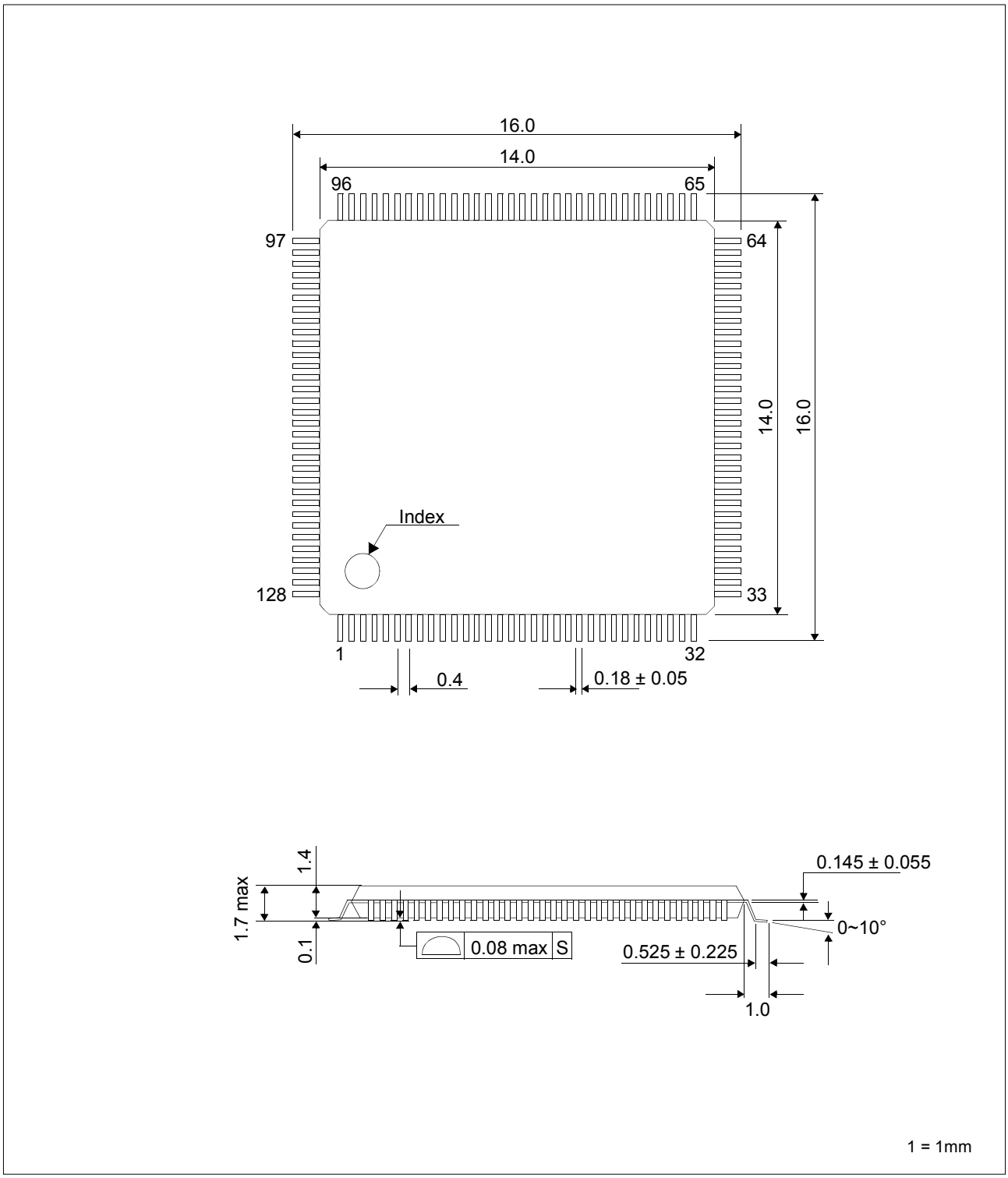


Figure 19-1: QFP15 128-pin Package

Chapter 20 Change Record

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- chapter 2.5 Display Support - change bulleted text “Maximum 1024 x 1024 display...” to “Maximum 960 x 960 display...”
- chapter 2.5 Display Support - change 16/18/24bpp to 16/18/24-bit
- chapter 2.6 Display Features - rewrite section
- chapter 6.2.1 Host Interface - add paragraph “For a summary of the Host pin mapping...” and in table add register REG[6Ah] reference to TE/INT pin Description
- chapter 6.2.2 LCD Interface - add paragraph “For a summary of the LCD pin mapping...”
- chapter 6.2.5 Miscellaneous - for CNF[2:0] description add reference to section 6.4
- chapter 6.2.5 Miscellaneous - for PLLGHGO description add reference to chapter 19
- chapter 6.4 Configuration Options - rewrite note after table
- chapter 8.2 Reset Timing - add t_{RESNC} to figure 8-, Reset Timing
- chapter 8.4.1 Indirect Intel80 Bus - correct a typo in note 3, change MD[7:0] to HD[7:0]
- chapter 8.4.2 Indirect ALE Bus - correct a typo in note 3, change MD[7:0] to HD[7:0]
- chapter 8.6 LCD Interface Timing - in table 8-12, *Panel Timing Parameters*, change VSW Register bits to 5-0 and Max value to 64
- chapter 8.6 LCD Interface Timing - in table 8-12, *Panel Timing Parameters*, change HDISP and VDISP Max to 960
- chapter 9.1 Clock Descriptions - changes to register references in figure 9-1 *Clock Block Diagram*
- chapter 9.3 Clock Control - in note, change all instances of SYSCLK to SDCLK
- REG[04h] bit 7 - in note, change SYSCLK to SDCLK
- REG[04h] bits 5-0 - rewrite note “Depending on CLKI, these bits...” and in the table, change M-Divide to D-Divide
- REG[08h] bit 0 - rewrite bit description
- REG[0Ch] bits 6-0 - add note 1 “The PLL output range is minimum 50MHz (REG[0Ch] = 18h), and maximum 180MHz (REG[0Ch] = 59h)”
- REG[0Eh] bit 7 - in note, change SYSCLK to SDCLK
- REG[12h] bit 4 - rewrite bit description
- REG[12h] bits 1-0 - in note, change SYSCLK to SDCLK
- REG[14h] bits 2-1 - rename these bits to “Input Image Format” and add note to bit description
- REG[16h] - update the formula in the bit description and in the note change the maximum to 960 pixels
- REG[18h] - rename these bits to “Horizontal Non-Display Period” and in the note, change HS Start to HPS and HS Width to HSW

- REG[1Ah] ~ REG[1Ch] - in the note change the maximum to 960 lines
- REG[1Eh] - in note change maximum to 512 lines
- chapter 10.3.4 Display Mode Registers - change section name to “Display Mode Registers” from “Input Mode Register”
- REG[24h] bits 5-0 - in bit description formula, change PVS to VSW
- REG[2Ah] bit 0 - in bit description change “internal system clock” to SDCLK
- REG[32h] - add notes “The value of this register...” and “The PIP1 window must be positioned such that...”
- REG[34h] ~ REG[36h] change register bit order
- REG[34h] ~ REG[36h] - add note “The PIP1 window must be positioned such that...”
- Reg[38h] - changes to formula in bit description and add notes “The value of this register...” and “The PIP1 window must be positioned such that...”
- REG[3Ah] ~ REG[3Ch] change register bit order
- REG[3Ah] ~ REG[3Ch] - add note “The PIP1 window must be positioned such that...”
- REG[44h] - remove “Display” from register and bit names and add note 2 “The PIP2 window must be positioned such that...”
- REG[44h] - add note “The value of this register...”
- REG[46h] ~ REG[48h] change register bit order
- REG[46h] ~ REG[48h] - add note “The PIP2 window must be positioned such that...”
- REG[4Ah] - add note 2 “The PIP2 window must be positioned such that...”
- Reg[4Ah] - changes to formula in bit description and add note “The value of this register...”
- REG[4Ch] ~ REG[4Eh] change register bit order
- REG[4Ch] ~ REG[4Eh] - add note “The PIP2 window must be positioned such that...”
- REG[50h] - change default value to “not applicable”
- REG[52h] bit 7 - rewrite bit description
- REG[52h] bit 3 - rewrite bit description
- REG[52h] bit 1 - rewrite bit description
- REG[52h] bit 0 - rewrite bit description
- REG[54h] - correct typo in bit description, change REG[53h] to REG[52h]
- REG[56h] - correct typo in bit description, change REG[53h] to REG[52h]
- REG[58h] - correct typo in bit description, change REG[53h] to REG[52h]
- REG[5Ah] - add note “The value of this register...”
- REG[5Ch] ~ REG[5Eh] - change register order in formula

- REG[60h] - change register reference REG[34h] to REG[52h], changes to formula in bit description and add note “The value of this register...”
- REG[62h] ~ REG[64h] - change register reference REG[34h] to REG[52h] and change register order in formula
- REG[66h] ~ REG[67h] - change register default values to “not applicable”
- REG[66h] ~ REG[67h] - correct typos in bit description, correct register numbers and “internal system clock (SYSCLK)” to SDCLK
- REG[68h] bit 0 - in bit description rename bit to “SDCLK Enable” and change SYSCLK to SDCLK
- chapter 10.3.8 General Purpose Output Pins Registers - change section name from IO to Output and add note “When 18-bit TFT is selected...”
- REG[84h] - change register default value to “not applicable”
- REG[86h} bit 6 - reserve this bit
- REG[86h} bit 1 - in bit description, change reference to REG[84h] bit 3 to REG[84h] bit 1
- REG[94h] - change register default value to “not applicable”
- REG[96h] - reserve this register
- REG[B6h] - change register default value to “not applicable”
- chapter 11.1.3 Memory Write (New Window) Procedure - in #3 change “five” to “six”
- chapter 12 Display Functions - rewrite entire section
- chapter 12.1.2 Display Window Setting - at the end of the first paragraph change “a multiple of eight” to “an eight pixel resolution”
- chapter 12.2.1 Picture-in-Picture Window Setting - at the end of the first paragraph change “a multiple of eight” to “an eight pixel resolution”
- chapter 13.3.6 Controller Status - in first paragraph change SYSCLK to SDCLK
- chapter 13.5 Memory Address - rewrite section
- chapter 15 Alpha-Blend Interrupt Circuit - move the figure and text to chapter 10.3.12 and delete this section
- chapter 16.2 Standby Mode - change SYSCLK to SDCLK in figure 16-3 *Recommended Procedure for Entering Standby Mode* and figure 16-4 *Recommended Procedure for Exiting Standby Mode*
- chapter 17.1 Initialization Sequence - change SYSCLK to SDCLK in figure 17-1 *Typical S1D13517 Initialization Sequence*
- chapter 17.2 Display Initialization Sequence - correct typos in figure 17-2 *Typical Display Initialization*, change “REG[66h], [68h]” to “REG[66h], [67h]”
- chapter 17.2 Display Initialization Sequence - correct typos in figure 17-2 *Typical Display Initialization*, change REG[5Ah] = 00h: Xstart = 0001, REG[5Ch] = 00h, REG[5Eh] = 00h: Ystart = 0001, REG[60h] = C6h: Xend = 640, and REG[62h] = 77h, REG[64h] = 03h: Yend = 480

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- chapter 5 Display Data Path - in figure 5-1, change “Main Window” to “Write Window”

- chapter 6.2.3 SDRAM Interface - change pins MCS#, MRAS#, MCAS#, MWE# and MCKE SDRAM Reset state / SDRAM Power Save Status to “H”, and change MCLKO SDRAM Reset state / SDRAM Power Save Status to “H or L”
- REG[32h] - change equation in bit description
- REG[38h] - change equation in bit description
- REG[44h] - change equation in bit description
- REG[4Ah] - change equation in bit description
- REG[5Ah] - change equation in bit description
- REG[5Ch] ~ REG[5Eh] - correct typos in bit designations of register table
- REG[60h] - change equation in bit description
- REG[62h] ~ REG[64h] - correct typos in bit designations of register table

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- chapter 4 Block Diagram - in figure 4-1 change “SDCLK” to MCLKO
- section 6.2.5 Miscellaneous - in table change TEST[1:0] and SCANEN descriptions to “...should be connected to VSS”
- section 8.4.1 Indirect Intel80 Bus - in table 8-9 Intel80 Bus A.C. Characteristics, change t_{rodh} MIN to “1”
- section 8.4.2 Indirect ALE Bus - in table 8-10 ALE Bus A.C. Characteristics, change t_{rodh} MIN to “1”
- section 8.5 SDRAM Interface Timing - in table 8-11 SDRAM Interface Timing, change t_{mcl1} and t_{mch1} MIN to “$0.3t_{mcc}$ - 2”, and t_{mcl2} and t_{mch2} MIN to “$0.5t_{mcc}$ - 2”
- REG[08h] bit 0 - change name in bit description to match register table
- REG[10h] bits 6-4 - in table change Width of Frequency Change for other values to reserved
- REG[12h] bits 1-0 - in table change 00b SS Clock Source to “SS is not used”
- REG[2Ah] bits 3-1 - in table change Display Data Output for 010b, 011b and 100b to “PIP1 screen display”, “PIP2 screen display”, and “PIP1 and PIP2 screen display” respectively
- REG[2Ah] bit 0 - add “Changes to this bit are not synchronized with...” to bit description
- REG[50h] bit 7 - change bit name to “Display Setting Register Update”
- REG[5Ah] ~ REG[64h] - rename registers and bits to “Write Window...”
- REG[6Ah] bit 5 - correct typo in bit description, change “VP” to “VDP”
- REG[6Ah] bits 1-0 - in table change TE/INT Output Function for 10b to “HDP OR’d with VDP”
- REG[86h] bit 6 Change bit description to “...When this bit = 0b, the SDRAM Controller is busy or otherwise in use. When this bit = 1b, the SDRAM Controller is idle.”
- REG[A2h] bits 7-0 - remove typo from bit range in register table, change “bits 7-15-8” to “bits 15-8.
- REG[A4h] bits 7-0 - remove typo from bit range in register table, change “bits 7-23-8” to “bits 23-8.

- section 11.1.3 Memory Write (New Window) Procedure - change the section name from “New Window Write Procedure” and in step 3 change reference to REG[5Ch] to REG[5Ah]
- section 11.1.4 Memory Write (Update Window) Using Existing Window Coordinates - change the section name from “New Window Write Using Existing Window Coordinates”
- section 12.1.2 Display Window Setting - in figure 12-2 Display Window Setting, correct typos - change “Strra” to “Start”, “(0, 0)” to “(1, 1)”, and “(H size - 1, V size - 1)” to “(H size, V size)”
- section 12.2.1 Picture-in-Picture Window Setting - in figure 12-5 Picture-in-Picture Window Setting, correct typos - change “Strat” to “Start”, “(0, 0)” to “(1, 1)”, and “(H size - 1, V size - 1)” to “(H size, V size)”
- section 13.2 SDRAM Connection - add this section

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway
San Jose, CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Dongcheng District,
Beijing 100005, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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