Gourav Singla #R11800214

Cache Simulator Report

The Cache simulator project demonstrates three cache mapping techniques. The first one is direct mapping. In direct mapping, the data from main memory can be stored at specific cache blocks only. That block can be found using formula block address % num of blocks. Implementation of single level cache has already been given to students. The analysis of three parts of project is explained below:-

NOTE: To run the program, please see steps in README.txt file. Also, please see the results folder for all the outcomes of different trace files.

Part 1. Direct-mapped cache

1.

Cache Hits	1301327
Cache Misses	198673
Total Access	1500000
Cache Hit rate	0.867551
Cache miss rate	0.132449

2. Please see the “**results”** folder for result of all trace files.

Part 2. Fully associative and n-way set associative cache

Fully associative worked better than direct mapping. Because in direct mapping the block number is fixed by a formula. While in fully associative the block number is not fixed. The data can go in any of blocks in cache blocks. Here is the fully-associative result for block size of **16 Byte.**

Cache Hits	1325236
Cache Misses	174764
Total Access	1500000
Cache Hit rate	0.883491

Cache miss rate	0.116509

In Fully associative, if we increase the block size or cache line size, the hit rate improves and miss rate reduces. Here is the fully-associative result for block size of **128 Byte.**

Cache Hits	1369996
Cache Misses	130004
Total Access	1500000
Cache Hit rate	0.913331
Cache miss rate	0.086669

N-Way Mapping also performed better than direct mapping. With settings of way size 8, cache size 32 KB and cache line size of 16 Byte, following result is recorded.

Cache Hits	9516250
Cache Misses	305024
Total Access	9821274
Cache Hit rate	0.968943
Cache miss rate	0.031057

If we set the way size of 1, the result is same as direct mapping. Becuase direct mapping and way size 1 is same.

Part 3. Two-level cache simulation

If we add two caches instead of single, the miss rate reduces and also hit rate increases. Because, we have one more cache with more blocks. If data or word is missed in first cache(closer to CPU), we can try to find in second cache and hence actual miss rate (L2 miss rate) reduces.
Here is the **direct - mapping** two level result.

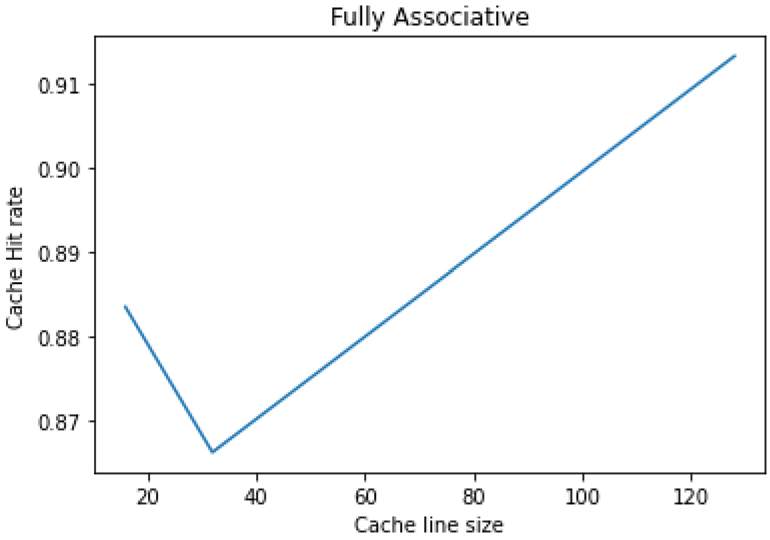
L2 global miss rate	0.102498

L2 local miss rate	0.110015
L2 global hit rate	0.897502
L2 local hit rate	0.889985

We can see, in direct single mapping we got 0.132449 miss rate, while with two-level direct mapping, we got lesser miss rate 0.110015. **For n-way two-level also, the result is same recorded.**

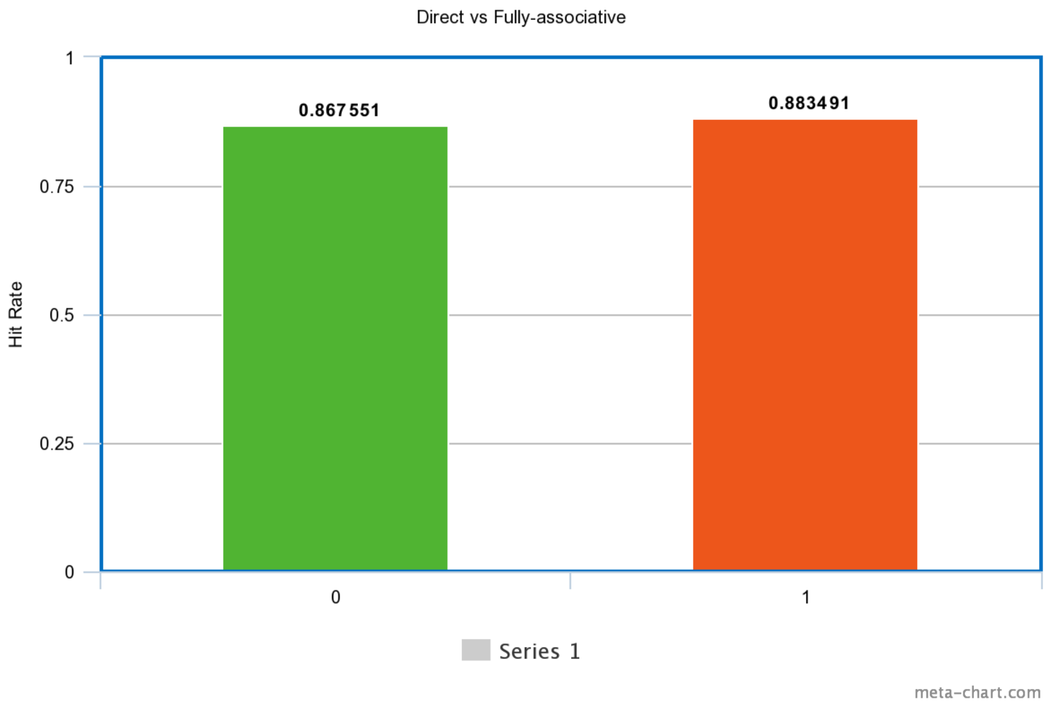
Graph analysis of different mappings with different configurations

Fully Associative - With increase in **cache line size**, the hit rate also increased.



Hit rate - It also increases with increase in **cache size.**

Here is comparison of Hit rates of **direct** vs **fully** associative with same settings of cache. In below picture we can see orange bar which is fully-associative is little more than green (direct). So, fully-associative has better hit rate than direct.


Direct vs Fully-associative
Hit Rate
1
0.75
0.5
0.25
0
0.867551
0.883491
0
1
Series 1
meta-chart.com