# HK32F030M
# manual additions and corrections, development hints

by gbm, 02’2021

The HK32F030M documents contain some inconsistencies and false information. The goal of this document it to correct and supplement these.
Datasheet and Reference Manual in Chinese may be downloaded from HK website. This document is based on Datasheet version 1.0.13 and Reference Manual version 1.1.9.
Google translate seems to do quite a good job while translating the HK32 documents from Chinese to English.
The HK32F030M is similar (but not identical) to STM32F0 series. The pinout is compatible with ST8S003, not with STM32F030. Compared to STM32F030 it has more flexible peripheral pin mapping and single-byte programmable and erasable EEPROM, but its best feature is its price.

## Revision history

02’2021 Initial version

## RCC

The HSI clock frequency is 32 MHz. The initial clock divider value is 6, so that the clock frequency is 5.33 MHz. To change the clock frequency to 32 MHz, the following steps should be taken:

- set 1 WS (latency 2) Flash access in FLASH->ACR,
- set Flash clock divider to “div by 8” (divider field value = 7) in RCC->CFGR4,
- set RCC->CFGR to 0, setting the main clock divider to 1.

Note that values after reset specified in the original documentation are incorrect for some registers.

## GPIO

The GPIO ports are logically 8-bits wide, so there are no AFRH/AFR[1] registers. The information on GPIO registers in the manual is incorrect in many aspects and it seems to be directly copied from STM32F030 manual. The bits 31..16 of MODER are permanently zeros. The initial setting of ports after reset is analog input (not digital input, like in STM32F0) for all pins other than SWDIO, SWCLK and PA0. The initial settings for these pins are:

- PA0 – digital input with pull-up, serves as NRST input;

- PD5 – AF with pull-up, SWDIO;
- PB5 – AF with pull-down, SWCLK.

There is a Schmitt trigger option available for each GPIO pin, controlled by GPIOx->IOSR register.

# Flash and EEPROM

The content od Flash after erase is unspecified – it may read as random. It seems to be all 0s (unlike in STM32 and other micros, in which erased Flash contains all ones).

Flash page size is 128 bytes. Unlike in STM32F030 it may be programmed in 16-bit or 8-bit units.

The EEPROM is a byte-programmable and byte-erasable Flash. A new register, ECR supports EEPROM byte erase and programming and main Flash byte programming.

# Pinout

NRST is PA0, regardless of number of pins available in the package (including TSSOP20). There is no real VCAP pin, the pin marked as such is simply PD7 with no VCAP function (also for TSSOP20).

The older batches of HK32F030M have a pinout different from the current ones. In these older chips NRST does not provide PA0 function in TSSOP20 and in SO8 pins 6 and 7 are swapped.

# HK32F030M support pack for Keil MDK-ARM

The pack may be downloaded from the vendor's website.

The files hk32f030m_conf.h and hk32f030m_def.h, referenced by hk32f030m.h are missing. The replacements for these may be downloaded from my HK32F030M github section.

The vendor's .pdsc file is incorrect and does not allow for creation of working Keil MDK-ARM projects. A replacement file is also available from github. After installing the pack, replace the original .pdsc file with the corrected one. Under Windows, it's usually stored in the user's Appdata\Local|\Arm\Packs\HKMicroChip folder.

# Debugging and programming

Segger J-Link may be used for debugging programming. There is no vendor-specific support for HK chips, but  setting the chip type to generic M0 works.