Graphic Era HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sanshya 12 of 2011)
University under section 2(f) of UGC Act, 1956

Term Evaluation (Odd) Semester Examination September 2025

Roll no. 2294038

Name of the Course: B.Tech
Semester: VII
Name of the Paper: Advanced Computer Architecture
Paper Code: TCS 704
Time: 1.5 hour **Maximum Marks: 50**

Note:
(i) Answer all the questions by choosing any one of the sub-questions
(ii) Each question carries 10 marks.

Q1. (10 Marks)
a. CO3

A CPU runs at 2 GHz with a CPI of 2 and executes a program with 10^{9} instructions.

I. Calculate execution time.
II. If the clock speed is doubled to 4 GHz but CPI remains the same, calculate the new execution time.
III. Now assume 30% of the instructions suffer a memory stall of 50 ns (unchanged with faster clock). Recalculate the execution time and compare.
IV. Why is the expected performance gain not achieved? Relate this to the Myopic View of Computer Architecture.

OR

b. CO3

A CPU has a two-level cache hierarchy:

- L1 cache hit time = 1 ns, hit rate = 90%
- L2 cache hit time = 10 ns, hit rate = 95% (for remaining 10%)

Main memory access time = 100 ns
(i) Calculate the average memory access time(AMAT). (ii) If L1 hit rate improves to 95%, recalculate AMAT. Comment on the performance improvement.

Q2. (10 Marks) CO1
a. Differentiate between temporal locality and spatial locality. Illustrate each with an example. For a loop that repeatedly accesses A[5], explain how temporal locality helps.

OR

b. CO1

What is Amdahl's Law? A program spends 40% of its time in a parallelizable section. Using Amdahl's Law:

I. Calculate speedup for 4 processors.
II. Calculate speedup for 8 processors.

Term Evaluation (Odd) Semester Examination September 2025

III. Comment on diminishing returns.

Q3. (10 Marks)
a. CO2

Classify parallel computers. For each type, give a numerical example:

- If a task of size 1000 operations is executed, estimate execution time assuming each architecture processes operations at different parallelism levels (you may assume SISD = serial, SIMD = 4 ops/cycle, MISD = redundant execution, MIMD = 4 processors).

OR

b. CO2, CO3

A dual-core system shares a cache. One core writes a value X = 5 into cache, while the other core reads X from memory as 3.

I. Explain the cache coherence problem.
II. Illustrate with an example how the MESI protocol (or any one protocol) solves this issue.

Q4. (10 Marks)
a. CO1

Moore's Law states transistor count doubles approximately every 18–24 months.

I. If a processor had 1 million transistors in 1980, estimate transistor count in 2000.
II. Discuss why physical scaling has slowed in modern era and its implications.

OR

b. CO2

Compare direct-mapped, fully associative, and set-associative cache organizations.

If you have 16 blocks of main memory and 4 cache lines, show how block 6 would be placed in each organization.

Q5. (10 Marks)
a. CO1

Term Evaluation (Odd) Semester Examination September 2025

Define dependability in computer architecture.

I. If a system has MTBF = 200 hours and MTTR = 2 hours, calculate availability.

Discuss how energy, power, and cost constraints affect system dependability.

OR

b. CO3

Explain the principle of Virtual Memory.

I. A system has 32-bit virtual addresses and 4 KB page size. Calculate:
   a. Number of pages in virtual address space.
   b. Number of offset bits.

II. Explain how paging helps efficient memory utilization.