Graphic Era
HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sankhya 12 of 2011)
University under section 2(f) of UGC Act, 1956

End Term (Even) Semester Examination May-June 2025

Roll no.....

Name of the Program and semester:
Name of the Course: CMOS Design
Course Code: TEC 611
Time: 3 hour

Maximum Marks: 100

Note:

(i) All the questions are compulsory.
(ii) Answer any two sub questions from a, b and c in each main question.
(iii) Total marks for each question is 20 (twenty).
(iv) Each sub-question carries 10 marks.

Q1. (2X10=20 Marks) CO1

a. Explain the difference between Dry Oxidation and wet Oxidation, and what are the applications of oxidations in VLSI.
b. Explain the process of creation n-well in MOS.
c. What is twin tub and Latch up explain in brief.

Q2. (2X10=20 Marks) CO2

a. Design the stick diagram of Y = (AB+E+CD)'
b. Explain in detail about Lambda (λ) based layout design rules.
c. Draw the Layout of Boolean expression Y = (AB+C)'

Q3. (2X10=20 Marks) CO3

a. Implement the Boolean expression Y = {AB(C+D) + (E+F)G}' using CMOS.
b. Derive the expression of saturation current in MOS device.
c. The slope of the I_D *vs* .V_{GS} curve of an n – channel MOSFET in linear region is $10^{-3}\ \Omega^{-1}$ at V_{DS}=0.1V . For the same device, neglecting channel length modulation, find the slope of the $\sqrt{I_D}$ *vs* V_{GS} curve ($in\ \sqrt{A}V$) under saturation region.

Q4. (2X10=20 Marks) CO4

a. Explain the working principles of the following memory and logic technologies:
   (i) Anti-fuse
   (ii) EPROM
   (iii) SRAM
b. What are programmable logic cells? Briefly discuss their role in the implementation of complex logic functions.
c. Define programmable inversion and expander logic in the context of programmable logic arrays or FPGAs. Explain how they contribute to logic optimization.

Q5. (2X10=20 Marks) CO5

a. Explain the internal architecture and programming technologies of Field Programmable Gate Arrays (FPGAs).
b. What do you understand by programmable I/O blocks in FPGA?
c. What are the dedicated specialized components of FPGA, and the applications of FPGA?