Graphic Era HILL UNIVERSITY

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End Term (Odd) Semester Examination December 2024

Roll no.............................

Name of the Course and semester: BTECH CSE 7th SEM

Name of the Paper: Advanced Computer Architecture
Paper Code: TCS 704

Time: 3 hours | Maximum Marks: 100

Note:

(i) All the questions are compulsory.
(ii) Answer any two sub questions from a, b and c in each main question.
(iii) Total marks for each question is 20 (twenty).
(iv) Each sub-question carries 10 marks.

Q1. (2X10=20 Marks)

a. Analyze the implications of Amdahl's Law in the optimization of parallel systems. How does it influence design decisions for high-performance computing? (CO4)

b. Moore's Law has been a driving force in computer architecture. Discuss its current relevance and challenges. Predict its role in the next decade with supporting arguments. (CO3)

c. A processor is tested using two benchmark standards: Benchmark A (measures integer performance) and Benchmark B (measures floating-point performance). The results are as follows:

Benchmark A: 1.5× speed improvement compared to a previous generation.

Benchmark B: 2.0× speed improvement compared to the same previous generation.

Analyze the processor's performance based on these benchmarks and discuss the reliability of these metrics in performance evaluation. (CO4)

Q2. (2X10=20 Marks)

a. Explain the memory hierarchy of a modern computer system, highlighting its different levels and characteristics. (CO1)

b. A CPU has a 32-bit address space and a cache that uses a block size of 16 bytes. Calculate the number of cache blocks for a direct-mapped cache with a size of 64 KB. Describe the address breakdown into tag, index, and block offset. (CO1)

c. Discuss various techniques for fast address translation in virtual memory systems. Explain how these techniques affect system performance. (CO2)

Q3. (2X10=20 Marks)

a. Explain the design principles of a RISC ISA and how they support efficient pipelining. Compare RISC and CISC architectures in terms of pipelining performance. (CO1)

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b. Processor has a five-stage pipeline (Fetch, Decode, Execute, Memory, Write-back). (CO4)

- Assume the following instructions are executed sequentially:
  - Instruction 1: Load R1, 100(R2)
  - Instruction 2: Add R3, R1, R4
  - Instruction 3: Store R3, 200(R2)
- Identify any potential hazards that may occur during execution.
- Suggest ways to resolve the identified hazards to ensure efficient pipeline operation.

c. Describe pipelining in computer architecture. Describe the five stages of the classic RISC pipeline, explaining the purpose of each stage. (CO1)

Q4. (2X10=20 Marks)

a. Discuss the concept of hierarchical branch predictors. How do multi-level predictors, such as the global-local predictor, work to improve prediction accuracy? Compare and contrast hierarchical predictors with single-level predictors in terms of design complexity and performance. (CO2)

b. Identify and describe the types of data dependencies that limit ILP. How can compiler techniques and processor mechanisms mitigate these dependencies to maximize parallelism? (CO4)

c. A program contains 5,000 branch instructions, of which 1,000 are simple conditional branches. Replacing the conditional branches with conditional move instructions eliminates the branch penalty (3 cycles). Calculate the total cycle savings if each branch misprediction occurs 10% of the time. (CO3)

Q5. (2X10=20 Marks)

a. Elaborate on the structure and working of distributed shared-memory architecture. Compare it with centralized shared-memory systems. (CO2)

b. Compare the performance of message-passing systems and shared-memory systems for solving a **matrix** multiplication problem involving large datasets. Illustrate with suitable examples and calculations. (CO4)

c. A message-passing system has: (CO3)

- Bandwidth = 200 MB/s.
- Total data transfer = 10 GB.
- Network latency = 5 ms.

Calculate the total time required to transfer the data.