Graphic Era
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Mid Term (Odd) Semester Examination October 2024

Roll no.....

Name of the Course and semester: B.Tech CSE VIIth Semester
Name of the Paper: Advanced Computer Architecture
Paper Code: TCS-704
Time: 1.5 hour Maximum Marks: 50

Note:
(i) Answer all the questions by choosing any one of the sub questions
(ii) Each question carries 10 marks.

Q1. (10 Marks)
a. How does Amdahl's Law limit the potential speedup of a parallelized program? (CO 1)

OR

b. What are the trade-offs between CISC (Complex Instruction Set Computing) and RISC (Reduced Instruction Set Computing) architectures? (CO 3)

Q2. (10 Marks)
a. How does the memory hierarchy take advantage of the different speeds of various memory types to optimize performance? (CO 2)

OR

b. How has the slowing down of Moore's Law impacted processor design and performance improvements? (CO 1)

Q3. (10 Marks)
a. What are the principles of temporal and spatial locality, and how do they influence memory hierarchy design? (CO 2)

OR

b. Explain the process of page table lookup and how multi-level page tables help optimize memory management. (CO 2)

Q4. (10 Marks)
a. How does set-associative cache organization balance the trade-offs between speed and complexity? A processor has a cache with a **hit rate** of 90%. The time to access data from the cache is 10 ns, and the time to access data from the main memory (on a miss) is 100 ns. What is the average memory access time? (CO 2)

OR

b. In a system, the Effective Memory Access Time (EMAT) is measured to be 105 cycles. (CO 2)
The system has:
TLB Access Time: 2 cycles, **Memory Access Time:** 80 cycles, **Page Table Access Time:** 80 cycles
Calculate the **TLB Hit Rate.**

Q5. (10 Marks)
a. How does Data-Level Parallelism (DLP) differ from ILP, and what types of workloads benefit from DLP? (CO 2)

OR

b. What are the key components of modern computer architecture, and how do they interact? (CO 1)