Graphic Era
HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sankhya 12 of 2011)
University under section 2(f) of UGC Act, 1956

Term Evaluation (Odd) Semester Examination September 2025

Roll no. [redacted]

Name of the Course: B.Tech(CSE)
Semester: III[rd]
Name of the Paper: Logic Design & Computer Organization
Paper Code: TCS 308
Time: 1.5 hour

Maximum Marks: 50

Note:
(i) Answer all the questions by choosing any one of the sub-questions
(ii) Each question carries 10 marks.

Q1. (10 Marks)
a. Minimize the 5-variable function F(A,B,C,D,E)=Σm(1,3,7,11,15,16,17,19,23,27,31) + d=Σm(2,6,10,14) using K-maps. (CO1)

OR

b. Design a 4 bit binary adder- subtractor. (CO1)

Q2. (10 Marks)
a. Realize the function F(A,B,C) = $AB + \bar{C}$ using NAND and NOR gates. (CO1)

OR

b. Design the Boolean expression F(A,B,C)=Σm(1,3,6,7) by using 4X1 MUX and 2X1MUX. (CO1)

Q3. (10 Marks)
a. *Implement 2bit X 2bit binary Multiplier.* (CO1)

OR

b. Using a 3×8 decoder, implement the two functions: F1(A,B,C)=Σm(1,2,5,7) and F2(A,B,C)=Σm(0,3,4,6). (CO1)

Q4. (10 Marks)
a. Explain the difference between a) Latch and Flip flop b) combinational and sequential circuits. (CO2)

OR

b. Design a T flip-flop using a JK flip-flop. Derive the logic equation and draw the circuit diagram. (CO2)

Q5. (10 Marks)
a. Derive the characteristic equation and truth table of a D flip-flop. Show how it avoids the invalid state of an SR flip-flop. (CO2)

OR

b. Derive the characteristic equations of SR, JK, D, and T flip-flops from their truth tables. (CO2)