Graphic Era HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sankhya 12 of 2011)
University under section 2(f) of UGC Act, 1956

Term Evaluation (Even) Semester Examination March 2025

Roll no.....

Name of the Course: B Tech
Semester: 6
Name of the Paper: CMOS Design
Paper Code: TEC 611
Time: 1.5 hour **Maximum Marks: 50**

Note:
(i) Answer all the questions by choosing any one of the sub-questions
(ii) Each question carries 10 marks.

Q1. (10 Marks)

a. What is the difference between NMOS and CMOS fabrication processes? Explain the key steps involved in fabricating each type of transistor.

OR

b. What causes latch-up in CMOS circuits, and what techniques can be employed during fabrication to prevent latch-up?

Q2. (10 Marks)

a. Compare and contrast the fabrication of CMOS and BiCMOS circuits. What are the benefits of integrating both bipolar and CMOS transistors in BiCMOS technology?

OR

b. Describe the twin-tub process in CMOS technology. What are its advantages over the traditional n-well or p-well processes?

Q3. (10 Marks)

a. Explain the significance of design rules in IC layout design. What are the key design rules that must be followed during CMOS layout fabrication?

OR

b. What is a stick diagram, and how is it used in the CMOS layout design process? Provide an example of a stick diagram for a simple logic gate.

Q4. (10 Marks)

a. Design the layout for a CMOS NAND gate? Describe the arrangement of NMOS and PMOS transistors and their connections to verify the truth table.

OR

b. Discuss the parasitic effects in CMOS layout design. How do parasitic capacitance, resistance, and inductance affect the performance of an integrated circuit?

Q5. (10 Marks)

a. What is the significance of layout design prospects, such as advanced lithography, 3D ICs, and AI-driven design tools, in the future of semiconductor manufacturing?

OR

b. Explain the fabrication process of an NMOS transistor. How does it differ from the CMOS fabrication process in terms of substrate and transistor formation?