



End Term (Even) Semester Examination May-June 2025

Roll no.....

Name of the Program and semester: B-Tech ECE, VI Semester

Name of the Course: Digital Signal Processing

Course Code: TEC-602

Time: 3 hour

Maximum Marks: 100

Note:

- (i) All the questions are compulsory.
- (ii) Answer any two sub questions from a, b and c in each main question.
- (iii) Total marks for each question is 20 (twenty).
- (iv) Each sub-question carries 10 marks.

Q1.

CO1 (2X10=20 Marks)

- a. Explain the methods for efficient computation of the DFT of 2N-Point real sequences.
- b. Differentiate between DTFS & DTFT based on few important properties.
- c. Find the 8-point DFT of the sequence $x(n) = \cos(n\pi/4)$.

Q2.

CO2 (2X10=20 Marks)

- a. Determine the IDFT of $X(k) = \{1, (1 + j), 2, (2 - j)\}$.
- b. Given $x(n) = \{0, 1, 2, 3, 4, 5, 6, 7\}$, find $X(k)$ using DIT FFT algorithm
- c. Given $x(n) = 2^n$ and $N = 4$, find $X(k)$ using DIT FFT algorithm.

Q3.

CO3 (2X10=20 Marks)

- a. Compare direct form-I and direct form-II realization of a third-order IIR filter. Which among the two is canonic and why ?
- b. Obtain a cascade realization of the system characterized by the transfer function.

$$H(z) = \frac{2z^{-3}(1+2z^{-1})}{(1-0.1z^{-1})(1+0.5z^{-1})(1+0.4z^{-1})}$$

- c. Determine the parallel realization of the IIR digital filter transfer function:

$$H(z) = \frac{3z(5z-2)}{(z+\frac{1}{2})(3z-1)}$$

Q4.

CO4 (2X10=20 Marks)

- a. Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation. Assume $T = 1$ s.

$$\begin{array}{ll} 0.9 \leq |H(e^{j\omega})| \leq 1 & 0 \leq \omega \leq \pi/2 \\ |H(e^{j\omega})| \leq 0.2 & 3\pi/4 \leq \omega \leq \pi \end{array}$$

- b. Explain any two most efficient windowing techniques for FIR filter design.

- c. Determine $H(z)$ using the impulse invariant technique for the analog system



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Function:

$$H(s) = \frac{1}{(s + 0.5)(s^2 + 0.5s + 2)}$$

Q5.

CO5 (2X10=20 Marks)

- a. Discuss multi rate signal processing and its applications.
- b. What are the advantages of DSP processors in relation to general-purpose processors?.
- c. Draw the schematic block diagram of the TMS320C5X processor architecture and explains the major blocks.