Graphic Era
HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sankhya 12 of 2011)
University under section 2(f) of UGC Act, 1956

End Term (Odd) Semester Examination November 2025

Roll no.............................

Name of the Course and semester: B.Tech IIIrd sem
Name of the Paper: Digital System Design
Paper Code: TEC 302
Time: 3 hour — Maximum Marks: 100

Note:
- *(i)* All the questions are compulsory.
- *(ii)* Answer any two sub questions from a, b and c in each main question.
- *(iii)* Total marks for each question is 20 (twenty).
- *(iv)* Each sub-question carries 10 marks.

Q1. (2X10=20 Marks)

a. Explain the concept of signed binary numbers. Perform the following operations and show all steps: $(-35)_{10} + (27)_{10}$, using 8-bit 2's complement arithmetic. (CO1)

b. Convert the following in required base (CO1)
$(56)_8 = (\_\_\_\_\_)_5 = (\_\_\_\_)_{16}$

c. Write short notes on: (i) Binary Codes (ii) Error detection using parity bit. (CO1)

Q2. (2X10=20 Marks)

a. Minimize the Boolean function $F(A,B,C,D,E) = \Sigma(0,2,4,8,9,10,12,13,15,19,21,23,25,27,29,31)$ using a 5-variable K-map. (CO2)

b. Explain Boolean theorems and postulates. Prove DeMorgan's theorems. (CO2)

c. Simplify the Boolean function $F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10,13)$ using Quine Mccluskey method. (CO2)

Q3. (2X10=20 Marks)

a. Draw and explain circuit of Decimal adder. (CO3)

b. Design a 4:16 decoder using 2:4 decoders. (CO3)

c. Implement Full adder using Demultiplexer. (CO3)

Q4. (2X10=20 Marks)

a. Explain operation of SISO shift register. (CO4)

b. Design a MOD-5 Asynchronous counter. (CO4)

c. Convert JK Flip Flop into D Flip Flop. (CO4)

Q5. (2X10=20 Marks)

a. Explain Verilog modeling styles and data types with examples. (CO5)

b. Write Verilog code for 4×1 multiplexer using case statement. (CO5)

c. Write Verilog code to model a 4-bit adder. (CO5)