



**End Term (Odd) Semester Examination November 2025**

Roll no. 2294038

Name of the Course and semester: B.Tech 7th sem  
Name of the Paper: Advanced Computer Architecture  
Paper Code: TCS 404  
Time: 3 hour

Maximum Marks: 100

**Note:**

- (i) All the questions are compulsory.
- (ii) Answer any two sub questions from a, b and c in each main question.
- (iii) Total marks for each question is 20 (twenty).
- (iv) Each sub-question carries 10 marks.

**Q1.** (2X10=20 Marks)

- a. Explain Moore's Law. Discuss how technology scaling has influenced processor performance, power consumption, and fabrication yield over the last two decades. (CO1)
- b. What is the Iron Law of Performance? Using a numerical example, show how CPI, Instruction Count, and Clock Cycle Time determine system performance. (CO3)
- c. A company plans to upgrade from a single-core processor to a multi-core processor for its data analytics workload. Analyze the performance improvement using Amdahl's Law, assuming 75% parallel portion and 4 processors. Also discuss the limitations of relying solely on Amdahl's Law for real systems. (CO5, 6)

**Q2.** (2X10=20 Marks)

- a. Explain the principles of locality (temporal & spatial). How do these principles influence the design of cache memory hierarchy? (CO1)
- b. Describe different cache organizations (direct-mapped, fully associative, set associative). Compare their hit rate, access time, and complexity. (CO2)
- c. Your program suffers high cache miss rates. Recommend three cache optimization techniques (such as blocking, prefetching, write strategies, replacement strategies) and justify how each technique reduces miss penalty or miss rate. (CO5, 6)

**Q3.** (2X10=20 Marks)

- a. Explain the classic five-stage RISC pipeline with a neat diagram. Describe the role of each stage. (CO2)
- b. Discuss data hazards (RAW, WAR, WAW) and structural hazards in pipelining. Suggest methods to reduce or eliminate pipeline hazards. (CO3)
- c. Consider a pipelined CPU where branch instructions cause frequent pipeline stalls. Propose methods (such as forwarding, hazard detection, branch handling techniques) to reduce these stalls. Explain how each method improves pipeline performance. (CO6)

**Q4.** (2X10=20 Marks)

- a. What is branch prediction? Explain direction predictors and hierarchical predictors with examples. (CO1)
- b. Define Instruction Level Parallelism (ILP). Explain RAW and WAW dependencies and how compiler or hardware techniques can overcome these limitations. (CO2)
- c. Your processor frequently mispredicts conditional branches in a loop-heavy program. Discuss how if-conversion, conditional move, and advanced branch predictors can reduce mispredictions and improve performance. (CO4)

**Q5.** (2X10=20 Marks)

- a. Explain the taxonomy of parallel architectures. Compare centralized shared-memory and distributed shared-memory systems with examples. (CO5)



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- b. Discuss message-passing architecture. Compare message passing with shared-memory communication in terms of speed, programmability, and scalability. (CO1)
- c. A scientific computing application must run on a cluster. Recommend whether a distributed shared-memory or message-passing architecture is more suitable. Justify your selection considering communication overhead, cost, and scalability. (CO6)