

FLOAT TO FIXED

Using Executable Models to
Make FPGA Design Easier

Taylor L. Riché, Jim Nagle, Joyce Xu, Don Hubbard

National Instruments

WHO AM I?



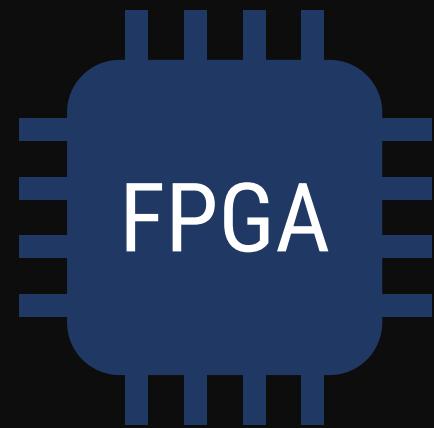
Taylor L. Riché

Principal Product Owner
National Instruments

Manager
Local Arrangements Chair MODELS 2017
Developer
Postdoc (Riché et. al, MODELS 2010)
PhD Student

GOAL:

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left(a_n \cos \frac{n\pi x}{L} + b_n \sin \frac{n\pi x}{L} \right)$$



PROBLEM: THIS IS HARD!

SOLUTION:



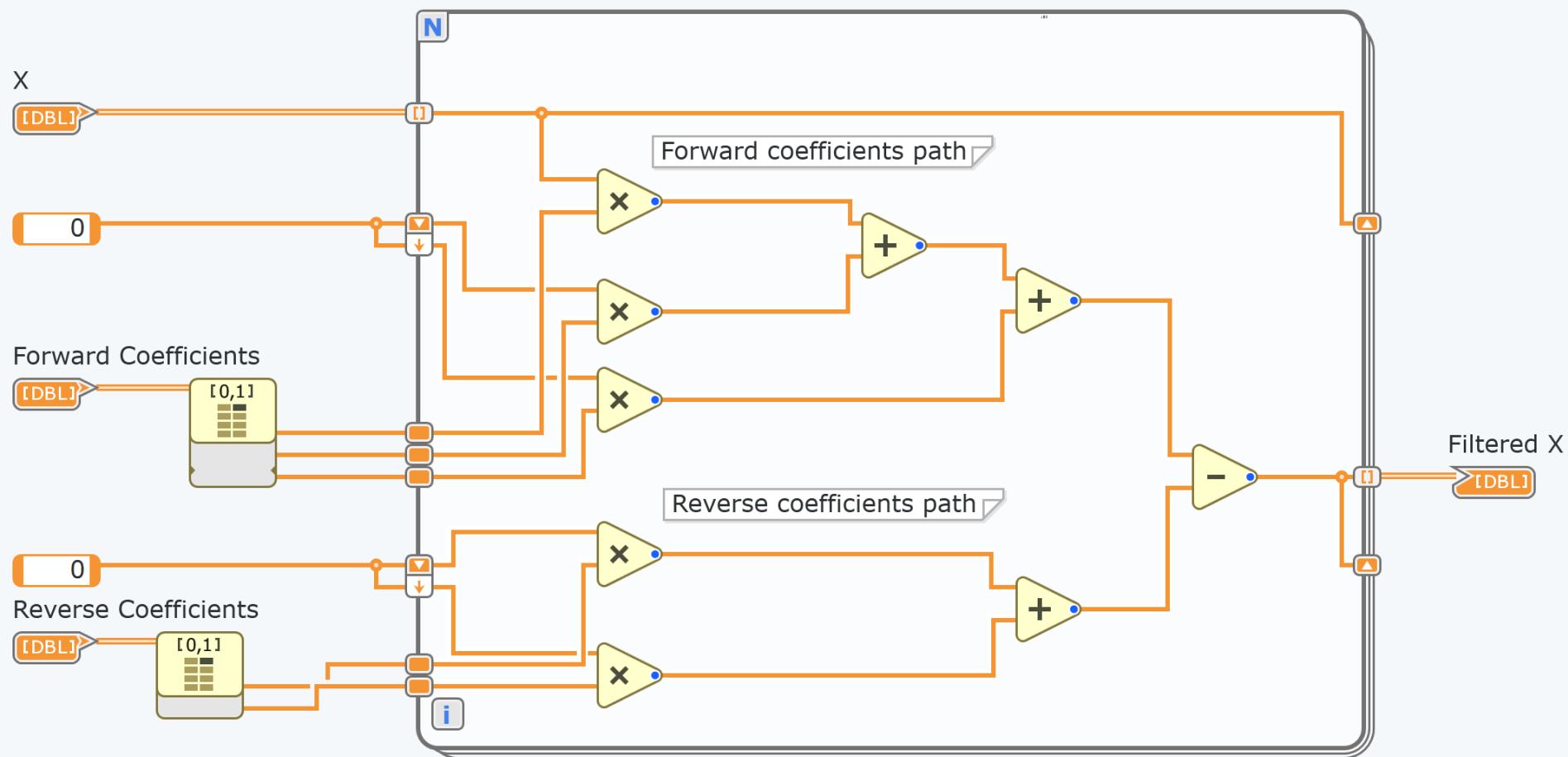
1. Have algorithm designers model their new algorithms in LabVIEW NXG
2. Use the executable nature of LabVIEW NXG to generate an initial model transform
3. Provide tools to help designers create and apply the remaining transforms
4. Along the way, executability gives constant feedback on “correct enough” by construction



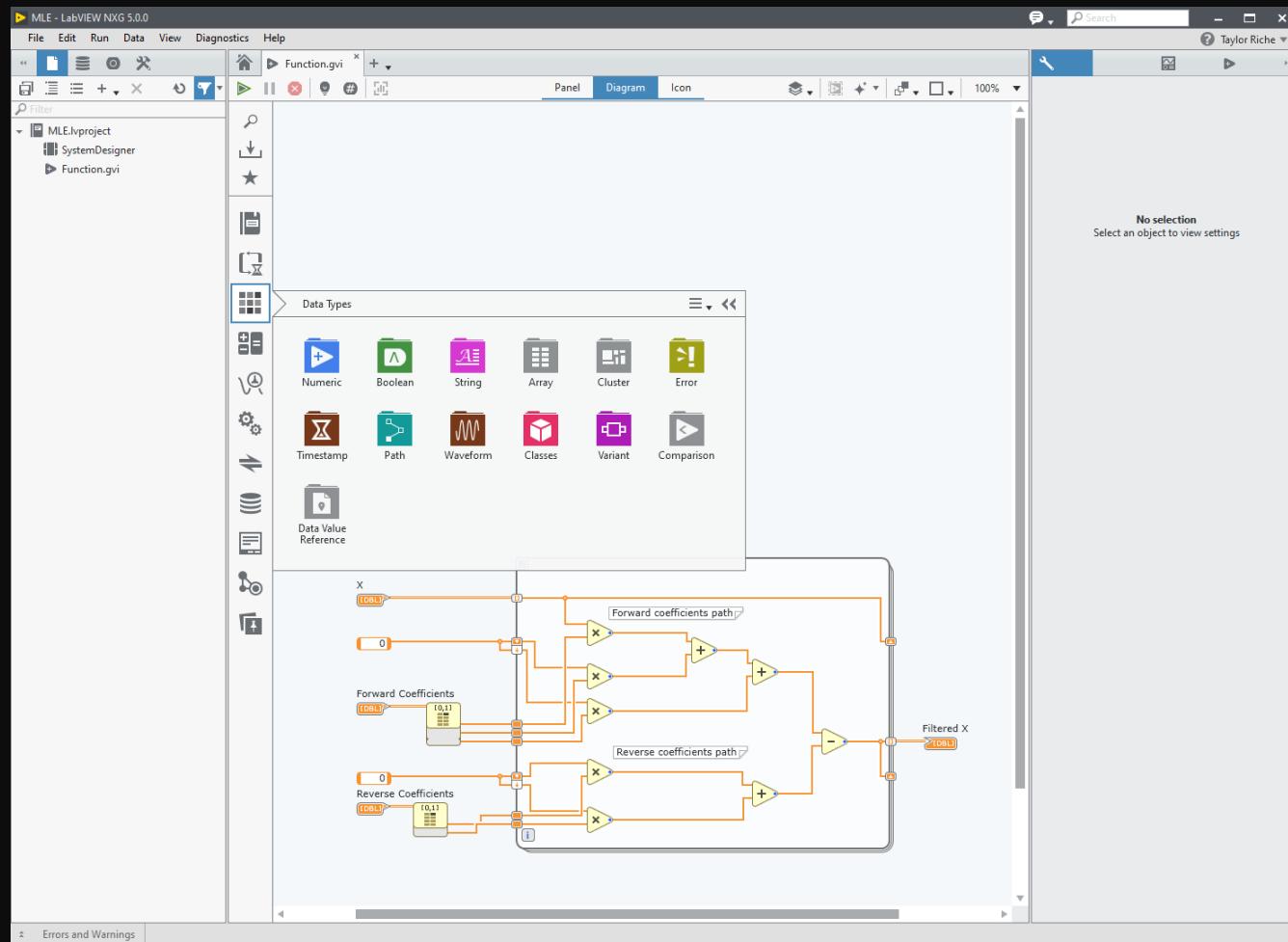


A QUICK INTRO TO G

SO THIS IS G...



AND THIS IS LABVIEW NXG...

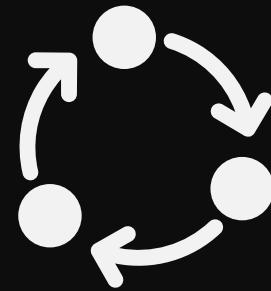


A FEW DETAILS

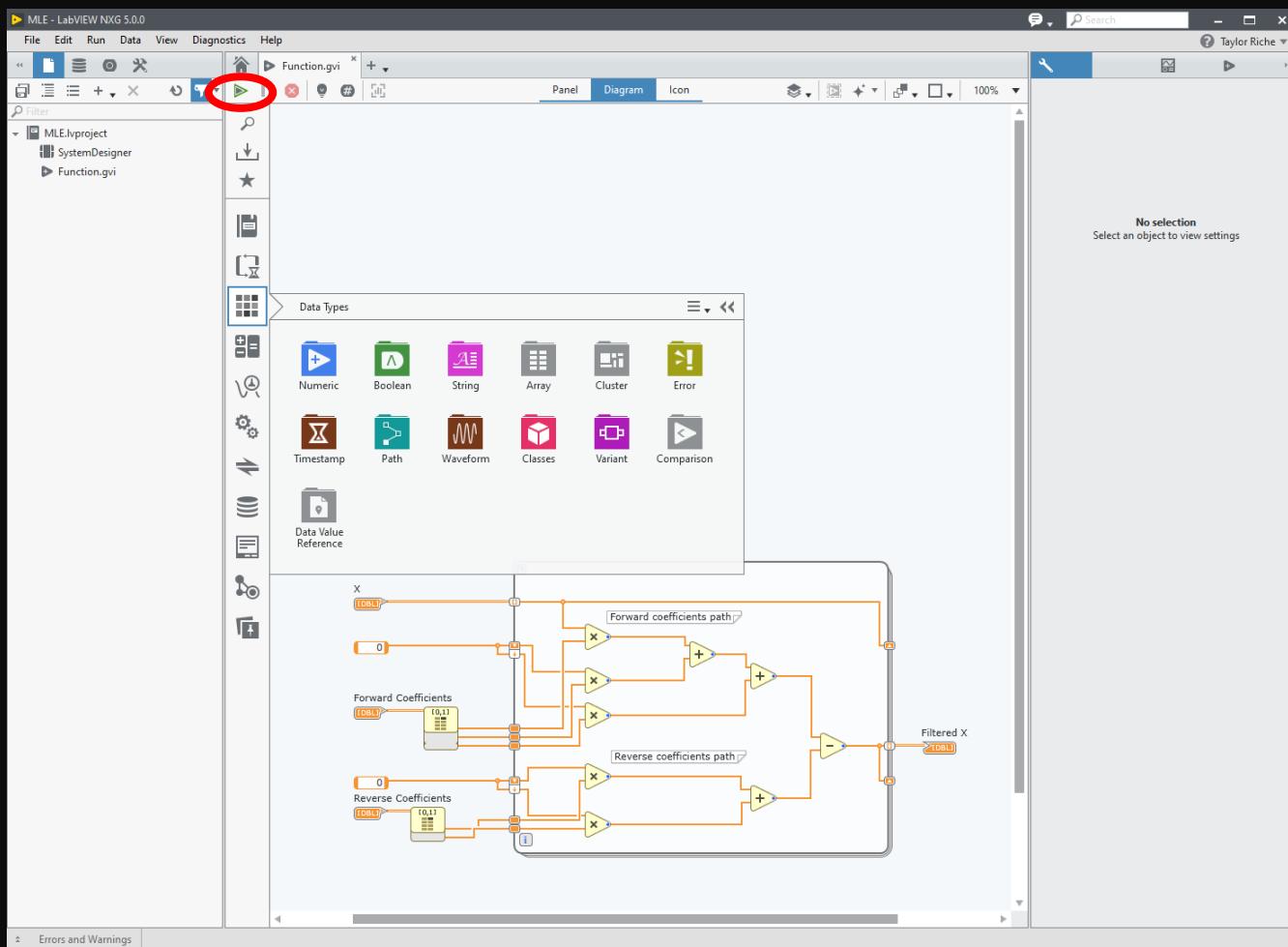
1. Graphical dataflow language
2. Test and Measurement DSL
3. Allows you to model computation
4. Allows you to model hardware configuration
5. Different libraries of mathematical tools
6. Allows creation of EXEs and reusable IP
7. Maps computation to desktop, FPGA, and Realtime

<http://www.ni.com/labviewnxg>

EXECUTABILITY

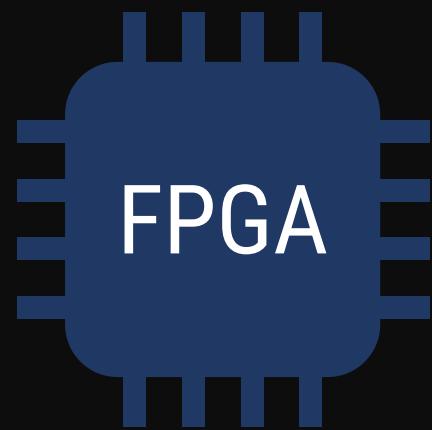


IT RUNS

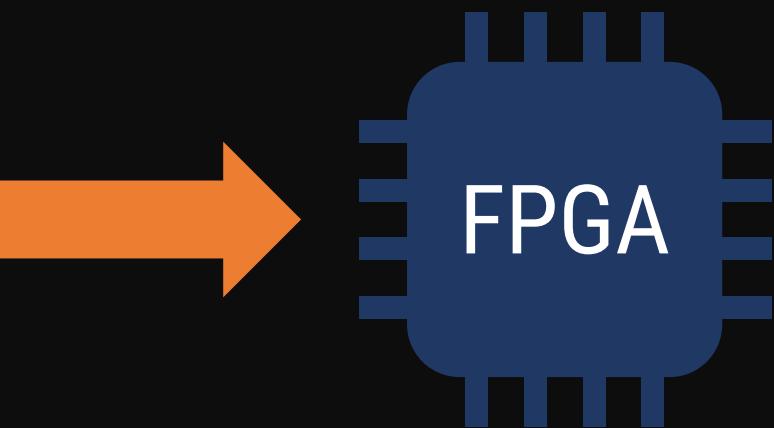
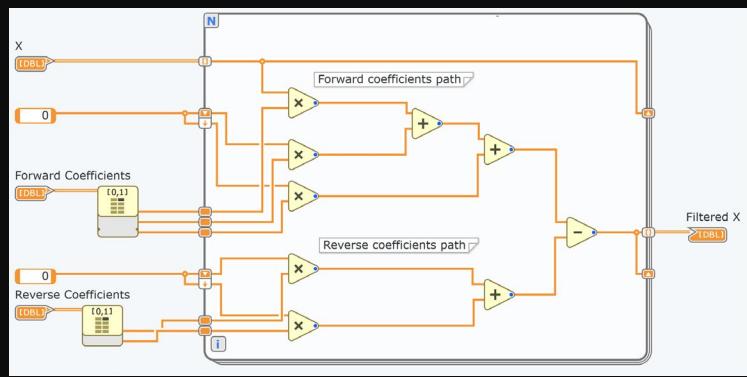


GOAL:

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left(a_n \cos \frac{n\pi x}{L} + b_n \sin \frac{n\pi x}{L} \right)$$



GOAL:



THE PROBLEM:

- Throughput constraints require HW
- FPGAs have limited resources
- Floating point takes many resources
- Digital design experts are expensive

THE RESOURCE SOLUTION: FIXED-POINT ARITHMETIC

FIXED POINT

XXXX.YYYYYYYYYYYY



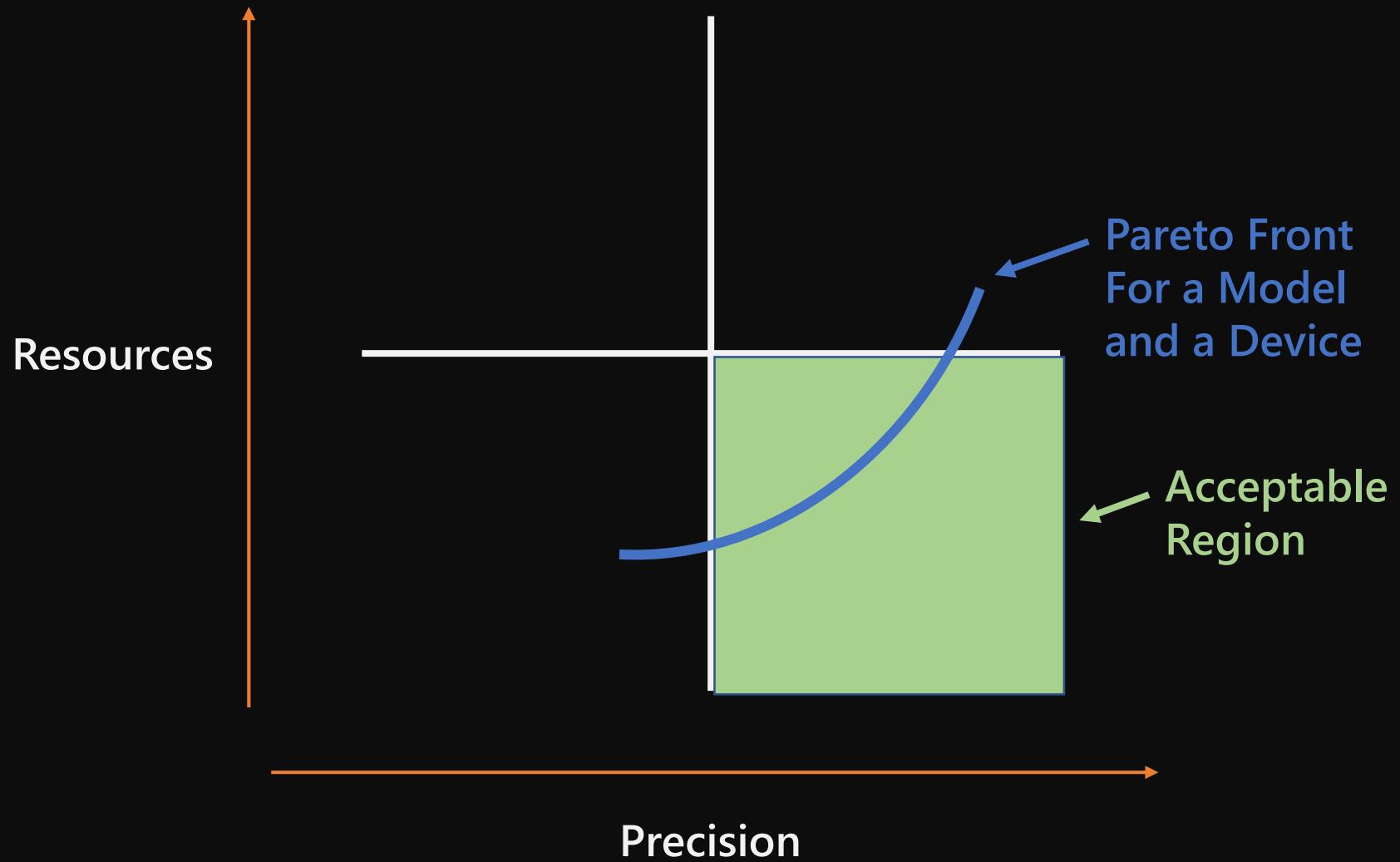
4 integer
bits

12 fractional
bits

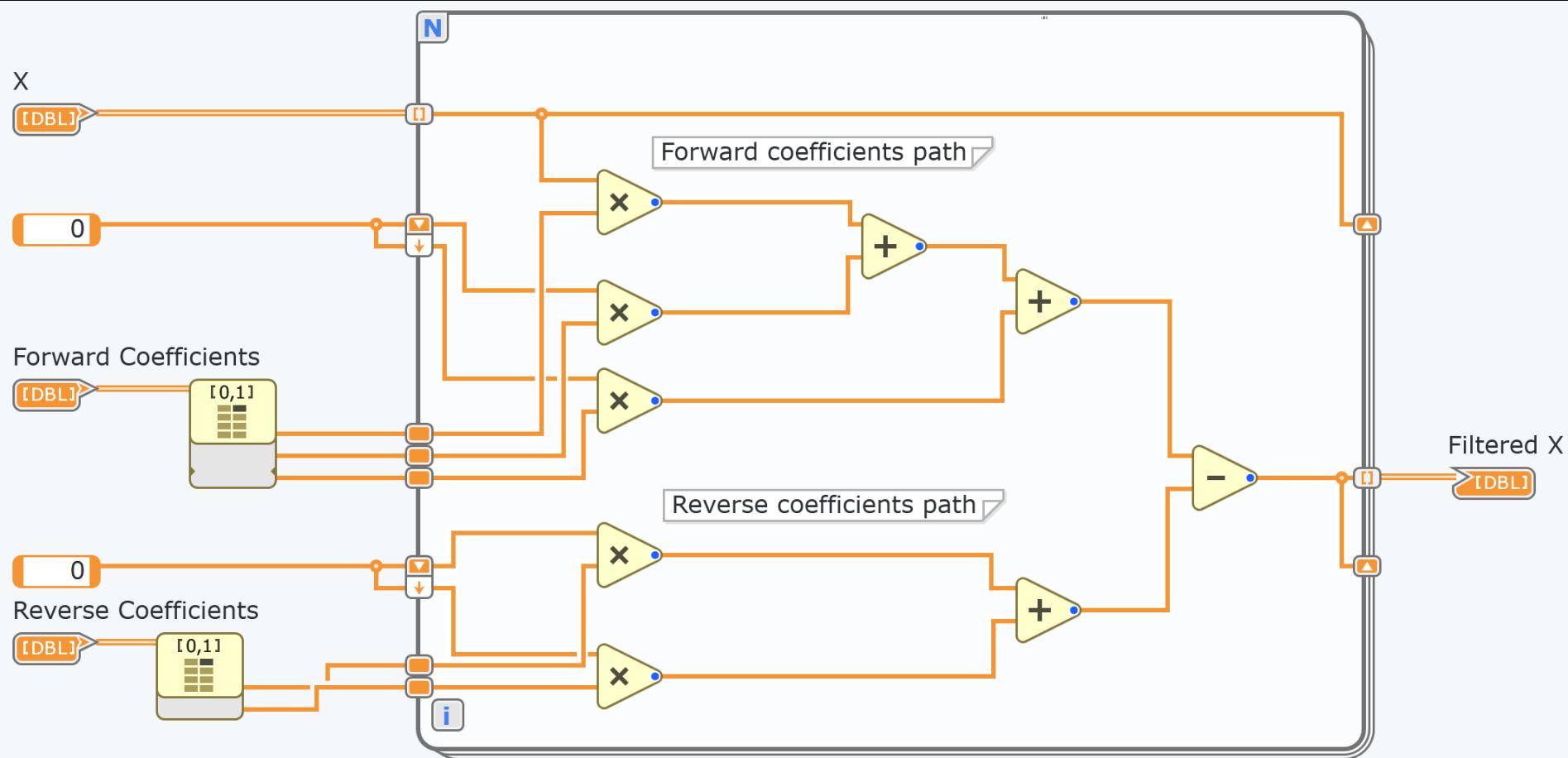
FIXED POINT CHALLENGES

- Too few integer bits → overflow
- Too few fractional bits → loss of precision
- More bits use more FPGA resources

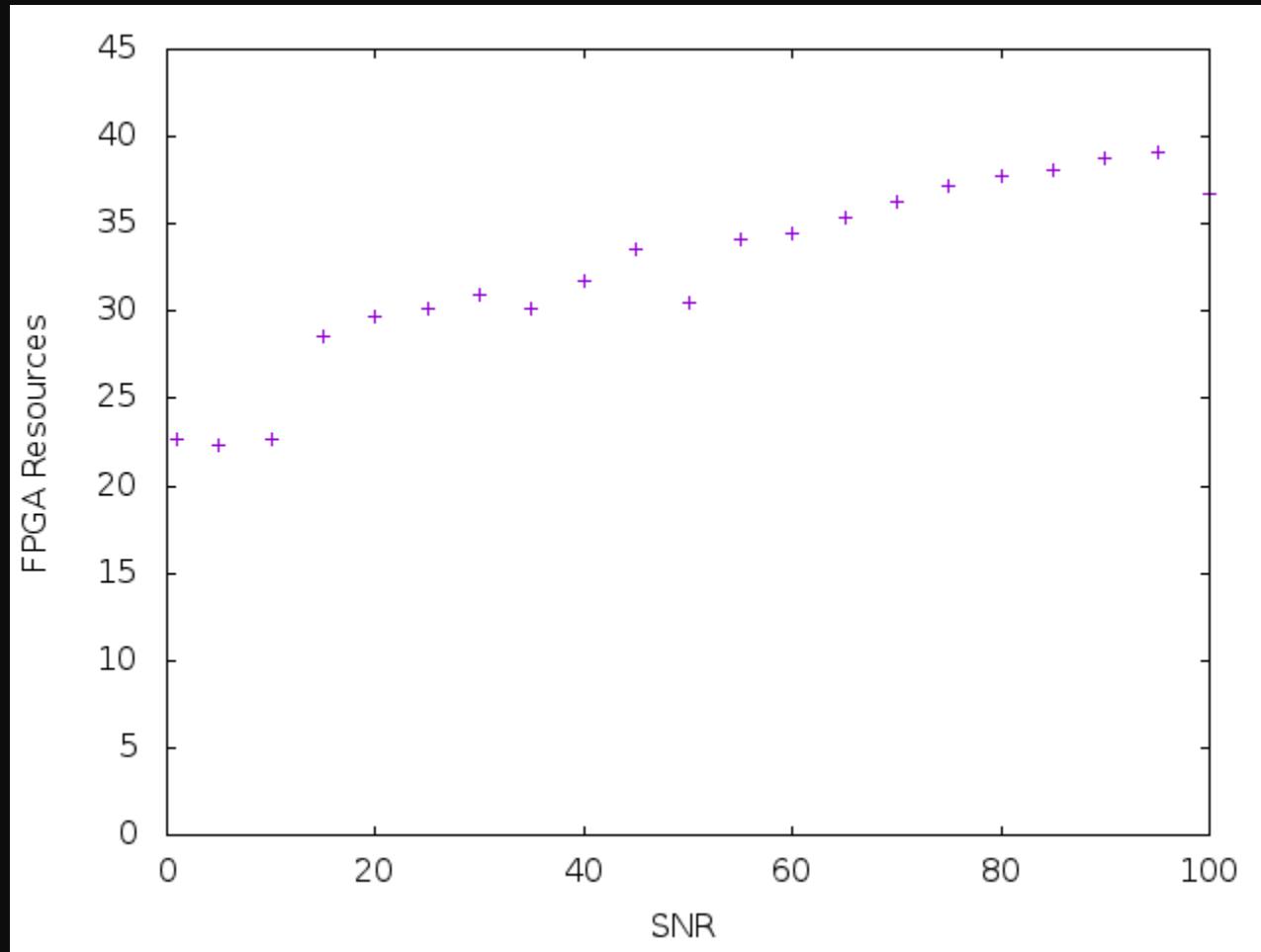
RESOURCES V. PRECISION



RESOURCE EXAMPLE



RESOURCE EXAMPLE



OUR SOLUTION: LABVIEW NXG F2F

DESIGN TENANTS:

- Not trying to make the best F2F tool
- Usability was paramount
 - Don't hire a FXP or DD expert
 - No spreadsheets!
- Don't try to encode all constraints
 - Focus on Signal-to-Noise Ratio (SNR)
- Perfect is the enemy of shipping

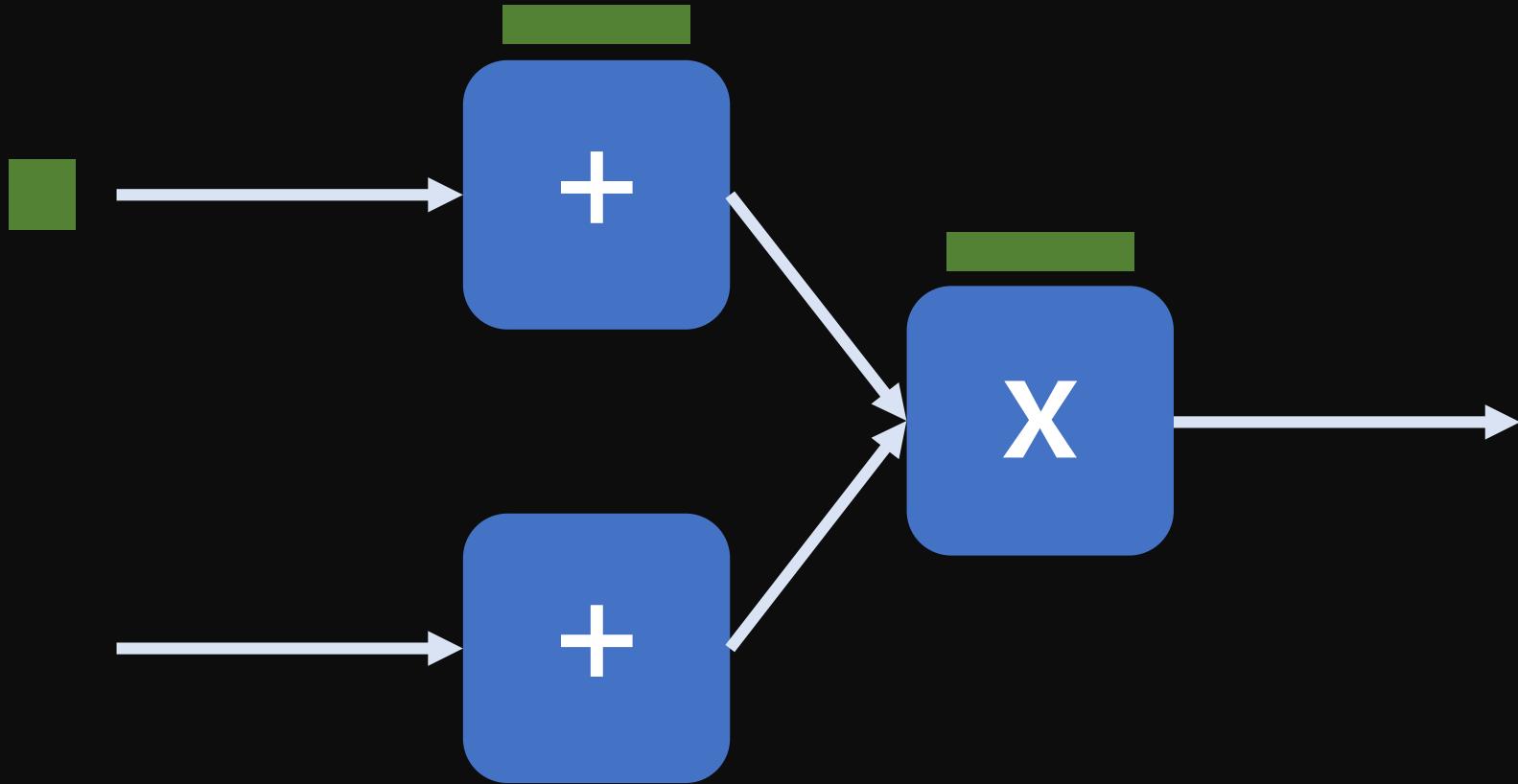
BUT FIRST, SOME FORMALISMS

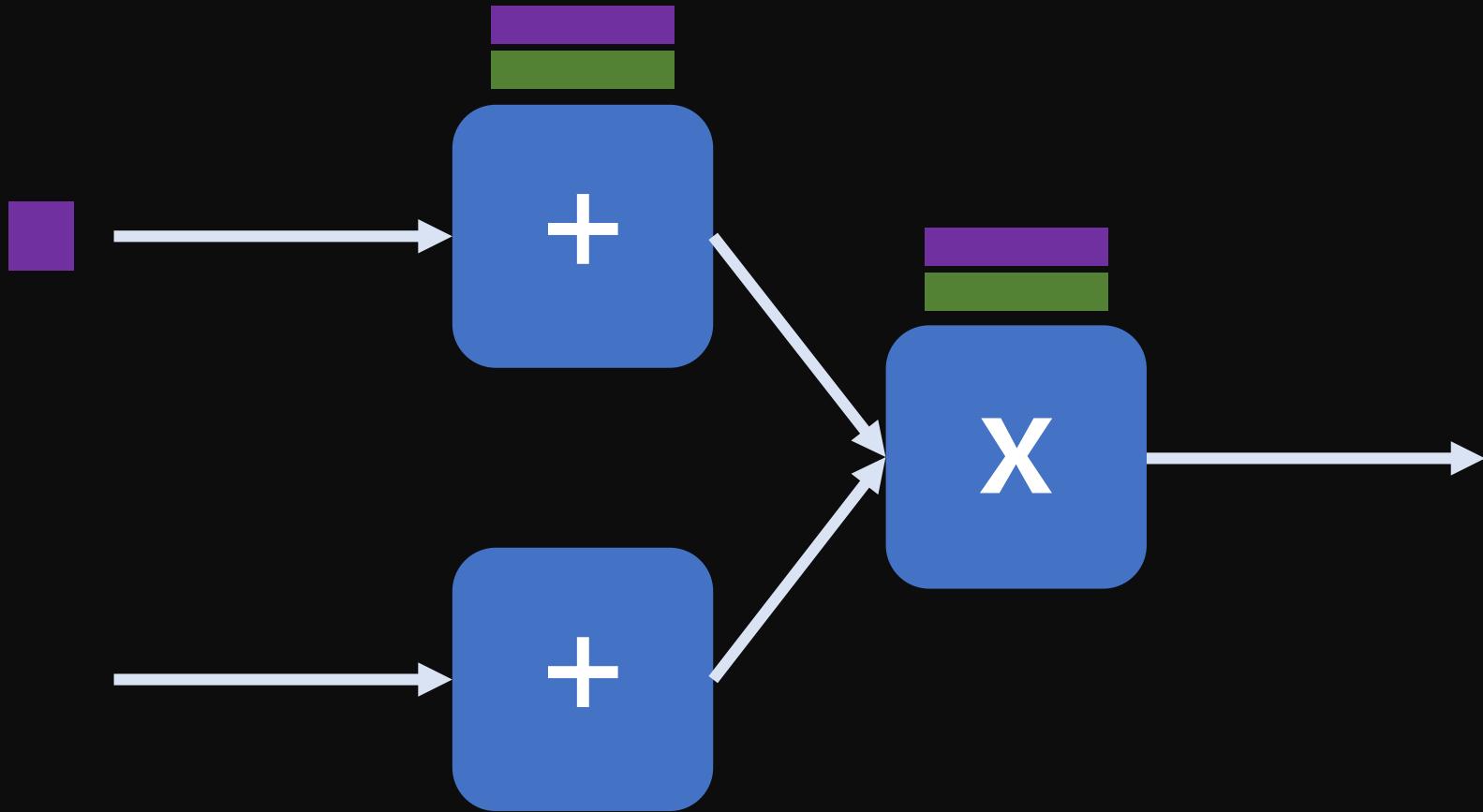
$$M_{golden} \rightarrow M_{FXP}$$

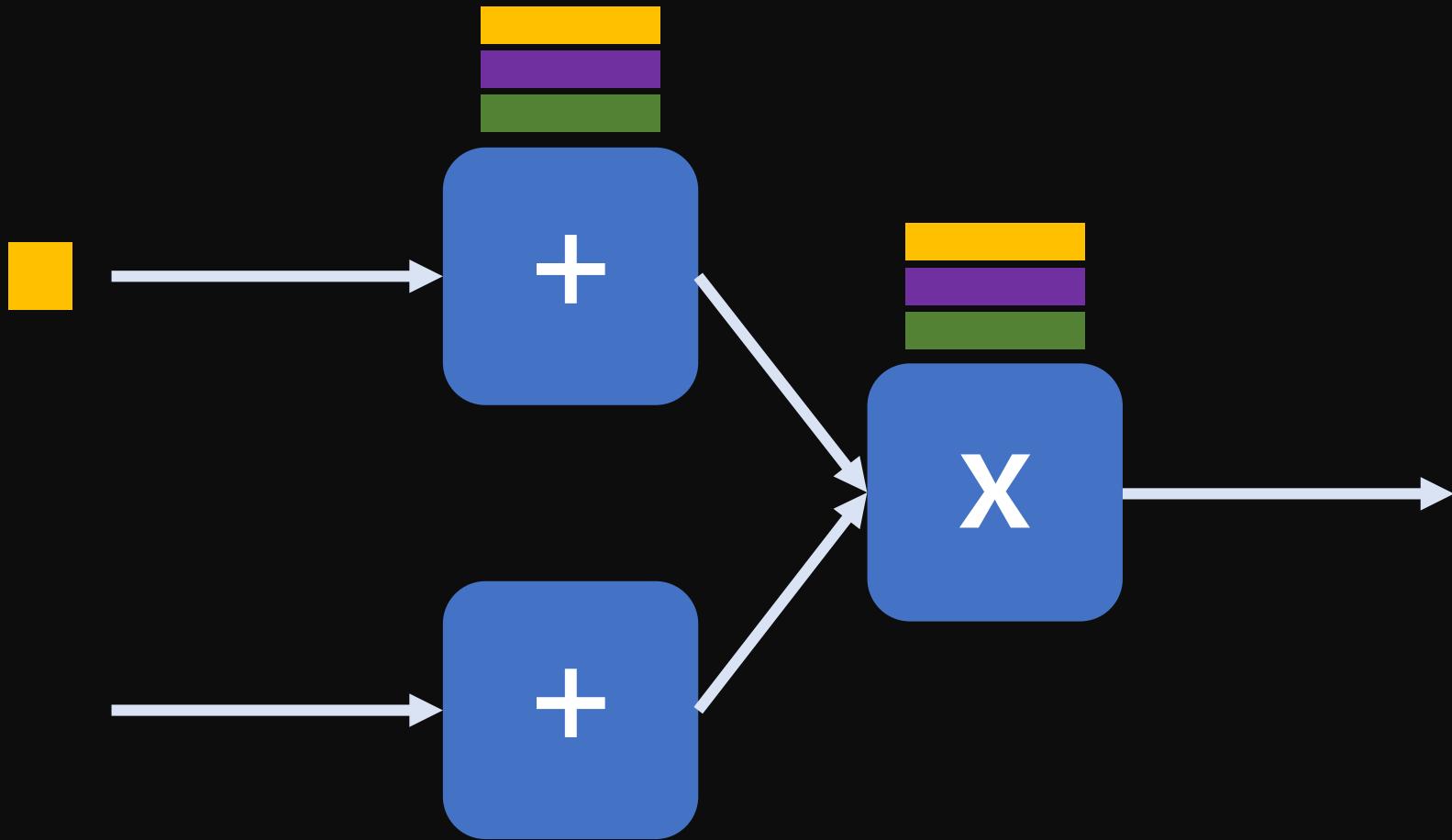
$$T = T_{FXP1} \ldots T_{FXPn}$$

$$T_{FXPi}=\{t_1,t_2,\ldots t_k\}$$

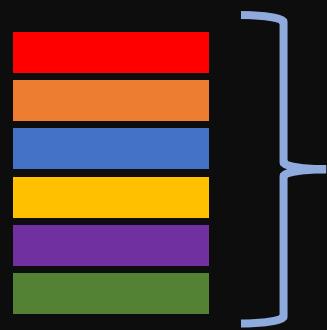
$$t_j=[DBL\rightarrow(1.15)]$$



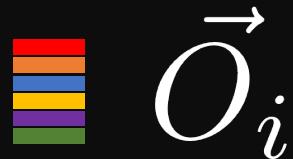




$IntMax$ }
integer bits required
for no overflow



FracMin
fractional bits required
to meet local SNR

$$t = [DBL \rightarrow (I.F)]$$

$$EXP_{(I.F)}(\vec{O}_i)$$

$$\|\vec{O}_i - FXP_{I.F}(\vec{O}_i)\|$$

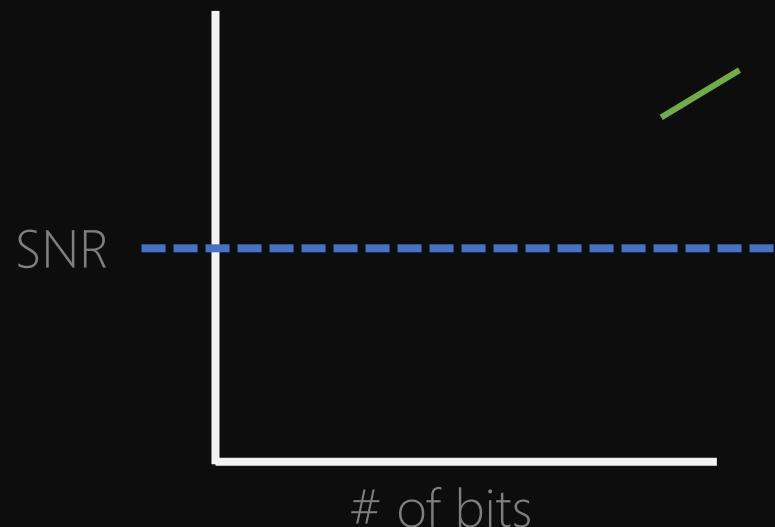
$$\sqrt{\sum_{j=1}^n(o_j - FXP_{I.F}(o_j))^2}$$

$$\|\vec{O}_i\| = \sqrt{\sum_{j=1}^n o_j^2}$$

$$SNR_i = \log_{10} \left(\frac{\|\vec{O}_i\|}{\|\vec{O}_i - FXP_{I.F}(\vec{O}_i)\|} \right)$$

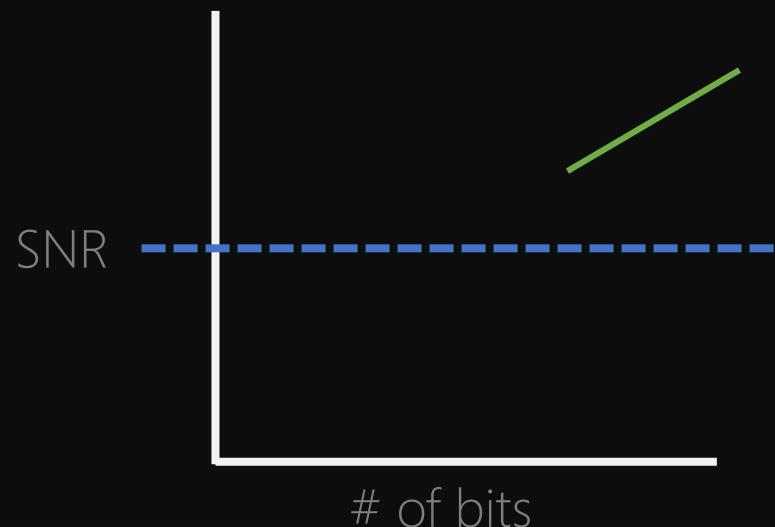
FINDING FRACTIONAL BITS

XXXX.YYYYYYYYYYYYYYYYY



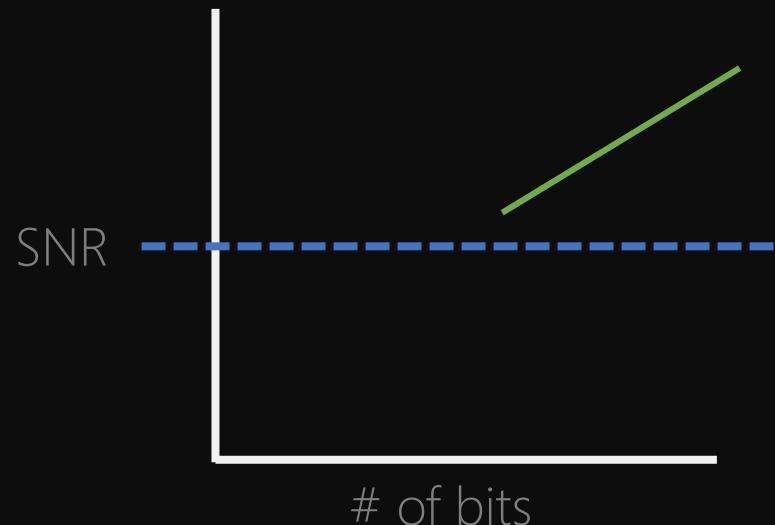
FINDING FRACTIONAL BITS

XXXX.YYYYYYYYYYYYYY



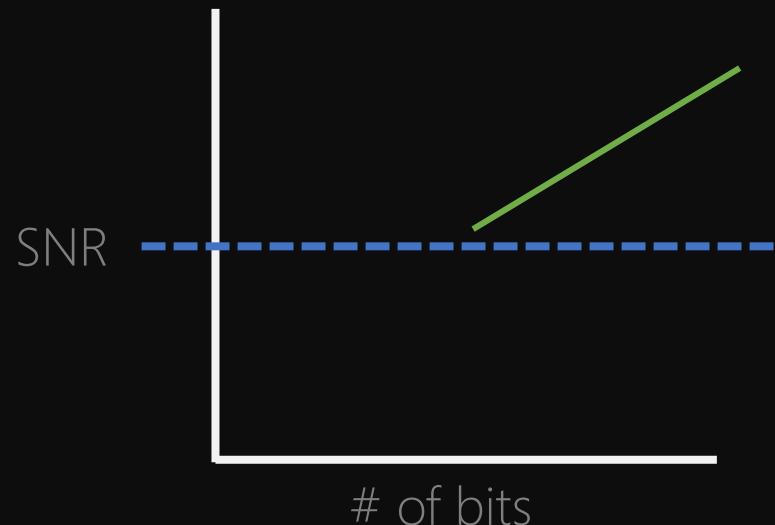
FINDING FRACTIONAL BITS

XXXX.YYYYYYYYYYYY



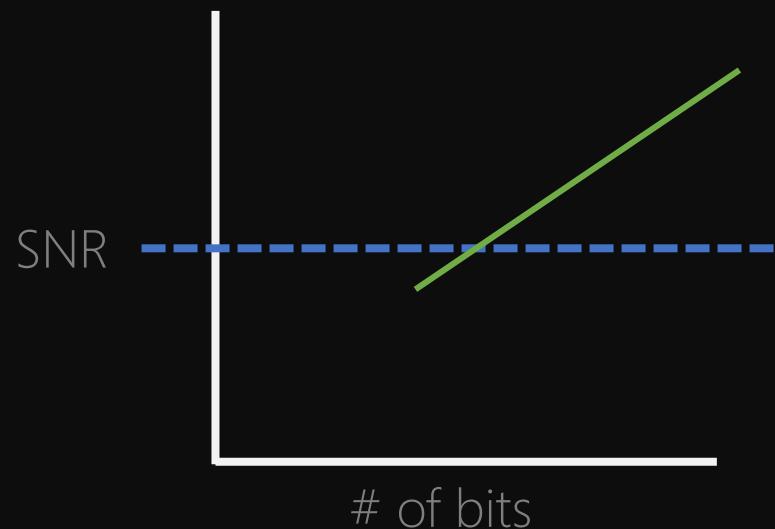
FINDING FRACTIONAL BITS

XXXX.YYYYYYYYYY



FINDING FRACTIONAL BITS

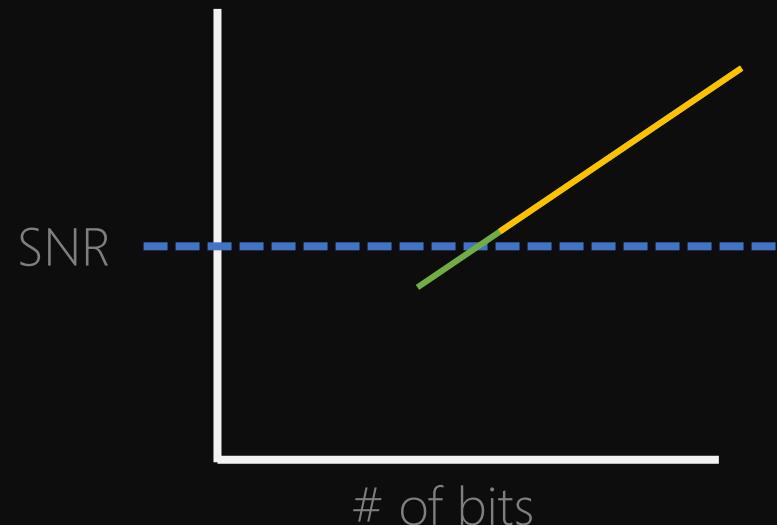
XXXX.YYYYYYYYYY



FINDING FRACTIONAL BITS

9 fractional bits

XXXX.YYYYYYYYYY

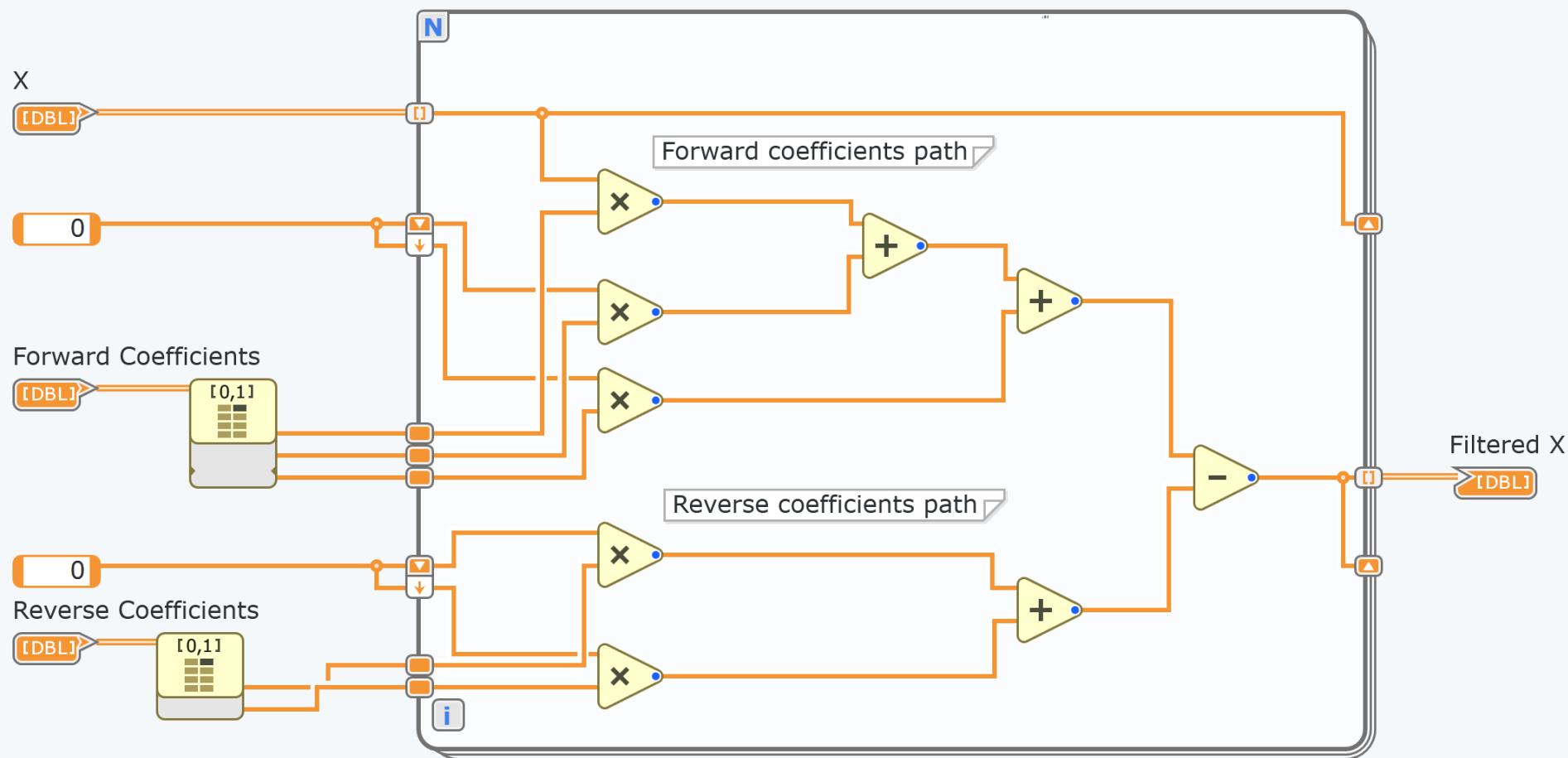


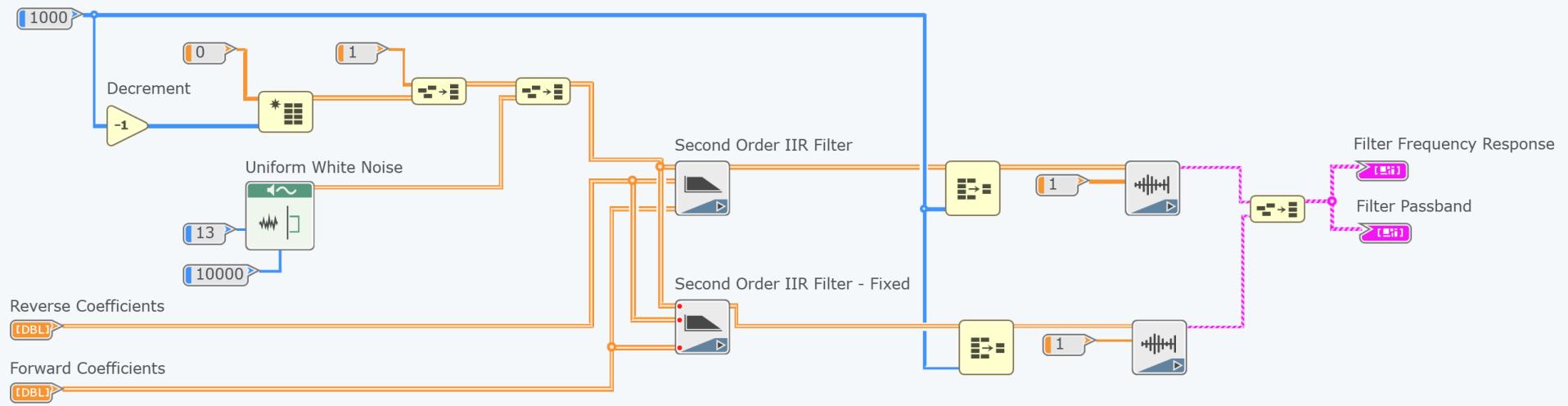
$$T = T_{FXP1} \ldots T_{FXPn}$$

$$T_{FXP1} = \{t_1,t_2,\ldots t_k\}$$

$$t_j=[DBL\rightarrow(IntMax_j.FracMin_j)]$$

THE WORKFLOW

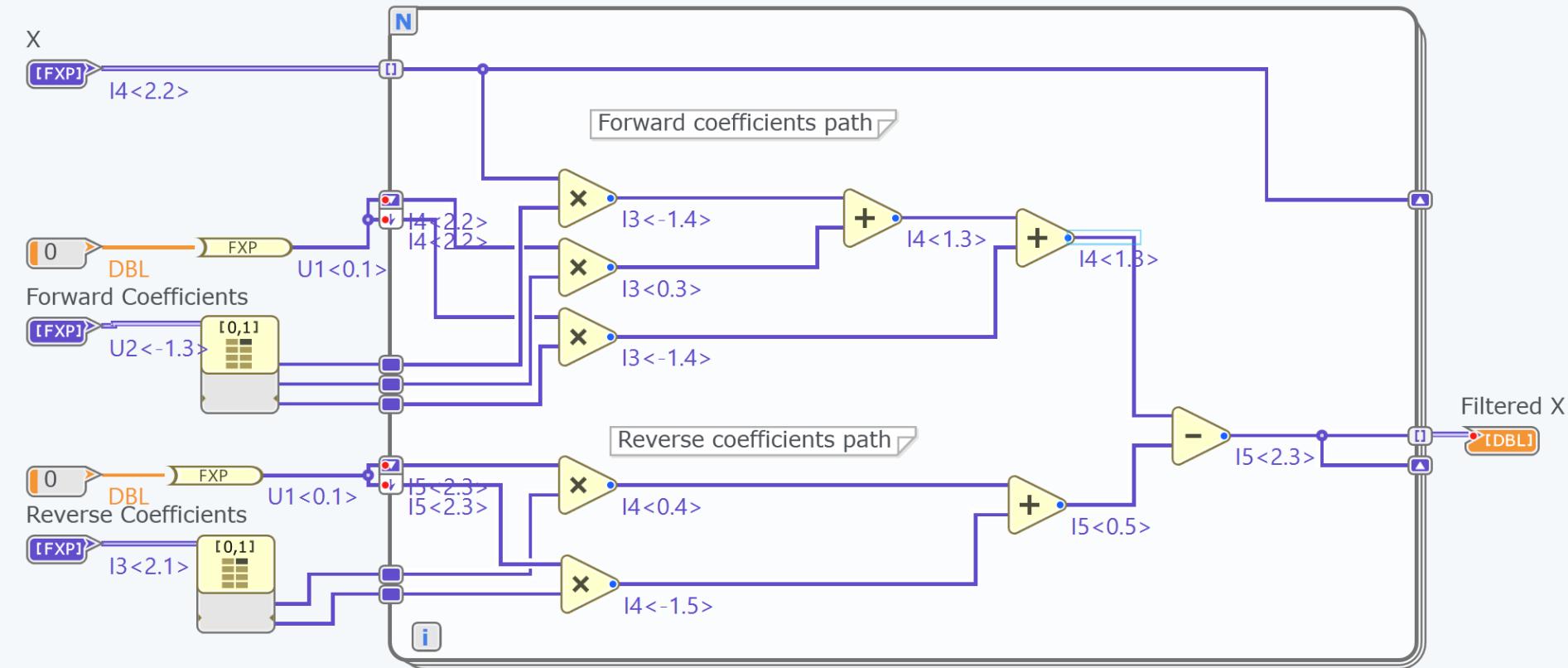




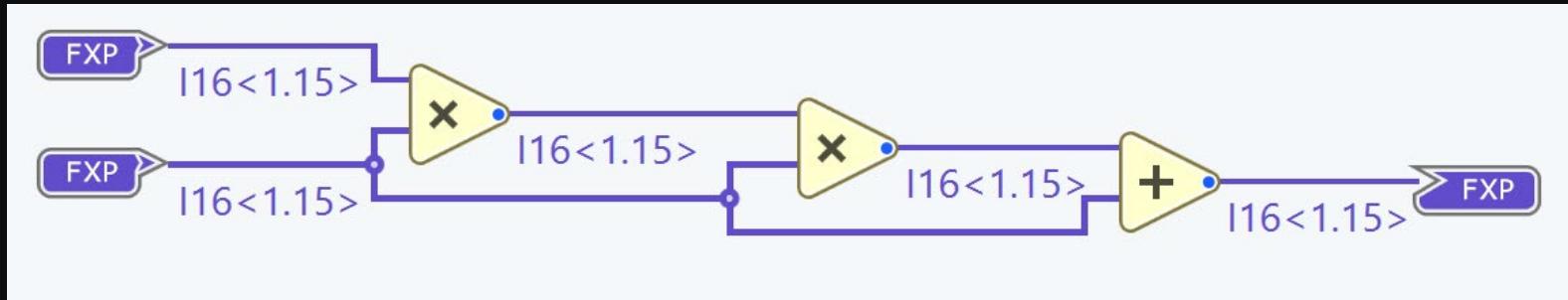
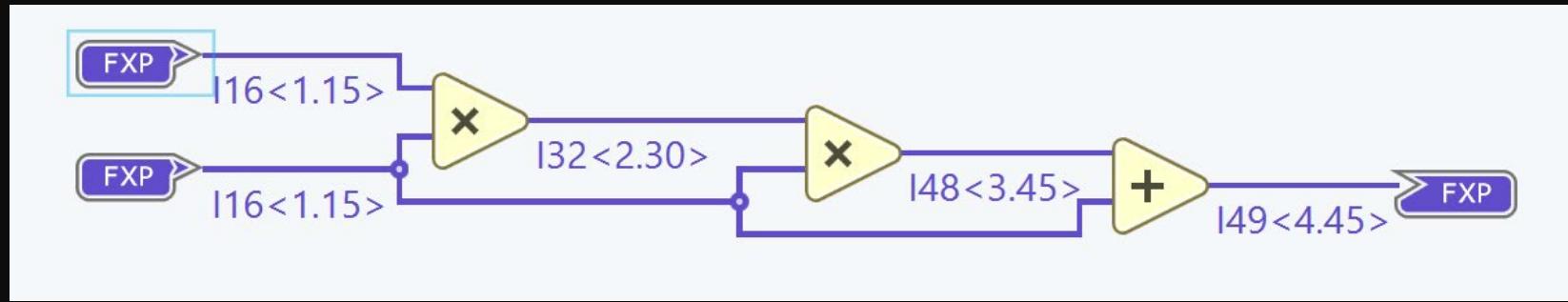
Convert to Fixed-Point

Convert Using Suggestion Edit Type Filter Sort Flush Profile Data Strategy: SNR (dB) ▾ 10

File Name	Object	Type	(Initial Suggestion)	SNR	Overflow	Underflow
Second Order IIR Filter - FXP.gvi	X	DBL	(I4<2.2>)	(12.41)	(0%)	(23%)
Second Order IIR Filter - FXP.gvi	Reverse Coefficients	DBL	(I3<2.1>)	(11.16)	(0%)	(66.7%)
Second Order IIR Filter - FXP.gvi	Forward Coefficients	DBL	(U2<-1.3>)	(10.57)	(0%)	(0%)
Second Order IIR Filter - FXP.gvi	Numeric Constant	DBL	(U1<0.1>)	(+Inf)	(0%)	(0%)
Second Order IIR Filter - FXP.gvi	Numeric Constant	DBL	(U1<0.1>)	(+Inf)	(0%)	(0%)
Second Order IIR Filter - FXP.gvi	Multiply	DBL	(I3<-1.4>)	(11.55)	(0%)	(25.4%)
Second Order IIR Filter - FXP.gvi	Multiply	DBL	(I3<0.3>)	(11.52)	(0%)	(25.4%)
Second Order IIR Filter - FXP.gvi	Multiply	DBL	(I3<-1.4>)	(11.55)	(0%)	(25.4%)
Second Order IIR Filter - FXP.gvi	Add	DBL	(I4<1.3>)	(12.46)	(0%)	(24.5%)
Second Order IIR Filter - FXP.gvi	Add	DBL	(I4<1.3>)	(13.2)	(0%)	(24.9%)
Second Order IIR Filter - FXP.gvi	Subtract	DBL	(I5<2.3>)	(14.8)	(0%)	(30.5%)
Second Order IIR Filter - FXP.gvi	Multiply	DBL	(I4<0.4>)	(10.71)	(0%)	(43.2%)
Second Order IIR Filter - FXP.gvi	Multiply	DBL	(I4<-1.5>)	(13.95)	(0%)	(32.8%)
Second Order IIR Filter - FXP.gvi	Add	DBL	(I5<0.5>)	(14.22)	(0%)	(32.5%)

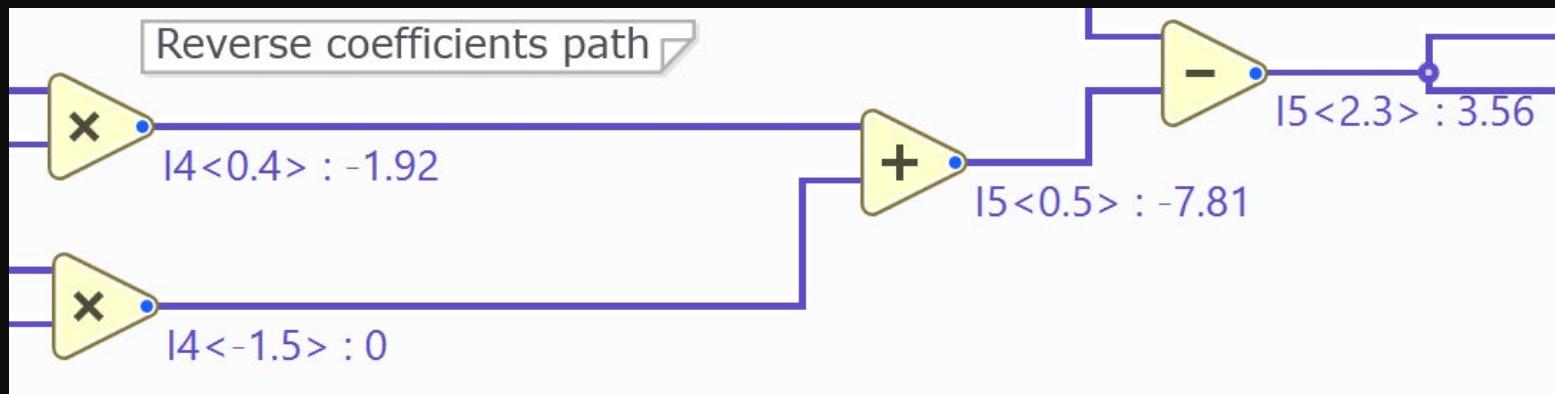


LOCAL ERROR V. REAL ERROR



CORRECT ENOUGH
BY CONSTRUCTION

Convert Using Suggestion	Edit Type	Filter	Sort	Flush Profile Data	Strategy:	SNR (dB)	▼	10
File Name	Object	Type	(Initial Suggestion)		SNR	Overflow		Underflow
Second Order IIR Filter - FXP.gvi	X	I4<2.2>			18.1	0%		11.4%
Second Order IIR Filter - FXP.gvi	Reverse Coefficients	I3<2.1>			11.16	0%		33.3%
Second Order IIR Filter - FXP.gvi	Forward Coefficients	U2<-1.3>			16.36	0%		0%
Second Order IIR Filter - FXP.gvi	Numeric Constant	U1<0.1>			+Inf	0%		0%
Second Order IIR Filter - FXP.gvi	Numeric Constant	U1<0.1>			+Inf	0%		0%
Second Order IIR Filter - FXP.gvi	Multiply	I3<-1.4>			15.55	5.92%		11.4%
Second Order IIR Filter - FXP.gvi	Multiply	I3<0.3>			12.96	0%		11.4%
Second Order IIR Filter - FXP.gvi	Multiply	I3<-1.4>			15.55	5.92%		11.4%
Second Order IIR Filter - FXP.gvi	Add	I4<1.3>			11.32	0%		21.9%
Second Order IIR Filter - FXP.gvi	Add	I4<1.3>			10.51	0%		20%
Second Order IIR Filter - FXP.gvi	Subtract	I5<2.3>			3.56	0%		17.6%
Second Order IIR Filter - FXP.gvi	Multiply	I4<0.4>			-1.92	3.8%		17.6%
Second Order IIR Filter - FXP.gvi	Multiply	I4<-1.5>			0	0%		99.9%
Second Order IIR Filter - FXP.gvi	Add	I5<0.5>			-7.81	0%		17.6%



Mass Edit Options for Fixed Point



Output Type Strategy

Specific Type



Auto Adapt Options

Specify Type:

e.g. 2.16

Signed

Add/Subtract Number of Bits (Relative):

+/- from Integer Component

0
▲
▼

+/- from Fractional Component

0
▲
▼

Overflow

Select Option to Change



Rounding

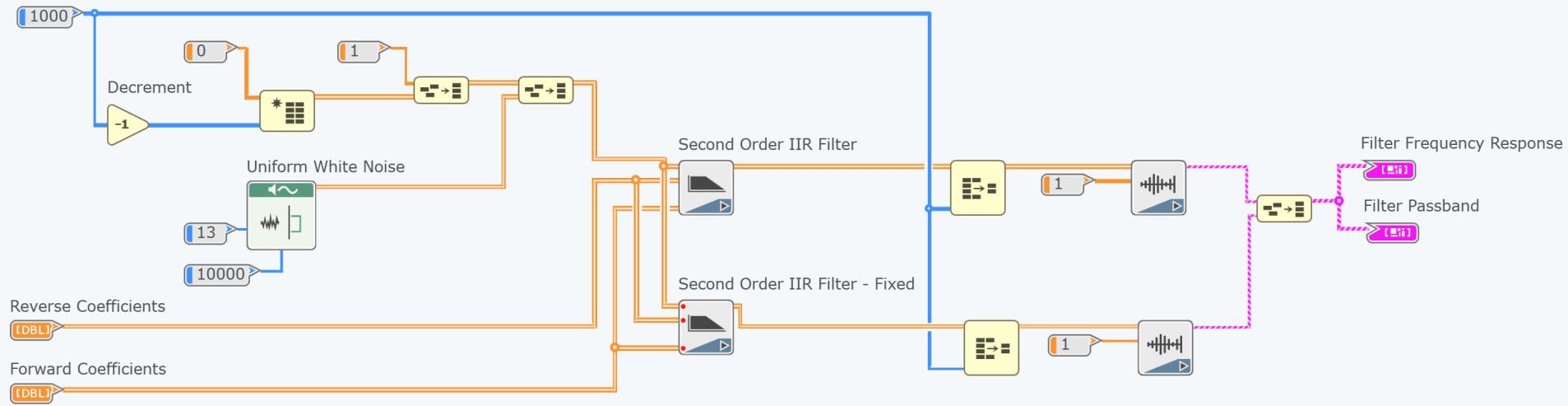
Round Half to Even



OK

Cancel

$$T = T_{F X P 1}, T_{F X P 2} \dots T_{F X P n}$$



EXECUTABILITY ALLOWS FOR CONTINUAL FEEDBACK

CONCLUSION

Our F2F tool in LabVIEW NXG FPGA:



1. Lets algorithm designers model their new algorithms in LabVIEW



2. Uses the executable nature of LabVIEW to generate an initial model transform



3. Provides tools to help designers create and apply the remaining transforms



4. Gives constant feedback on “correct enough” by construction