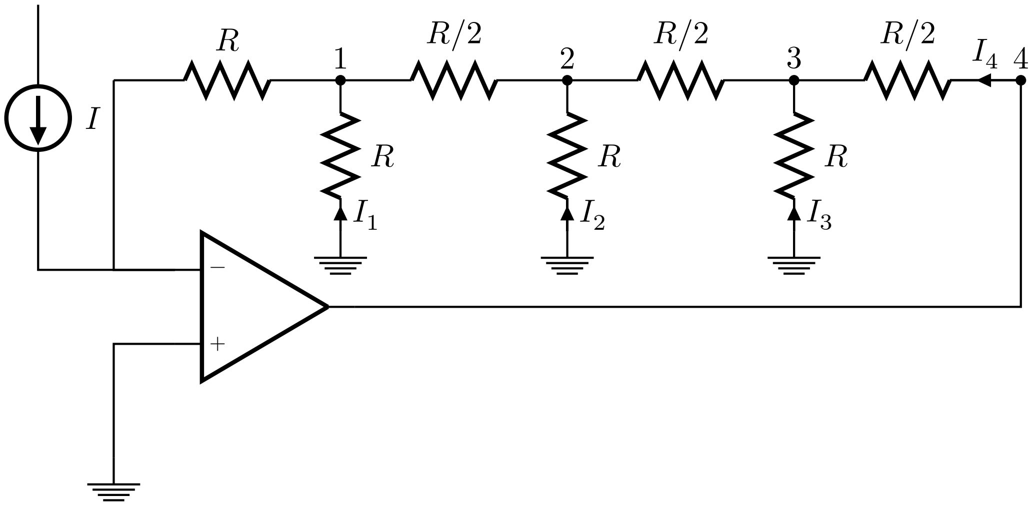
1 2.27

The circuit in Fig below can be can be consider to be an extension of the circuit in Fig. 2.8



(a) Find the resistance looking into node 1, 2, 3, 4.
Ans:

$$
\begin{aligned}
R_1 &= R \\
R_2 &= (R||R) + R/2 = R \\
R_3 &= (R||R) + R/2 = R \\
R_4 &= (R||R) + R/2 = R
\end{aligned}
$$

(b) Find the currents I_1, I_2, I_3, I_4, in terms of I
Ans:

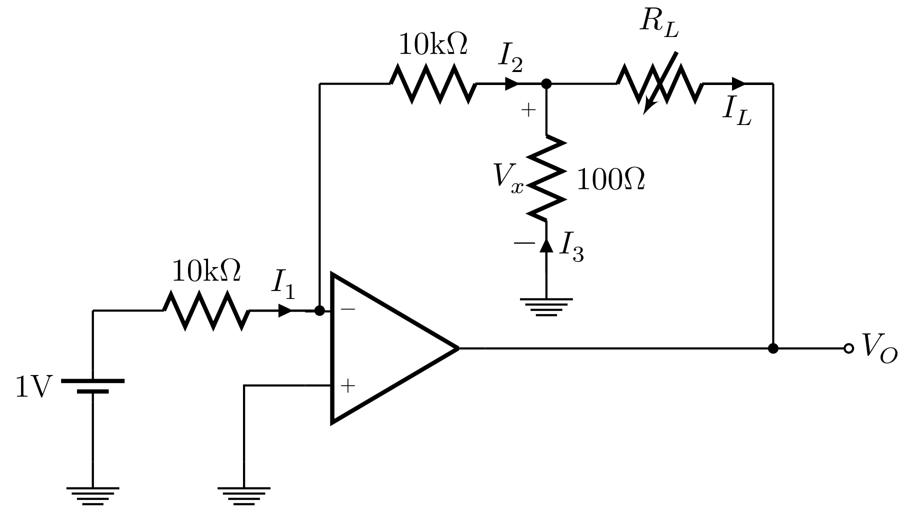
$$
\begin{aligned}
I_1 &= IR/R = I \\
I_2 &= ((I + I_1)(R/2) + IR)/R = 2I \\
I_3 &= (4IR/2 + 2IR)/R = 4I \\
I_4 &= (8IR/2 + 4IR)/R = 8I
\end{aligned}
$$

(c) Find the voltages at node 1, 2, 3, 4.
Ans:

$$
\begin{aligned}
V_1 &= IR \\
V_2 &= V_1 + 2IR/2 = 2IR \\
V_3 &= V_2 + 4IR/2 = 4IR \\
V_4 &= V_3 + 8IR/2 = 8IR
\end{aligned}
$$

2 2.28

The circuit below utilizes an ideal op amp.



(a) Find I_1, I_2, I_3, V_x
Ans:

$$\begin{aligned} I_1 &= 1\text{V}/10\text{k}\Omega = 0.1\text{mA} \\ I_2 &= I_1 = 0.1\text{mA} \\ V_x &= 0 - (0.1\text{mA})(10\text{k}\Omega) = -1\text{V} \\ I_3 &= 1/100\Omega = 10\text{mA} \end{aligned}$$

(b) If V_O is not to be lower than -13V, find the maximum allowed value of R_L
Ans:

$$\begin{aligned} V_O &= V_x + R_L I_L = V_x + R_L(I_2 + I_3) \\ &= -1\text{V} - (10.1\text{mA})R_L \end{aligned}$$

so

$$R_L \leq 12\text{V}/10.1\text{mA} \approx 1.19$$

(c) If R_L is varied in the range 100Ω to 1kΩ, what is the corresponding change in I_L and in V_O? I_L would not change

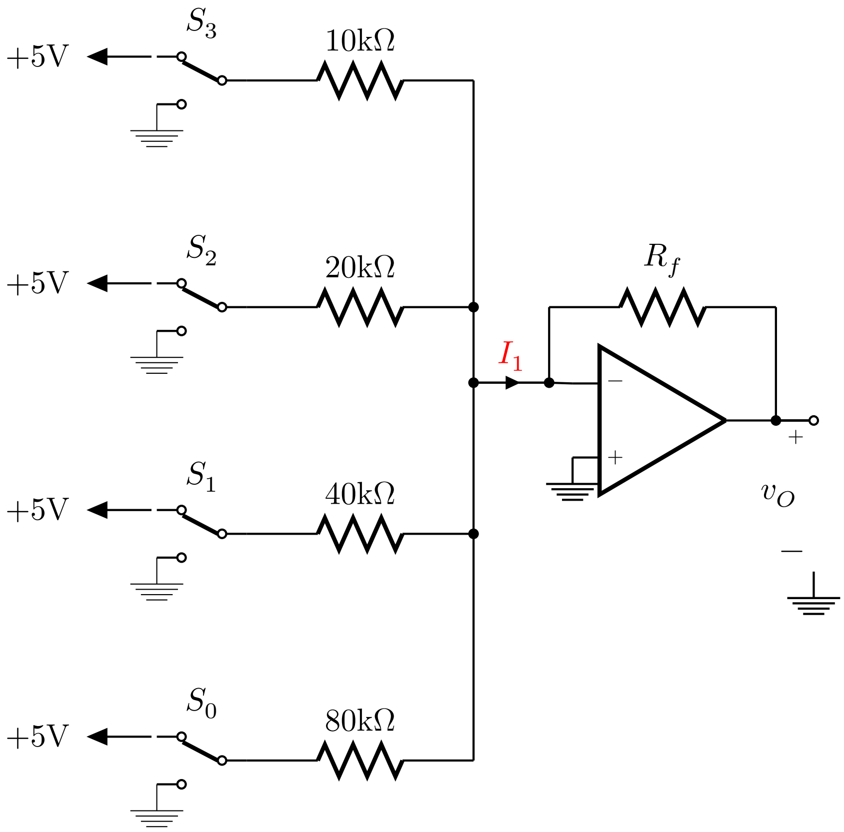
$$V_O|_{R_L=100\Omega} = 2.02\text{V}, V_O|_{R_L=1\text{k}\Omega} = 11.2\text{V}$$

3 2.37

Figure P2.37 shows a circuit for a digital-to-analog converter. The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$ where $a_i \in \{0, 1\}$. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if a_2 is 0 then switch S_2 connects the 20kΩ resistor to ground, while if a_2 is 1 then S_2 connects the 20kΩ resistor to the +5V power supply. Show that v_O is given by

$$v_O = -\frac{R_f}{16}\sum_{i=0}^{3} 2^i a_i$$

where R_f is in kiloohms. Find the value of R_f so that v_O ranges from 0 to −12V.



Ans:
Note that

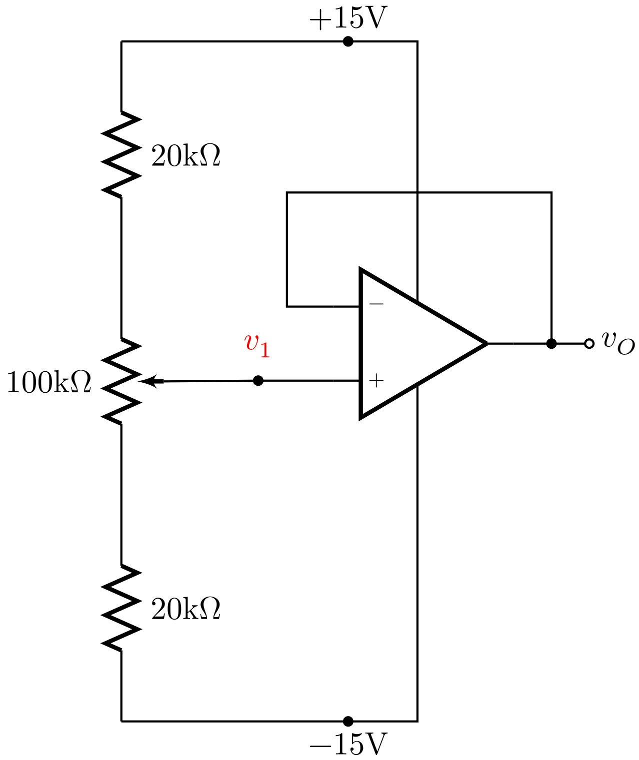
$$I_1 = \sum_{i=0}^{3} a_i(5\text{V})/(10\cdot 2^{(3-i)}\text{k}\Omega) = \sum_{i=0}^{3} a_i/2^{(4-i)}(\text{mA})$$

so

$$v_O = 0 - R_f I_1 = -R_f\sum_{i=0}^{3} a_i 2^i/16(\text{kV})$$

4 2.51

Figure shows a circuit that provides an output voltage v_o whose value can be varied by turning the wiper of the 100kΩpotentiometer. Find the range over which v_o can be varied. If the potentiometer is a "20-turn" device, find the change in v_o corresponding to each turn of the pot.



Ans:
We have

$$
\begin{aligned}
v_O &= v_1 \\
v_{1,\max} &= (15\text{V})\frac{100+20}{100+20+20} + (-15\text{V})\frac{20}{100+20+20} \approx 10.7\text{V} \\
v_{1,\min} &= -v_{1,\max}
\end{aligned}
$$

And so the voltage change each turn is $(v_{1,\max} - v_{1,\min})/20 \approx 1.07$.

5 2.63

For an instrumentation amplifier of the type shown in Fig 2.20(b), a designer proposes to make $R_2 = R_3 = R_4 = 100\text{k}\Omega$ and $2R_1 = 10\text{k}\Omega$. For ideal components, what difference-mode gain, common-mode gain, and CMRR result? Reevaluate the worst-case values for these for the situation in which all resistors are specified as $\pm 1\%$ units. Repeat the latter analysis for the case in which $2R_1$ is reduced to $1\text{k}\Omega$. What do you conclude about the importance of the relative difference gains of the first and second stages?

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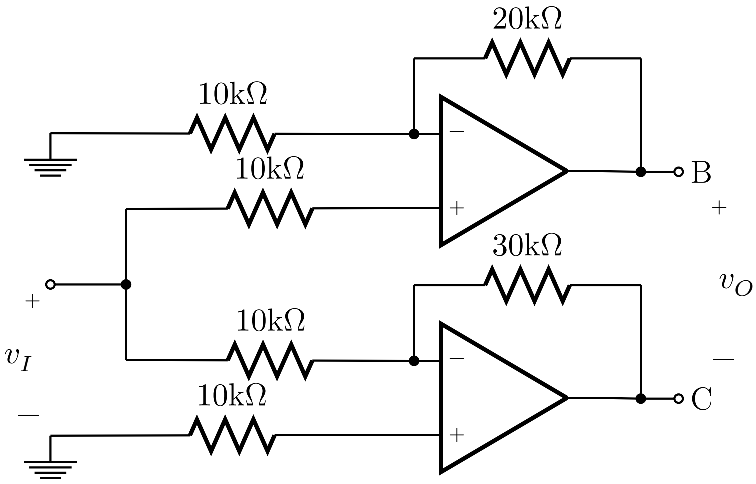
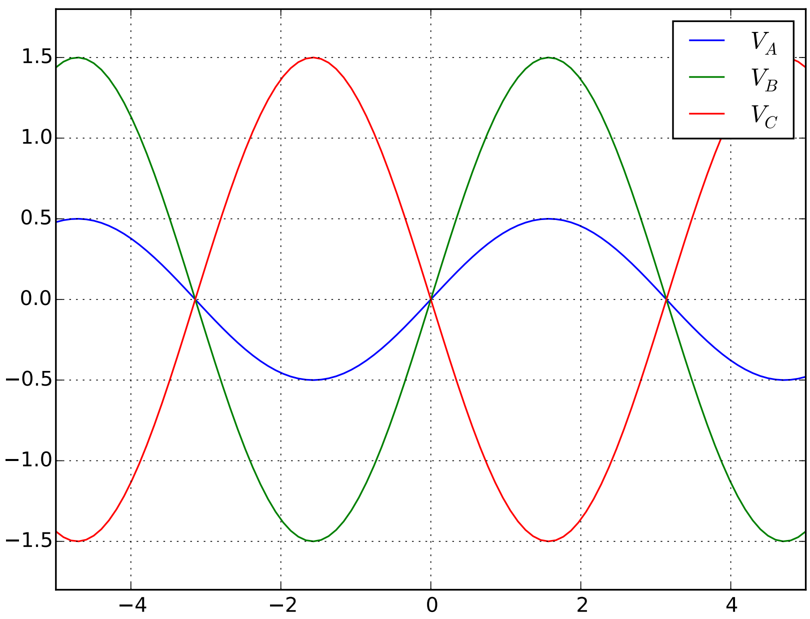
6 2.65

The circuit shown in Fig is intended to supply a voltage to floating loads (those for which both terminals are ungrounded) while making possible use of available power supply.



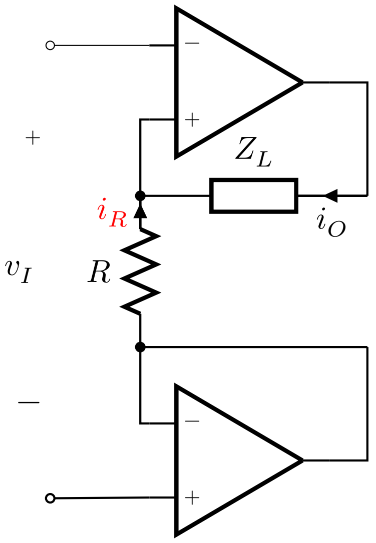
(a) Assuming ideal op amps, sketch the voltage waveforms at nodes B and C for a 1V peak-to-peak sine wave applied at A. Also sketch v_O
ans:

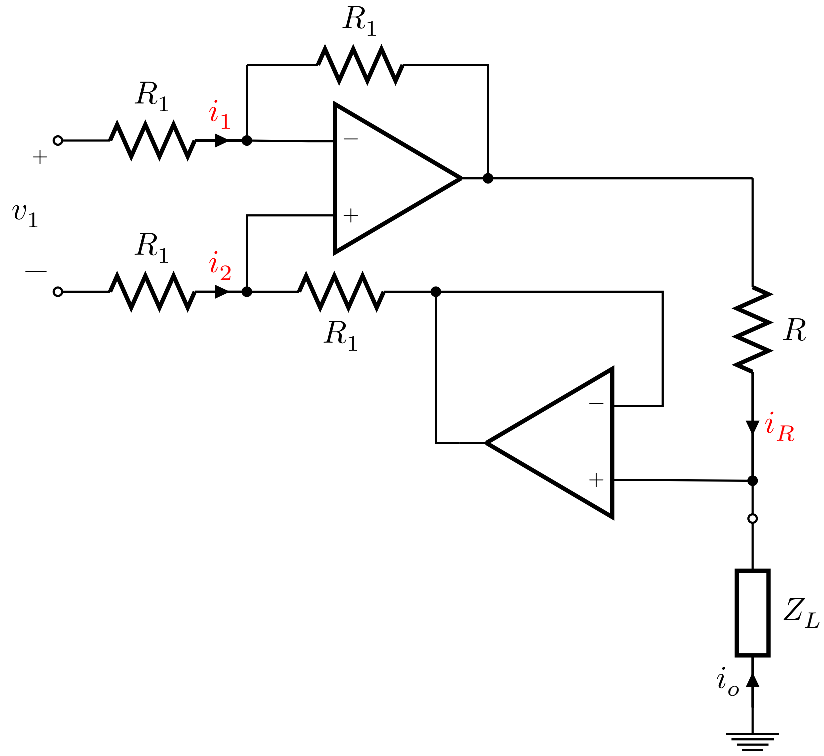


(b) What is the voltage gain v_O/v_I?
Ans: It is easy to see that $v_B = 3v_A, v_C = -3v_A$, so $v_O/v_I = 3$.

7 2.66

The two circuits in Fig are intended to function as voltage-to-current converters; that is, they supply the load impedance Z_L with a current proportional to v_I and independent of the value of Z_L. Show that this is indeed the case, and find for each circuit i_o as a function of v_I. Comment on the differences between the two circuits.





For fig 1, $i_O = i_R = v_I/R$ and hence proportional to v_I and independent of Z_L.
For fig 2, $i_O = i_R$, note that since the pos/neg terminal of the op amp above is virtual shorted, $v_I - i_1R_1 = -i_2R_1$,so $-i_1R_1 + i_2R_1 = -v_I$, hence we have

$$i_R = \frac{v_I - 2i_1R_1 + 2i_2r_1}{R} = -v_I/R$$

and hence proportional to v_I and independent of Z_L.

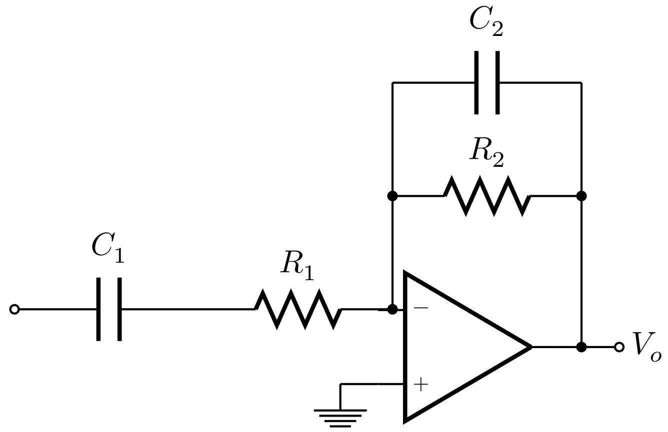
8 2.69

An op-amp-based inverting integrator is measured at 1kHz to have a voltage gain of −100V/V. At what frequency is its gain reduced to −1V/V? What is the integrator time constant?

9 2.79

Derive the transfer function of the circuit in Fig and show that it can be written in the form

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{(1 + (\omega_1/(\mathrm{i}\omega)))\,(1 + (\omega/(\mathrm{i}\omega_2)))}$$



10 2.100

A designer, wanting to achieve a stable gain of 100V/V at 5MHz, considers her choice of amplifier topologies. What unity-gain frequency would a single operational amplifier require to satisfy her need? Unfortunately, the best available amplifier has an f_t of 40MHz. How many such stages would she need to achieve her goal? What is the 3dB frequency of each stage she can use? What is the overall 3dB frequency?

11 2.102

Consider an inverting summer with two inputs V_1 and V_2 and with $V_O = -(V_1 + V_2)$. Find the 3dB frequency of each of the gain functions V_o/V_1 and V_o/V_2 in terms of the op amp f_1.

12 2.104

An op amp having a slew rate of 20V/µs is to be used in the unity-gain follower configuration, with input pulses that rise from 0 to 3V. What is the shortest pulse that can be used while ensuring full-amplitude output? For such a pulse, describe the outputing resulting.