Simplest VHDL Counter

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all; -- allows std_logic_vector to be treated like integer

entity counter8 is
	port(
		clock	: in	std_logic;
		q	: buffer	std_logic_vector(7 downto 0));
end counter8;

architecture count of counter8 is
begin
	process(clock)
	begin
		if(clock'event and clock = '1')then
			q <= q+1;
		end if;
	end process;
end count;
```