UART Receiver (References: Chapter 9 in textbook, Application Note Handout, and Lecture Notes)

You could be asked to respond to the following questions using words (W), a circuit or block diagram (C), a VHDL code segment (V), or a timing diagram (T), as appropriate to the question.

- State the required speed of a UART receiver clock, relative to a specified incoming bit rate, and calculate the required receiver clock speed. (W, T)
- State why the receiver clock requires a speed of 16× the incoming bit rate. (W, T)
- Describe the operation of the start bit detector and how it is used in the UART receiver circuit. (W, C, T)
- State the purpose of the sample clock in the UART receiver, describe how it is generated and how it is placed in the centre of an incoming bit. (W, C, V, T)
- Describe how the bit counter counts the incoming data bits of a serial character and how it tells the shift register to stop shifting after the entire character has been received. (W, C, T)
- State the two signals required to enable the receiver data shift register. Under what conditions are they active? (W, C, V, T)
- The bit counter and receiver shift register do not respond to every cycle of the receiver clock. Why not? What proportion of the receiver clock cycles do these modules respond to? Why? (W, C, V, T)
- How is data transferred from the receiver shift register to the receiver data buffer? At what point in the cycle of the bit counter does this happen? (W, C, T)
- How is the UART receiver prepared to receive a new character? What happens to the previously received character? (W, C, T)