Lab 4
Multiplexer Applications

Name_____ Class _____ Date _____

OBJECTIVES:

Upon completion of this laboratory exercise, you should be able to:

- Write VHDL design code for an 8-to-1 multiplexer, create a simulation for the design, download and test it.
- Use an 8-bit MUX as a programmable waveform generator.
- Write VHDL code for a bus multiplexer, create a simulation for the design, download and test it.
- Use a bus MUX to switch 4-bit data to a seven-segment display.

REFERENCE READING:

Dueck, Robert K., *Digital Design with CPLD Applications and VHDL*:
Chapter 6: Combinational Logic Functions
6.1 Decoders (Seven-segment decoders)
6.3 Multiplexers

EQUIPMENT REQUIRED:

Altera DE1 or DE2 Development and Education Board
AC Adapter, minimum output: 7 VDC, 250 mA DC
USB Blaster Cable
Quartus II Software
Anti-static wrist strap

PROCEDURE:

VHDL Multiplexer

1. Write a VHDL file, using a selected signal assignment statement, to design an 8-to-1 multiplexer. Define the data inputs and select inputs as STD_LOGIC_VECTOR types. Make a new folder and save the file as **mux_8ch.vhd** in that folder.

2. Write a test spec to test the correctness of this design.

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Use the test spec to create a simulation of the design in ModelSim. Show the simulation to your instructor.

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3. Make a new Block Diagram File to test the multiplexer. Save the file as **mux8test.bdf**. From the Quartus II **Project** menu, select **Set as Top-Level Entity**, as shown in Figure 1. We will use this file to place our previously designed MUX as a graphical component within a higher-level design file.

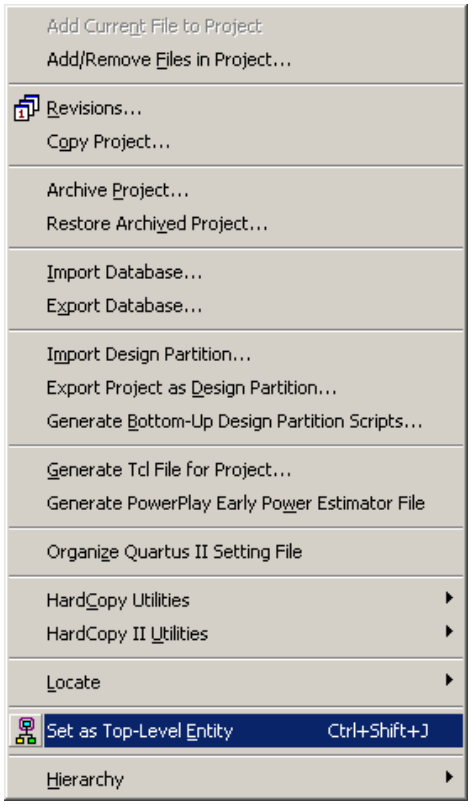

Figure 1 Project Menu

4. **Follow the instructions below and on the next page** to add two components to the design: the 8-channel multiplexer and a counter that will divide the CPLD board clock

frequency and generate a binary count so that the MUX output can be observed on an oscilloscope. The connections are shown in Figure 2.

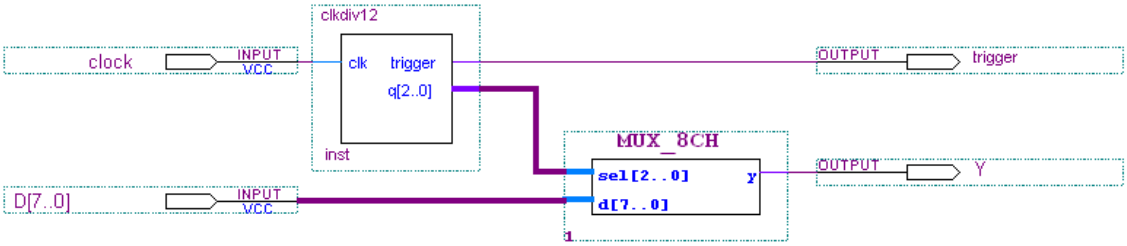

Figure 2 MUX Test File (Block Diagram File)

5. **MUX component:** Open the VHDL file for the multiplexer. From the **File** menu, select **Create/Update**, then **Create Symbol Files for the Current File**. Place the component in the Block Diagram File by double-clicking on a blank space on the desktop and selecting the component from the **Project** library in the dialog box that opens, as shown in Figure 3.

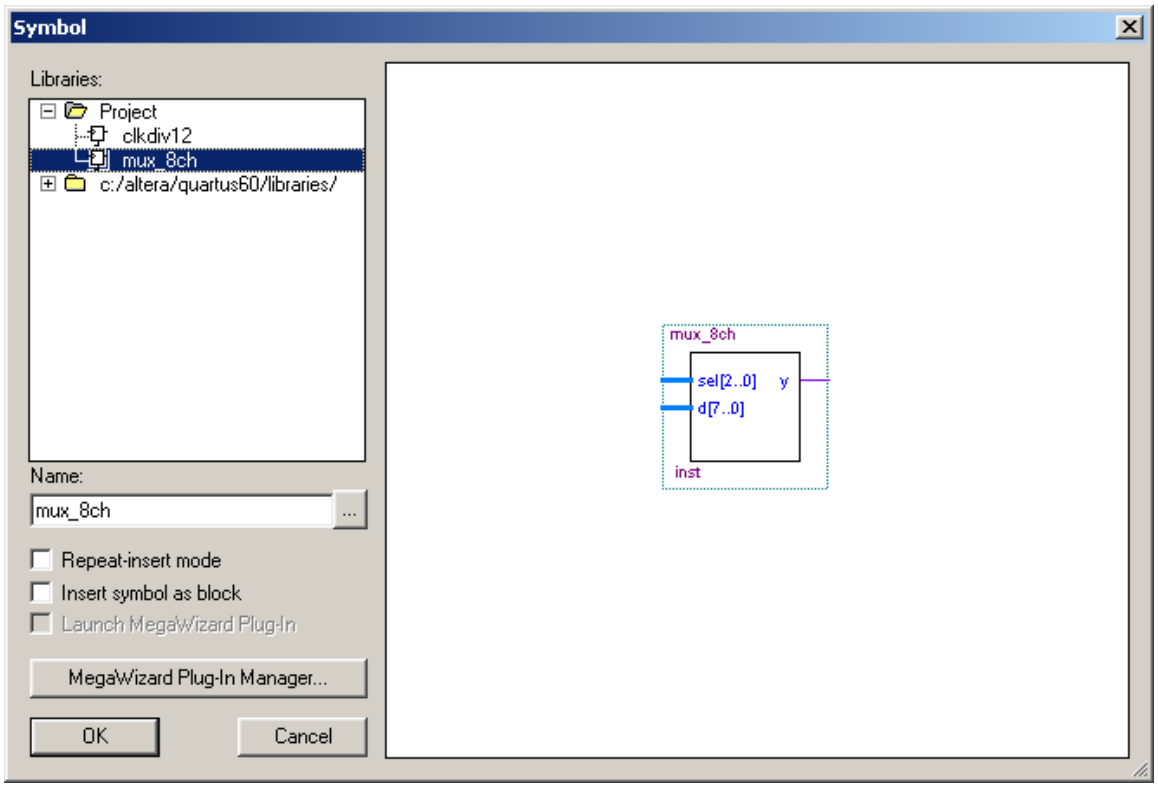

Figure 3 Inserting a user-defined component

6. **Clock divider component:** The clock divider is called **clkdiv12**. It contains three outputs to control the MUX select inputs, as well as an output called **trigger**, which generates a HIGH pulse when MUX channel d[0] is selected. This can be used to

synchronize the oscilloscope trace to a known starting point in a repeating cycle. Its VHDL file is found on the department network in folder:

I:\Course Material\Digital Design\Student_Lab_Files\Lab04_MUX_Apps

Copy this VHDL file to the project folder. Open the file and create the component for the clock divider, using the same procedure as for the other component.

4. Compile the project. Choose pin numbers as shown in Table 1.

Table 1 Pin Assignments for MUX Test Circuit

Board: DE2			
Family: Cyclone II			
Device: EP2C20F484C7 (DE1) or EP2C35F672C6 (DE2)			
Pin Name	**Pin Number (DE1)**	**Pin Number (DE2)**	**Input or Output Device**
d[0]			
d[1]			
d[2]			
d[3]			
d[4]			
d[5]			
d[6]			
d[7]			
y	P18	W23	JP2-40
clock	L1	N2	50 MHz Clock
trigger	P17	W25	JP2-39

5. Download the design to the test board.

Monitoring the MUX Waveform Generator with an Oscilloscope

1. Connect one channel of an oscilloscope to the **y** output of the multiplexer, as shown in Table 2. Connect the other channel to the **trigger** output of the clock divider. Trigger the oscilloscope on the channel with the **trigger** signal.

Table 2 Connections for oscilloscope

Connection: IDE Cable into JP2 (right side of board)
y: Insert wire into pin 40
trigger: Insert wire into pin 39
ground: Insert wire into pin 30

2. Set the D switches to 01010101. What do you see on the oscilloscope? How does this relate to the D inputs.

_____
_____
_____
_____

3. Change the D switches to 00010100. How does the waveform change?

_____
_____
_____
_____

4. Set the D switches to 00000000. Change the switches to HIGH, one at a time. Note your observations below.

_____
_____
_____
_____

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5. Close the project for the 8-channel MUX.

VHDL Bus Multiplexer

1. Create a new folder for a VHDL Bus Multiplexer. Write a VHDL file that defines a multiplexer that switches two 4-bit inputs, **x** and **y** to a 4-bit output, **z**. Define **x**, **y**, and **z** as type BIT_VECTOR. Save the file as in the new folder as **quad2to1.vhd**.

2. Write a test spec to test the correctness of this design.

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Use the test spec you wrote to create a simulation in ModelSim. Show the simulation to your instructor.

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3. Create a symbol for the MUX and, in a new Block Diagram File, connect the **z** outputs to a hexadecimal-to-seven-segment decoder created in Lab 3, as shown in Figure 4. Recall that the Altera DE2 board has common anode (active-LOW) numerical displays.

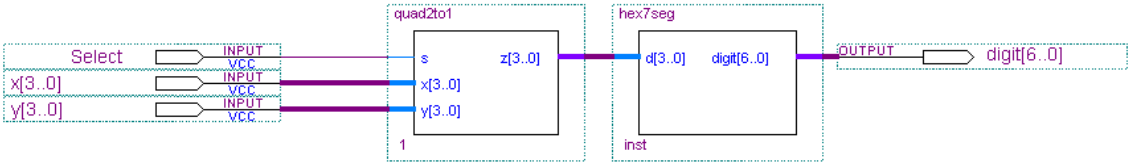

Figure 4 4-bit Bus MUX Test Circuit

4. Assign the device and pin numbers as shown in Table 3.

Table 3 Pin Assignments for 4-bit Bus MUX Test Circuit

Board: DE2		
Family: Cyclone II		
Device: EP2C20F484C7 (DE1) or EP2C35F672C6 (DE2)		
Pin Name	**Pin Number**	**Switch or LED Number**
y[0]		
y[1]		
y[2]		
y[3]		
x[0]		
x[1]		
x[2]		
x[3]		
select		
digit[0]		
digit[1]		
digit[2]		
digit[3]		
digit[4]		
digit[5]		
digit[6]		

5. Save and compile the file and download it to the CPLD test board.

6. Set switches for input **x** to 0101. Set switches input **y** to 1100. What effect does the **Select** switch have on the digit shown on the seven-segment display? Try several combinations of **x** and **y**. Show the results to your instructor.

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