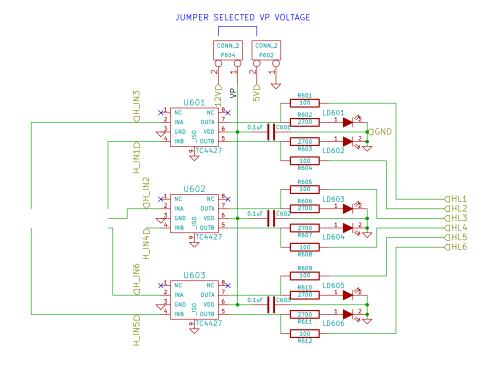
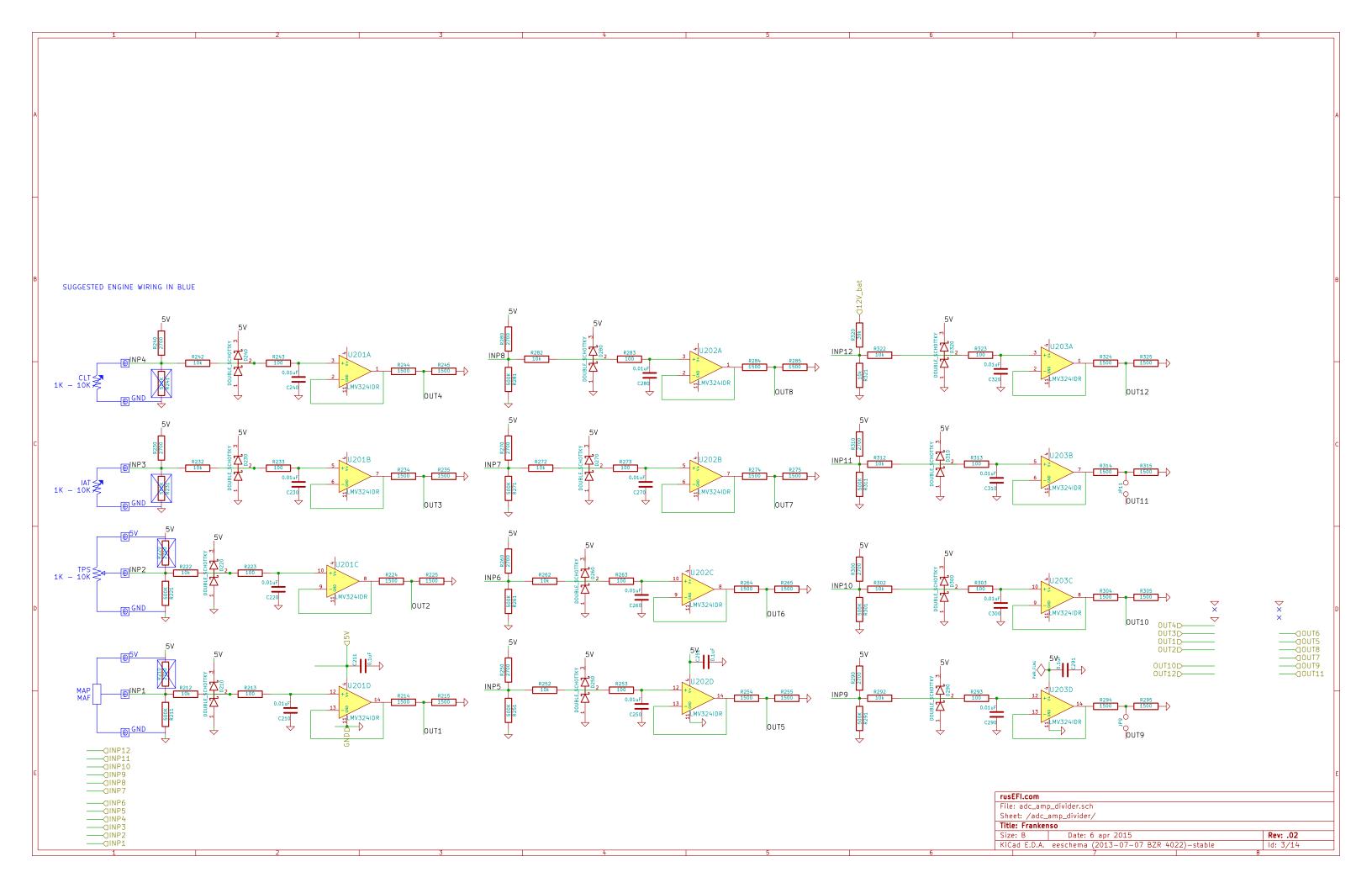
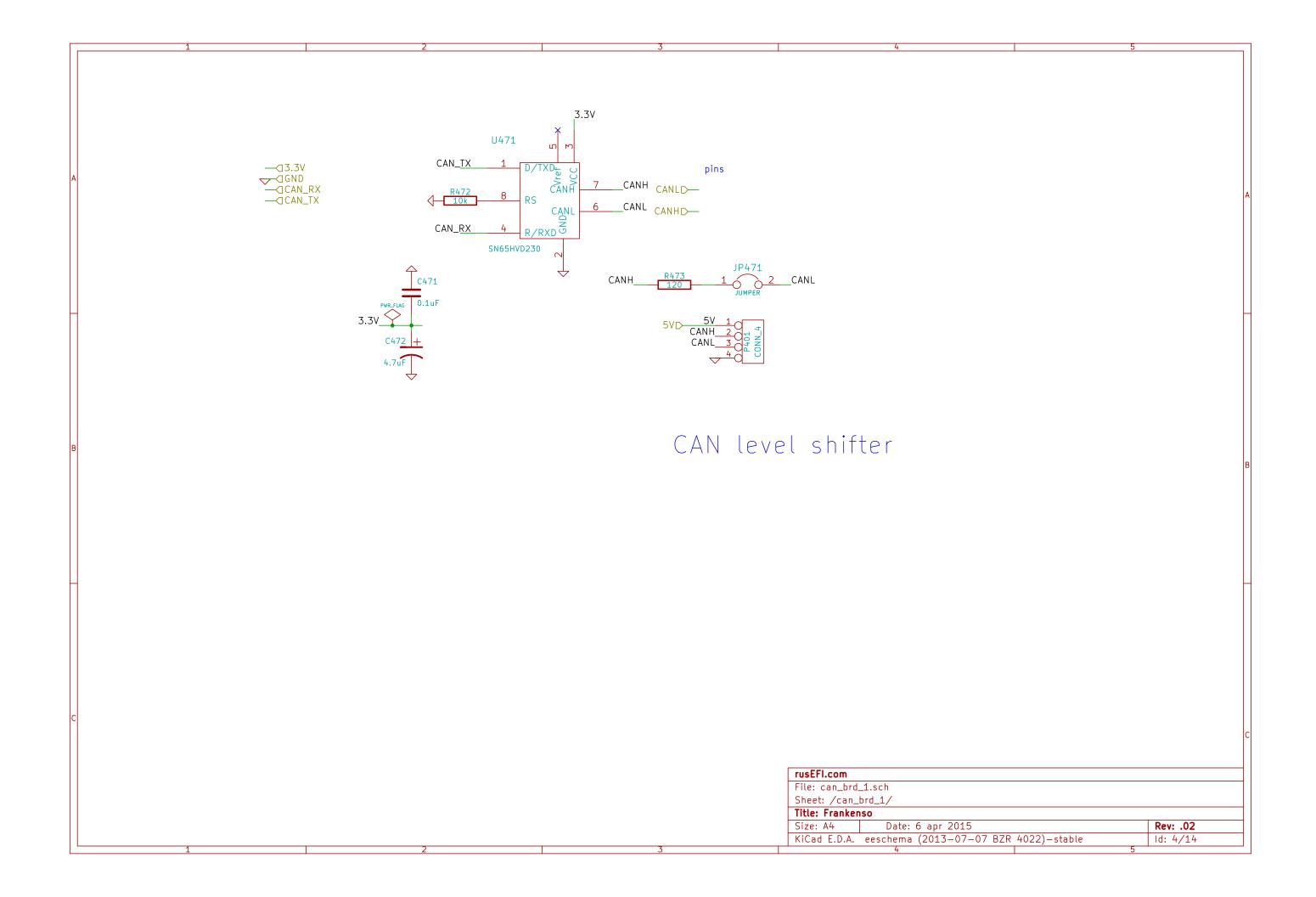


## 6 channel high / low side driver

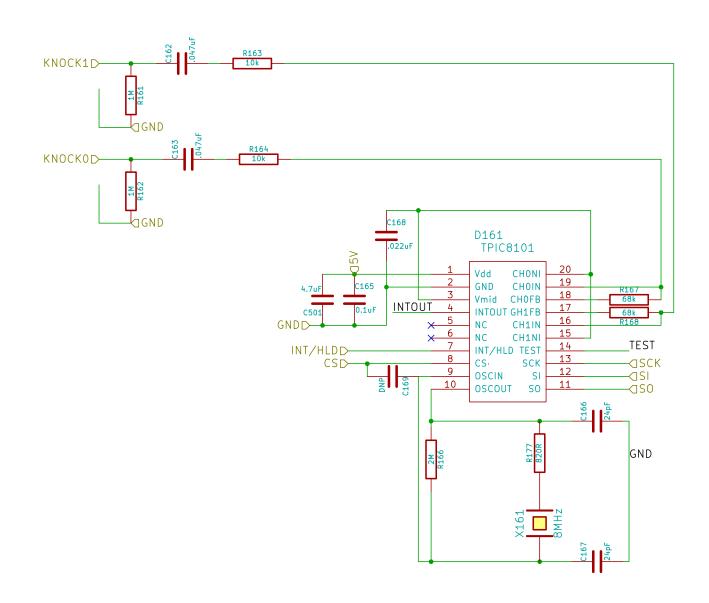


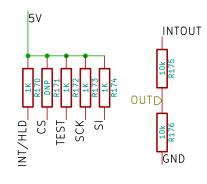
rusEFI.com				
File: hi-lo.sch				
Sheet: /hi-lo/				
Title: Frankenso				
Size: B	Date: 6 apr 2015	Rev: .02		
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	ld: 2/14		
	7	8		

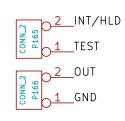




## DD\_HIP9011 ver.2 RusEfi.com



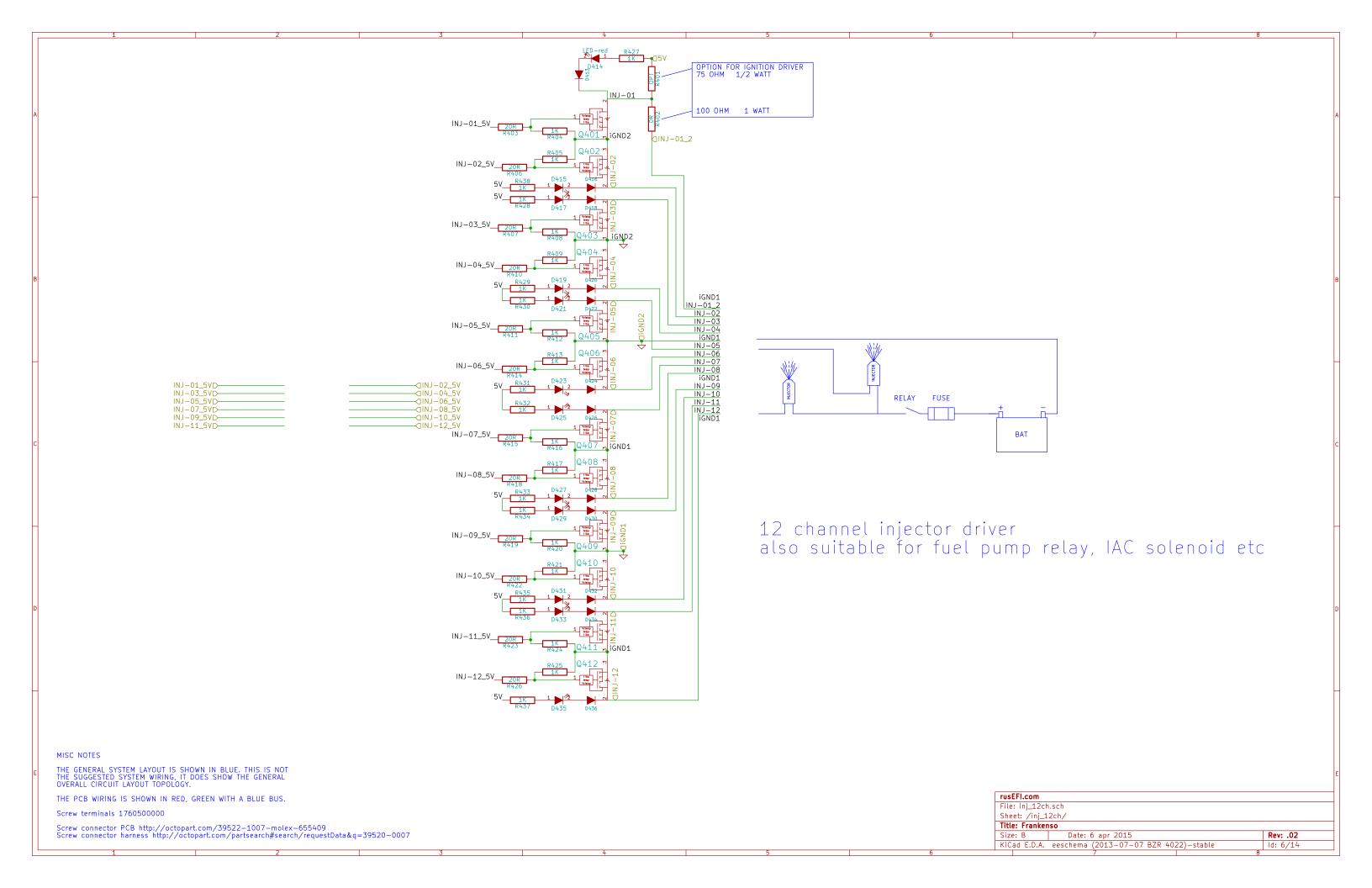




rusEFI.com

http://www.crystek.com/documents/appnotes/Pierce-GateIntroduction.pdf
PCB per predictions with SaturnPCB has less then 3.5pF traces,
TPIC pins assumed 5pF
ESR = 80ohms max
Rf = 2meg could be between 1meg and 10meg.
Cload = 18pF per XTAL datasheet
Cload = ([Cin+C1][C2+Cout])/(Cin+C1+C2\_Cout)+PCBstray
Cload = ([5+24][24+5])/(5+24+24+5)+3.5= 18pF
C1=C2=C166=C167 = 24pF
Rs = 1/(2piFC2) = 1/(2\*pi\*8MHz\*24pF) = 829ohms, 820ohms is close enough = R177

	File: DD_HIP9011.sch				
Sheet: /DD_HIP9011/					
Title: Frankenso					
	Size: A4	Date: 6 apr 2015	Rev: .02		
	KiCad F D A	eeschema (2013-07-07 BZR 4022)-stable	Id. 5/14		



WJO1 IS A BACKUP PLAN. THE VOLTAGE DROP ACROSS D703 MAY BE NOT TOLERABLE, SO WE HAVE A BACK UP PLAN IF WE NEED TO BYPASS THE DIODE WITH A LOWER VOLTAGE DROP U351 C702 ──USART\_TX ──USART\_RX RXD 16 USBD-15 USBD+ SHIELD 6 Shield RESET 19 RESET 4700pF × 27 × 28 OSCO CBUS1 C351 13 CB2 2 1 14 D702LED-grn CBUS2 CBUS3 3V30UT CBUS4 0.1uF C356 RESET\_\_\_\_RI FT232RL For right conn — GCS\_SD\_MODULE — GSPI\_MOSI — G3.3V Vdd - □SPI\_SCK - □GND SCLK DO -√SPI\_MISO DATA1 CDN SD card slot USB TTL module rusEFI.com File: mmc\_usb\_1.sch Sheet: /mmc\_usb\_1/ Title: Frankenso Size: A4 Date: 6 apr 2015 Rev: .02 KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable ld: 7/14

