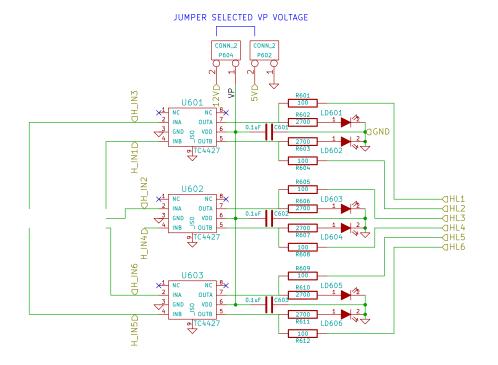
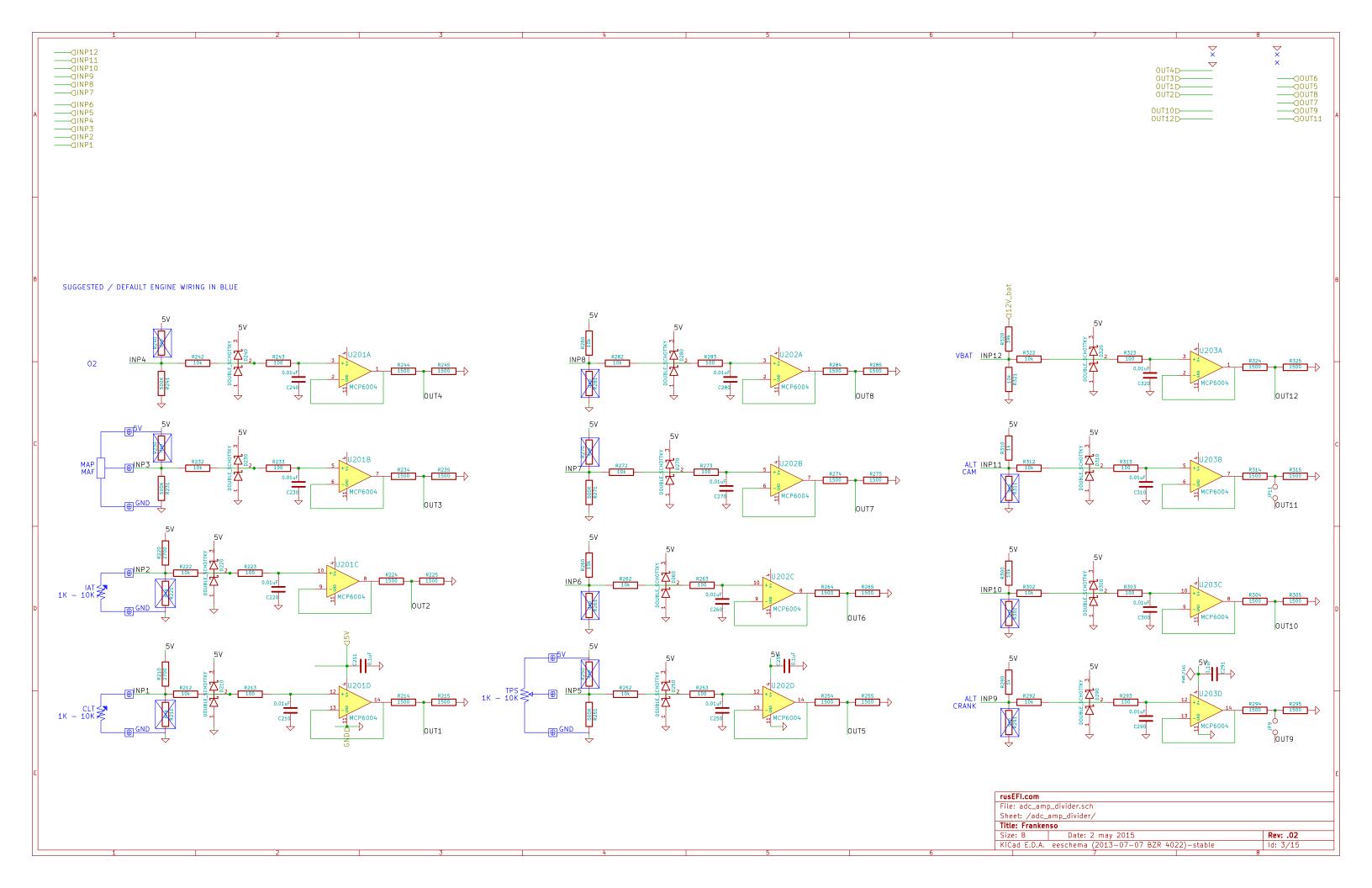
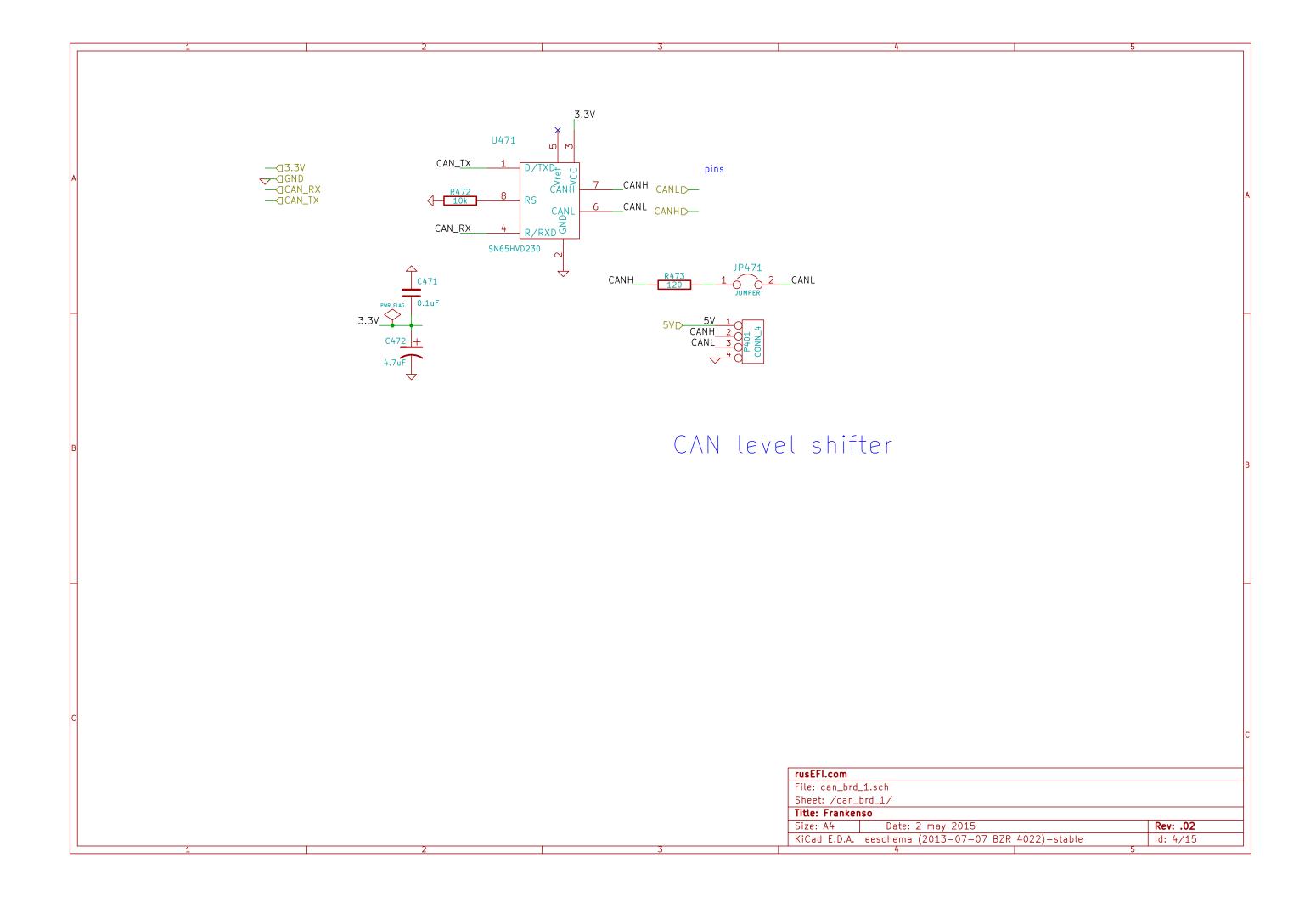


6 channel high / low side driver

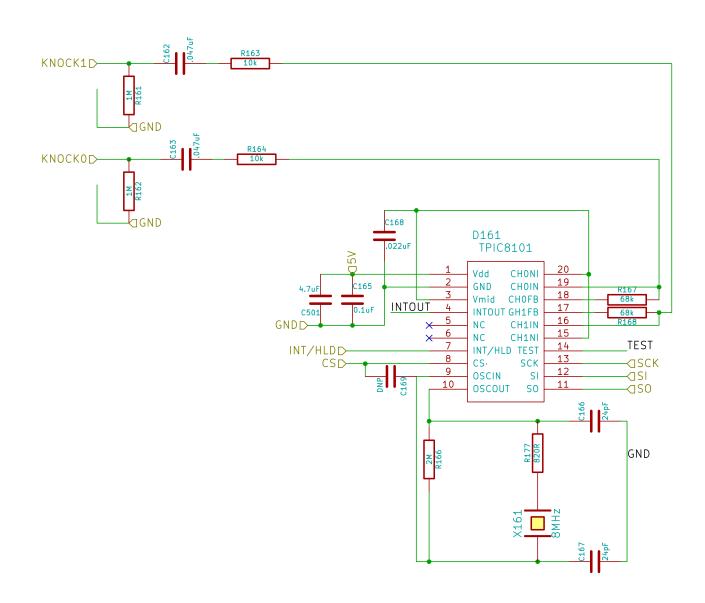


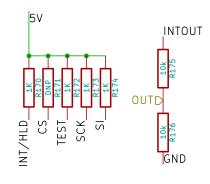
rusEFI.com		
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KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	ld: 2/15

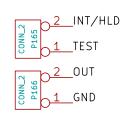




DD_HIP9011 ver.2 RusEfi.com







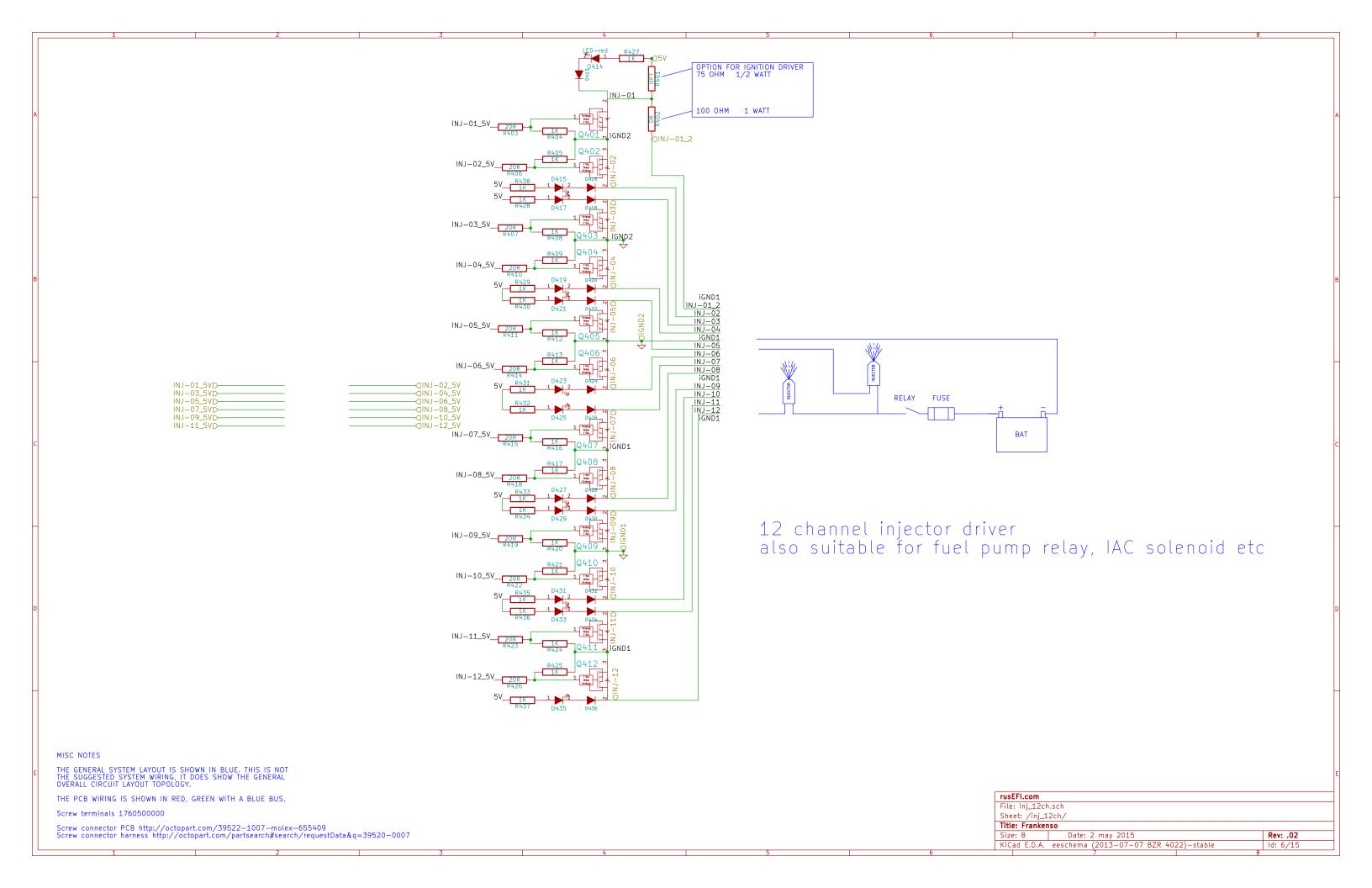
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable

http://www.crystek.com/documents/appnotes/Pierce-GateIntroduction.pdf
PCB per predictions with SaturnPCB has less then 3.5pF traces,
TPIC pins assumed 5pF
ESR = 80ohms max
Rf = 2meg could be between 1meg and 10meg.
Cload = 18pF per XTAL datasheet
Cload = ([Cin+C1][C2+Cout])/(Cin+C1+C2_Cout)+PCBstray
Cload = ([5+24][24+5])/(5+24+24+5)+3.5= 18pF
C1=C2=C166=C167 = 24pF
Rs = 1/(2piFC2) = 1/(2*pi*8MHz*24pF) = 829ohms, 820ohms is close enough = R177

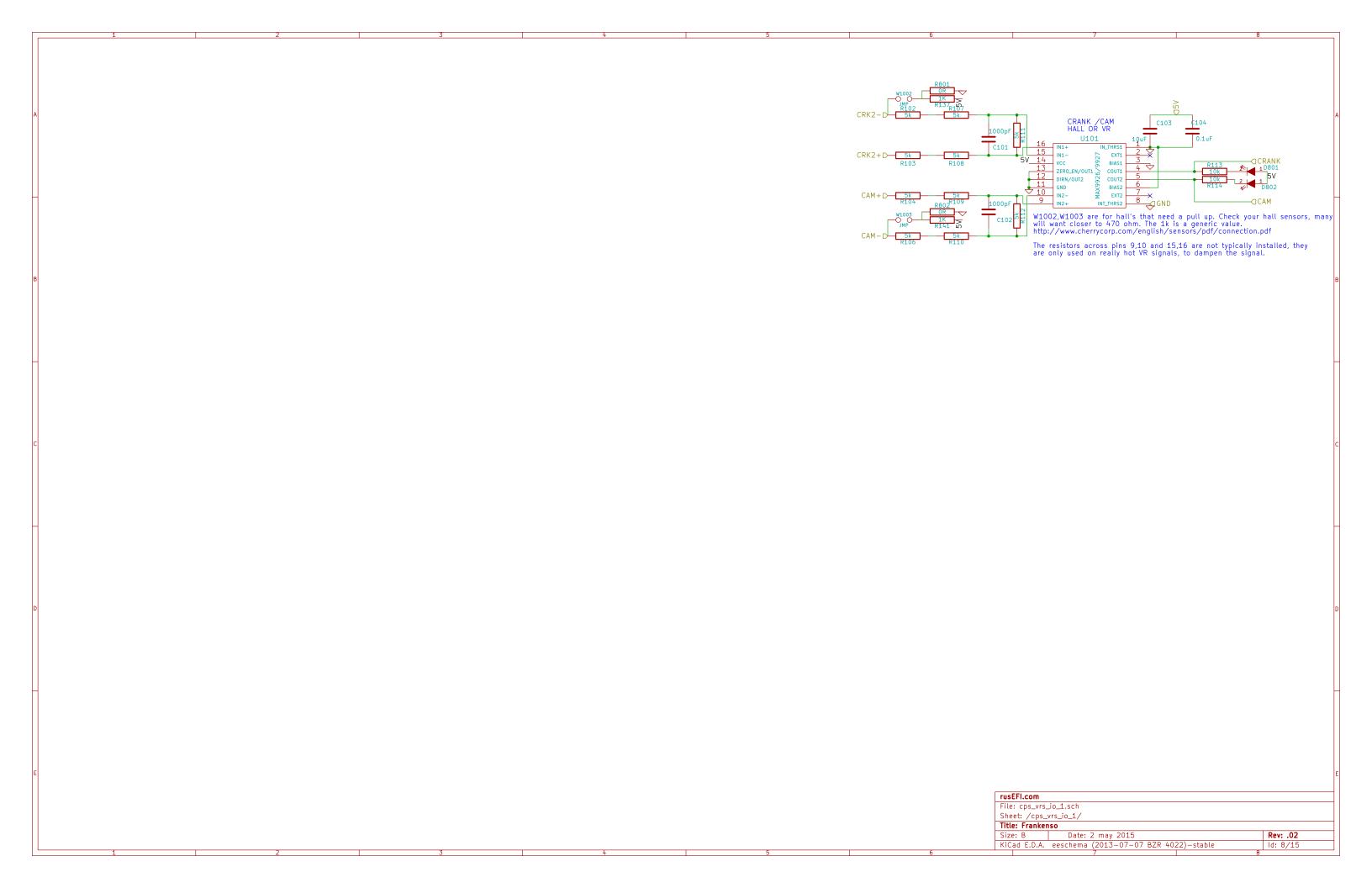
rustfi.com		
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Size: A4	Date: 2 may 2015	Rev: .02

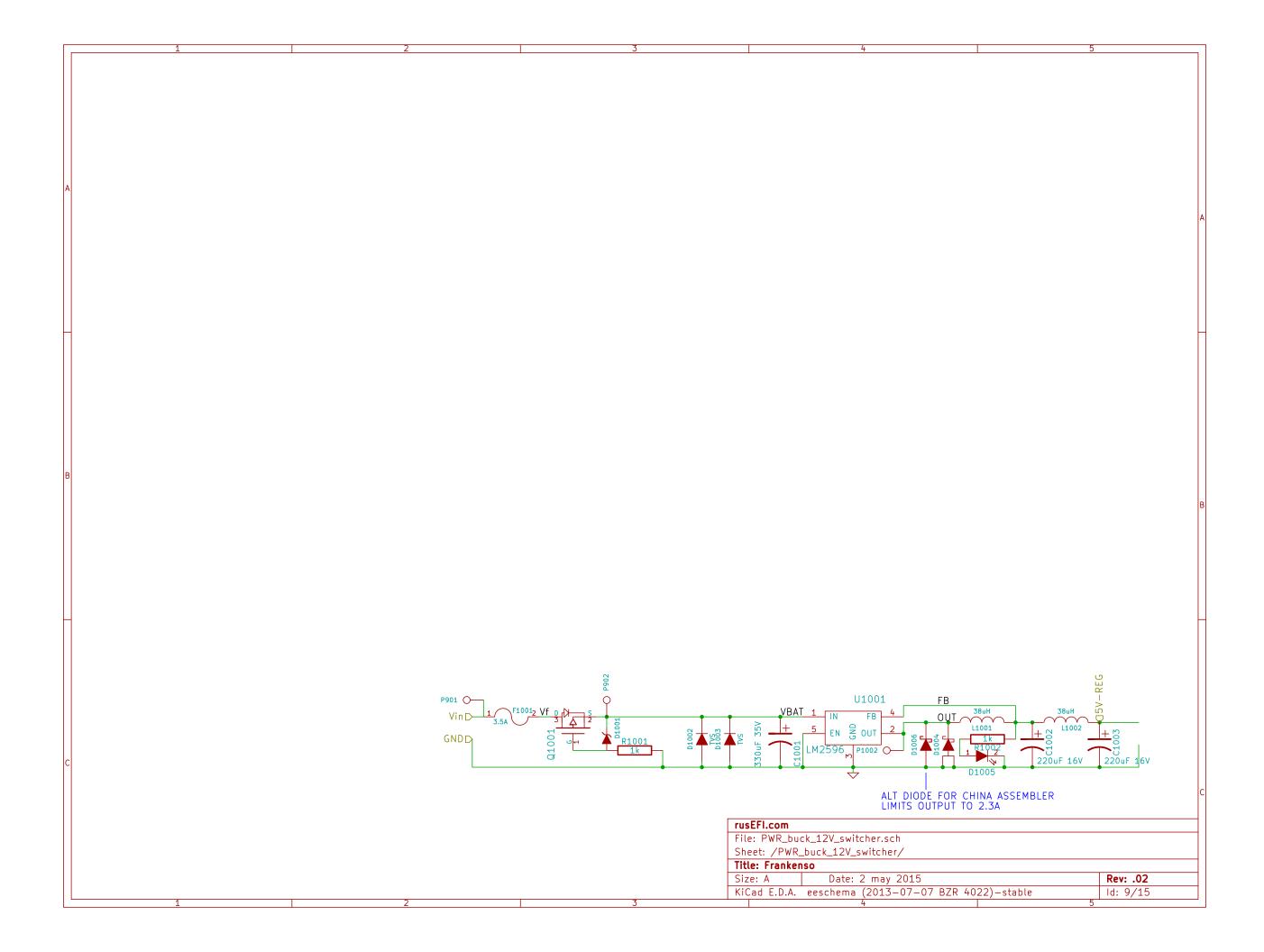
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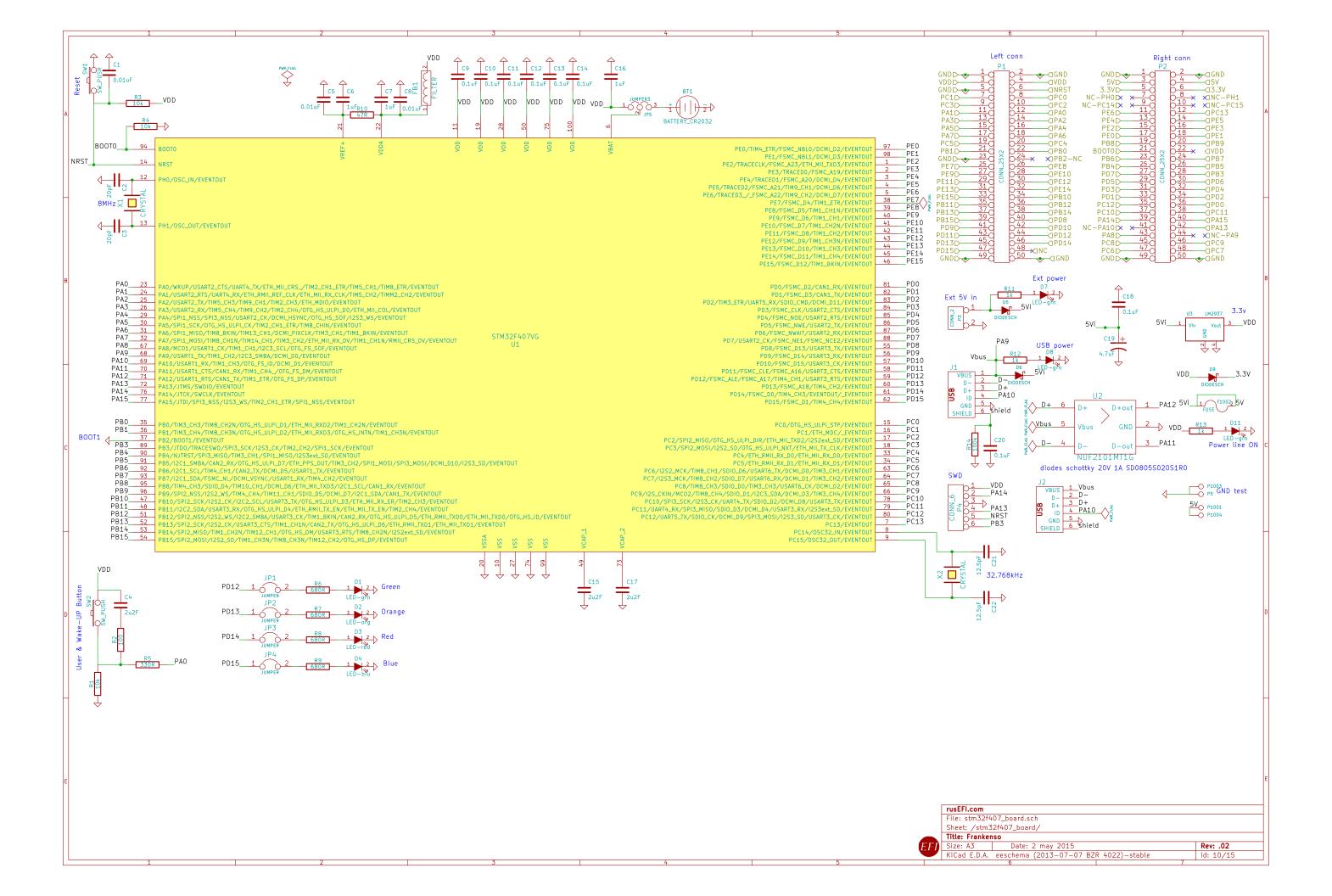
7

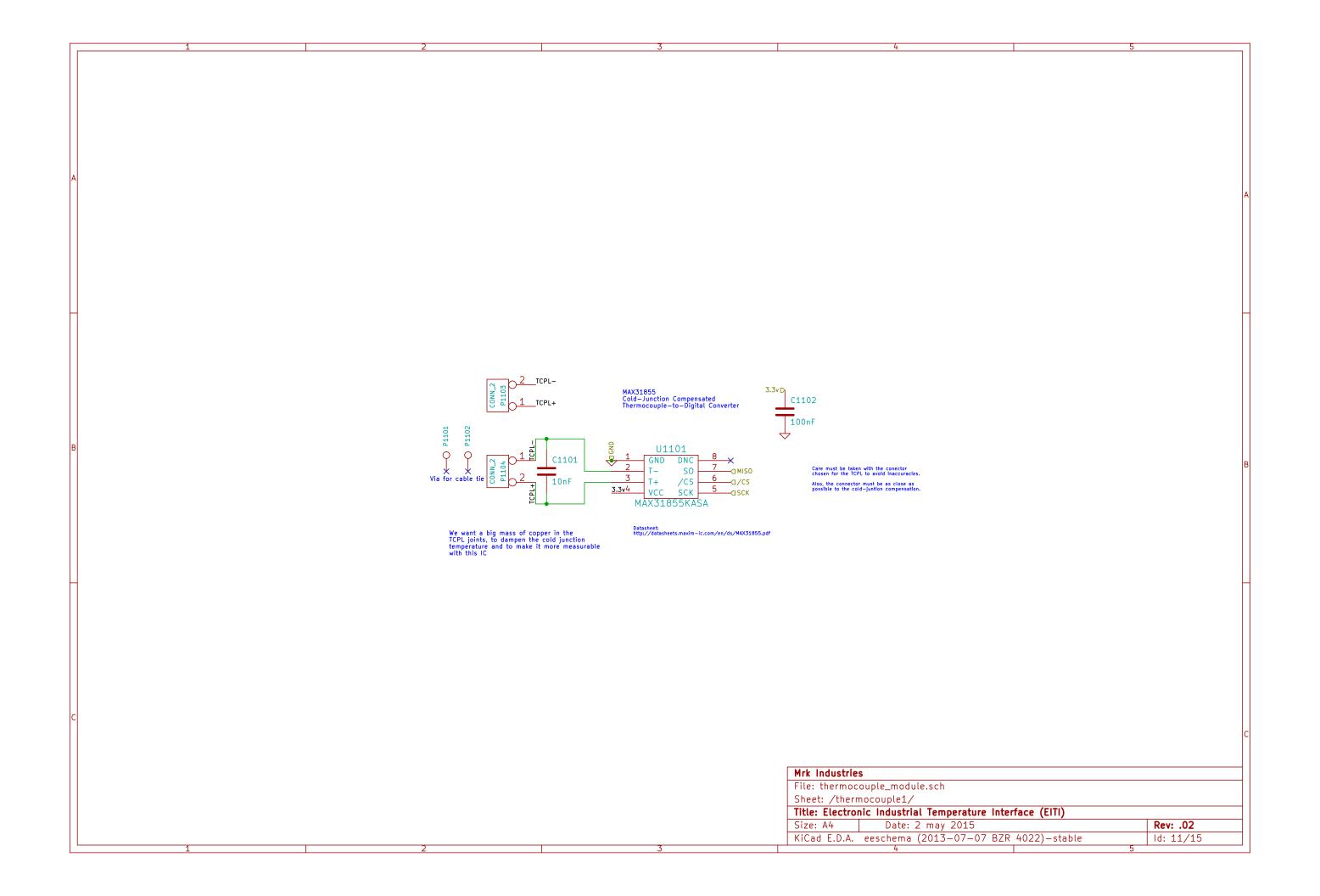


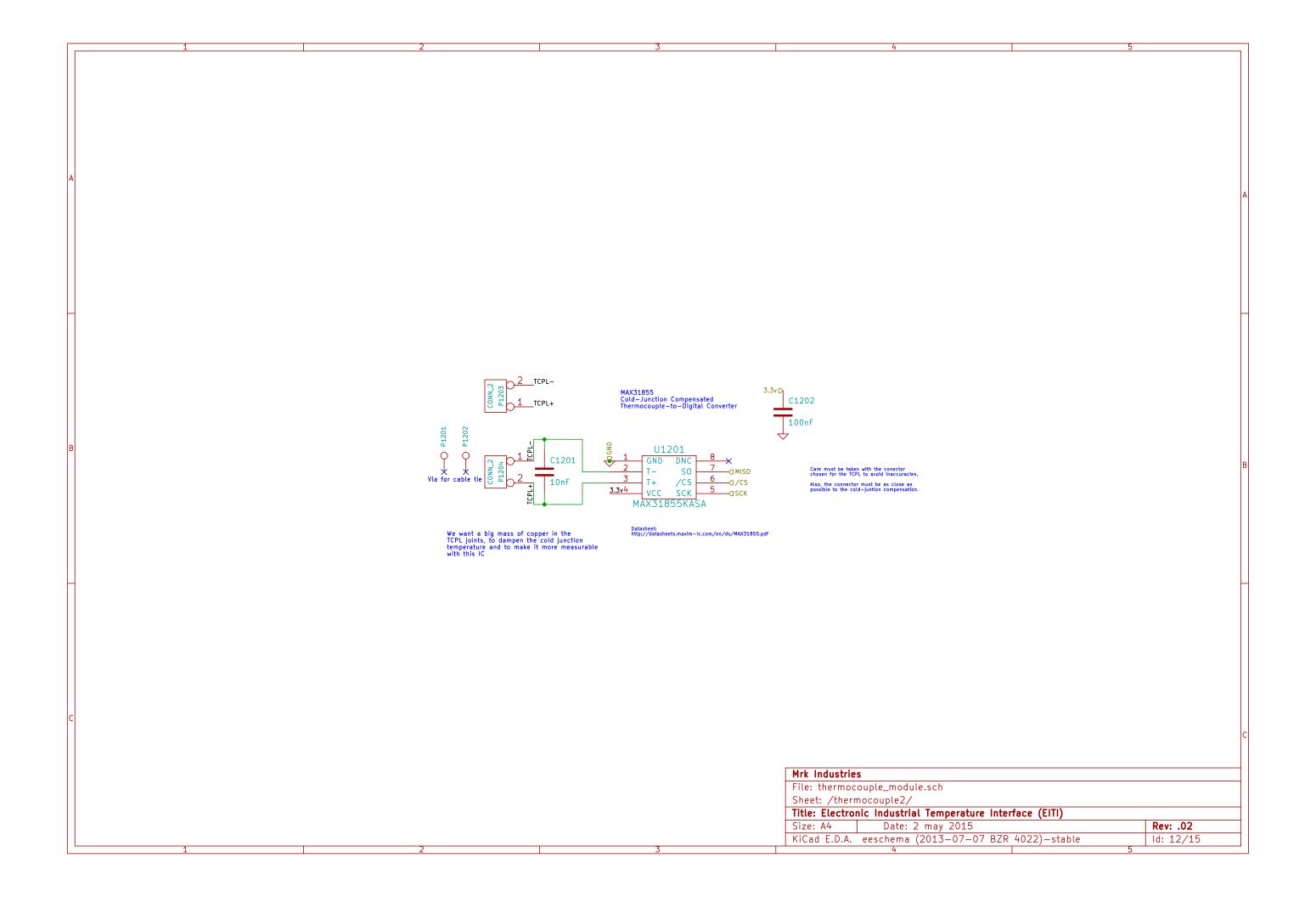
WJO1 IS A BACKUP PLAN. THE VOLTAGE DROP ACROSS D703 MAY BE NOT TOLERABLE, SO WE HAVE A BACK UP PLAN IF WE NEED TO BYPASS THE DIODE WITH A LOWER VOLTAGE DROP U351 C702 ──USART_TX ──USART_RX RXD 16 USBD-15 USBD+ SHIELD 6 Shield RESET 19 RESET 4700pF × 27 × 28 OSCO CBUS1 C351 13 CB2 2 1 14 D702LED-grn CBUS2 CBUS3 3V30UT CBUS4 0.1uF C356 RESET____RI FT232RL For right conn — GCS_SD_MODULE — GSPI_MOSI — G3.3V Vdd - ☐SPI_SCK - ☐GND SCLK DO -√SPI_MISO DATA1 CDN SD card slot USB TTL module rusEFI.com File: mmc_usb_1.sch Sheet: /mmc_usb_1/ Title: Frankenso Size: A4 Date: 2 may 2015 Rev: .02 KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable ld: 7/15

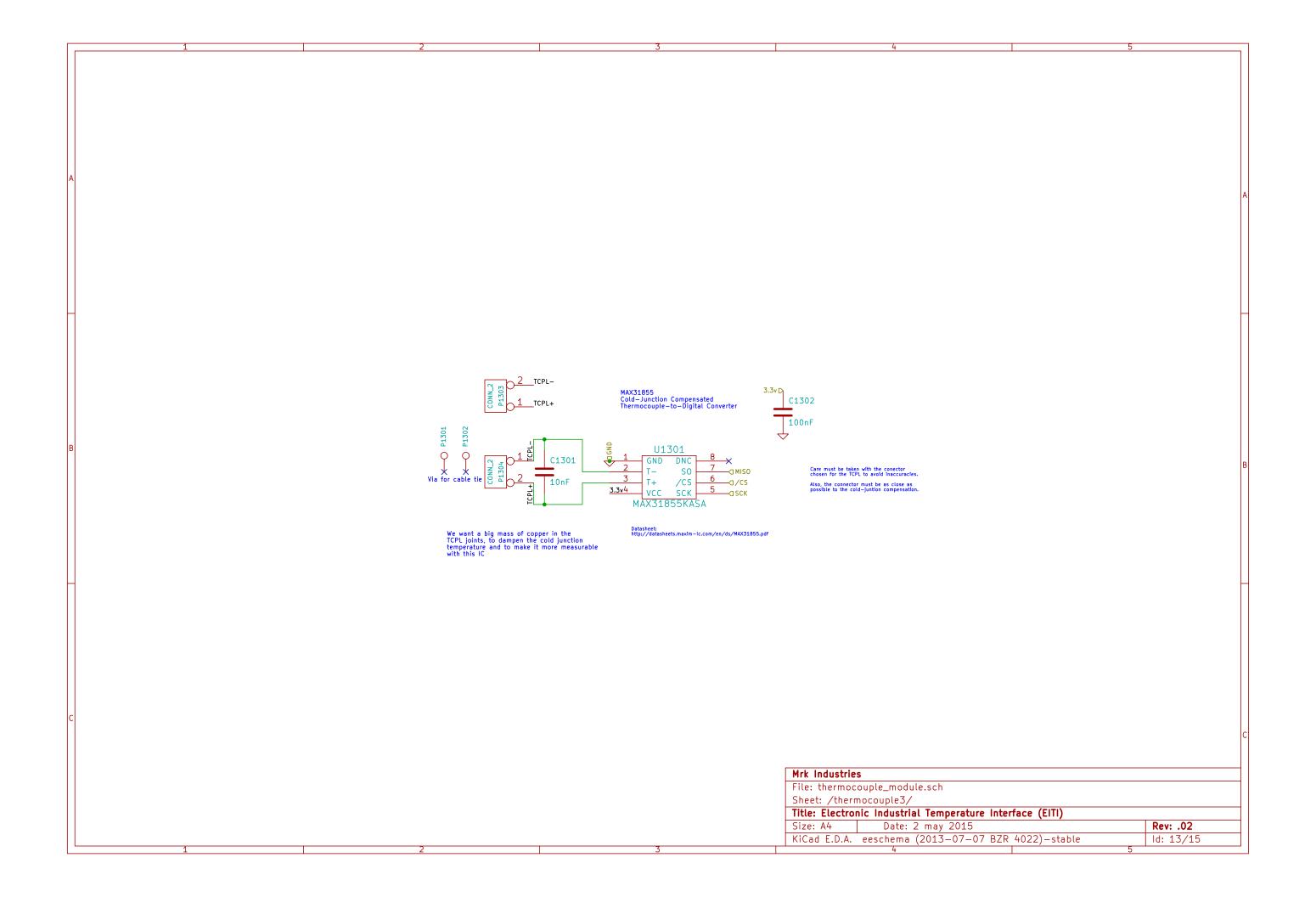


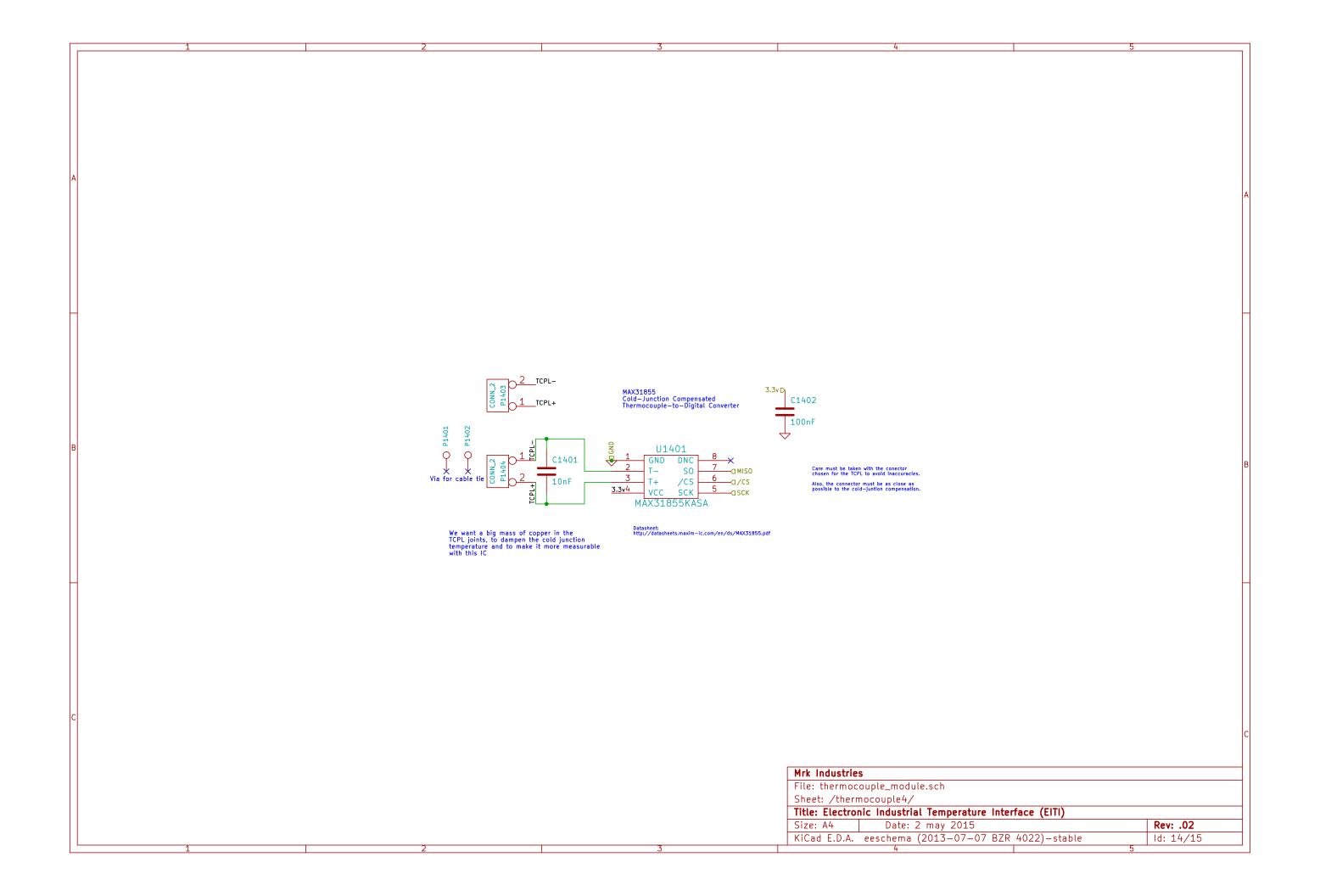


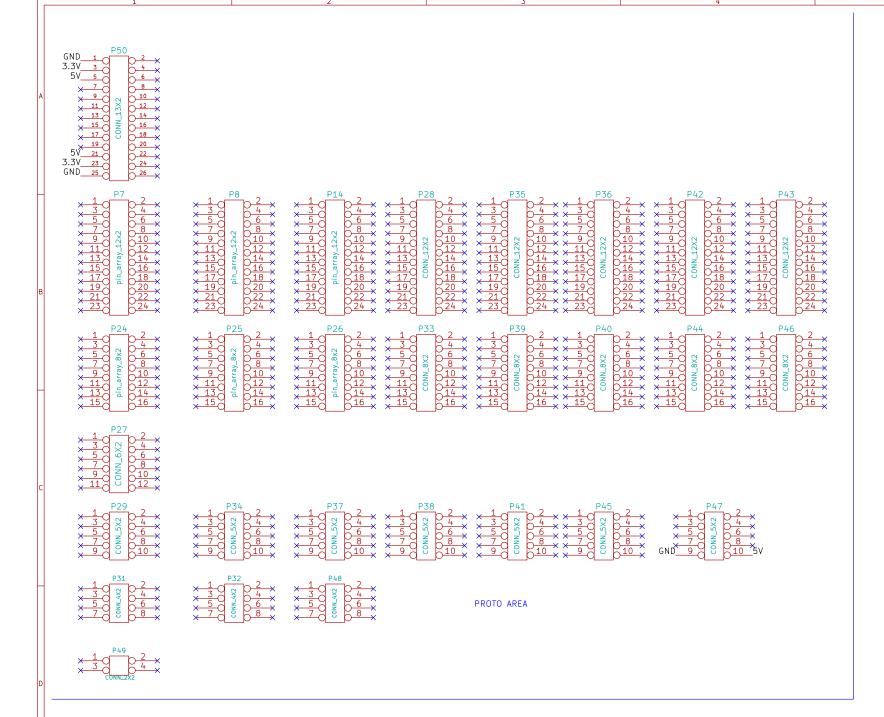












That's alternative signal OUTPUT — these traces should be routable to PC6 and PA5 via jumpers. Aleternative to W212 and W212 routung of op-amps ch 11 and ch 12

CRANKD—O

rusEFI.com		
File: Misc_Via	es.sch	
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Size: B	Date: 2 may 2015	Rev: .04
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