

## **Bi-Di buffer (vsdbidi) spec sheet for 180nm tech node**

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- **Please contact Kunal at [kunalpghosh@gmail.com](mailto:kunalpghosh@gmail.com) in case of any doubts**

# OSU 180nm-6 Metal Layer

IO_CELL name	Pin names	Direction	Values
vsdbidi(13440 um2)	A	I	
	EN	I	
Bi-directional Buffer with Non-Inverting CMOS Input and Gated Pull-down and Pull-up, Strength 4mA @ 3.3V, Normal, High noise (Fast speed)	GNDO	I	VSS
	GNDR	I	VSS
	PAD	IO	
	PDEN	I	
	PI	I	
	PO	O	
	PUEN	I	
	VDD	I	VDD1V8
	VDDO	I	VDD3V3
	VDDR	I	VDD3V3
	Y	O	

INPUTS					Bi-Dir	OUTPUTS	
A	EN	PDEN	PI	PUEN	PAD	PO	Y
Input Path (PAD --> Y --> core)							
X	1	X	X	X	0	1	0
X	1	X	0	X	1	1	1
X	1	X	1	X	1	0	1
PAD --> high-impedence							
X	1	1	1	1	Z	X	X
X	1	1	0	1	Z	1	X
X	1	0	X	1	Z	1	0
X	1	1	0	0	Z	1	1
X	1	1	1	0	Z	0	1
Output Path (core --> A --> PAD) when EN = 0							
X	1	-	-	-	Z	-	X
0	0	-	-	-	0	-	0
1	0	-	-	-	1	-	1