The Xilinx PicoBlaze Microcontroller

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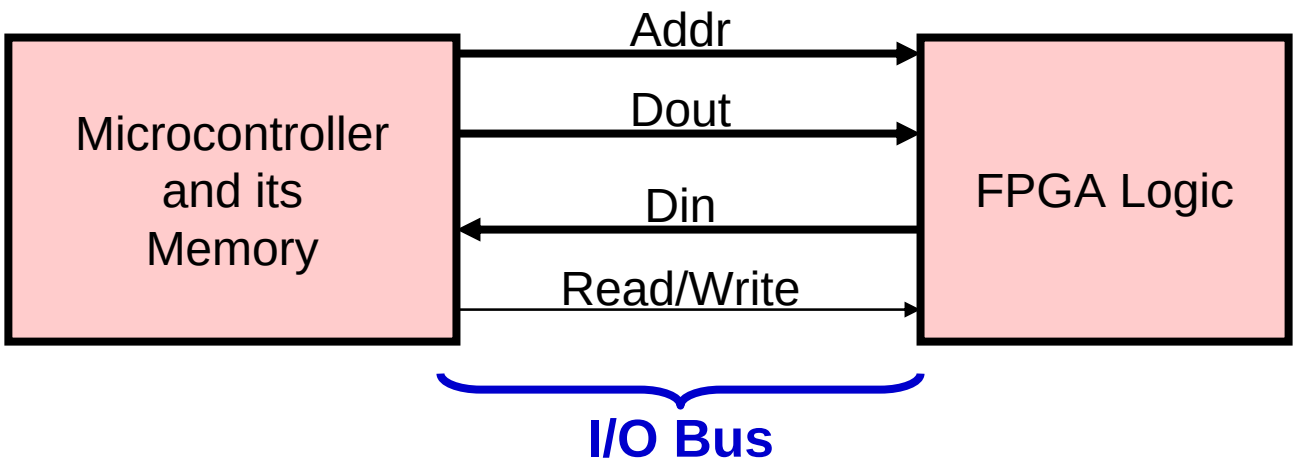
Microcontrollers in HW-Based Systems

- **Don't always need the speed of custom HW**
- **Lots of sequential control is hard in HW**
  - Easier using SW
  - If performance allows using SW, do it
- **Reads and writes on bus**
  - Decode them, read/write registers inside FPGA logic in response…



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Microcontroller Vs. Logic CoDesign Tradeoffs

	PicoBlaze Microcontroller	FPGA Logic
Strengths	• Easy to program, excellent for control and state machine applications • Resource requirements remain constant with increasing complexity • Re-uses logic resources, excellent for lower-performance functions	• Significantly higher performance • Excellent at parallel operations • Sequential vs. parallel implementation trade-offs optimize performance or cost • Fast response to multiple, simultaneous inputs
Weaknesses	• Executes sequentially • Performance degrades with increasing complexity • Program memory requirements increase with increasing complexity • Slower response to simultaneous inputs	• Control and state machine applications more difficult to program • Logic resources grow with increasing complexity

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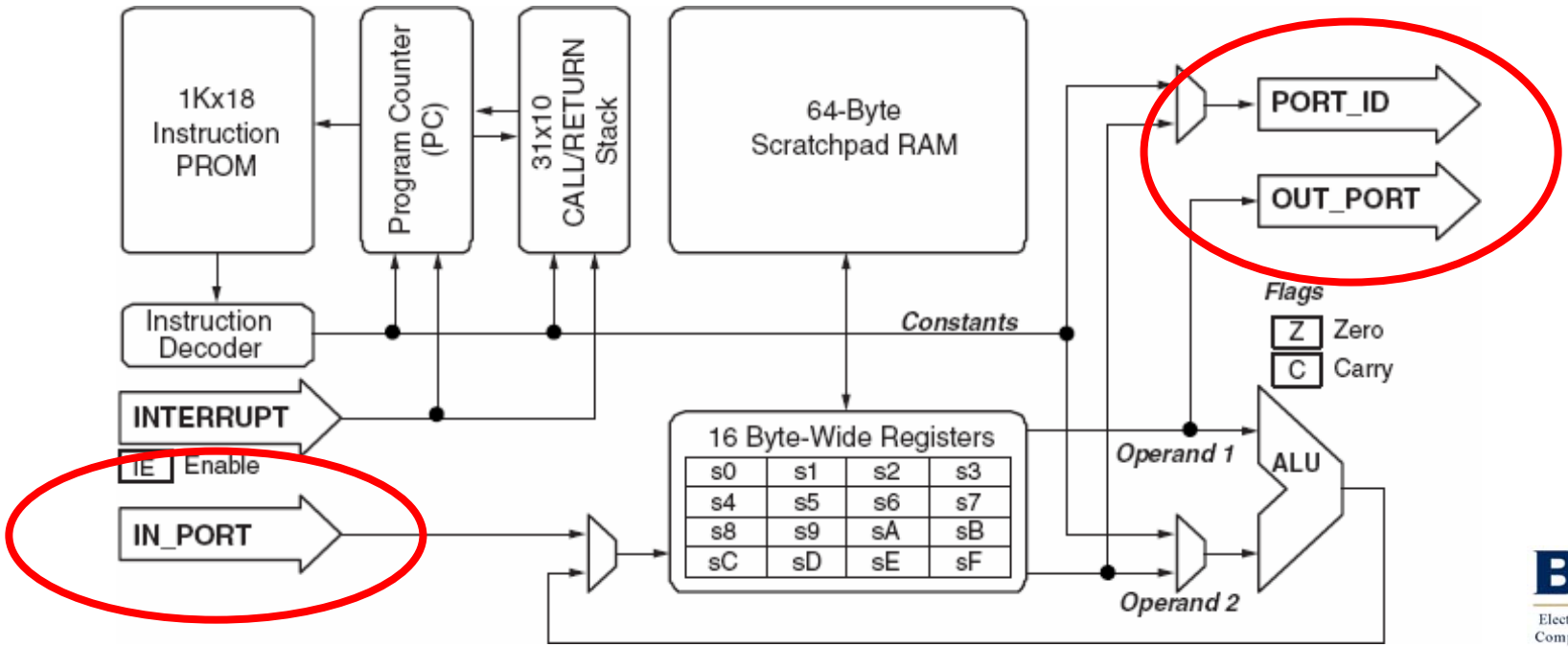
PicoBlaze Architecture Features

- **Program memory = 1024 18-bit instructions**
- **Register file = 16 8-bit general-purpose registers**
- **Flags = Zero and Carry**
- **Scratch-pad Memory = 64 8-bit locations**
- **Call/Return Stack = 31 entries deep**
- **I/O port = 8-bit data, 8-bit address**
- **Timing = 2 clock cycles per instruction**
- **Interrupt Response = 5 clock cycles**



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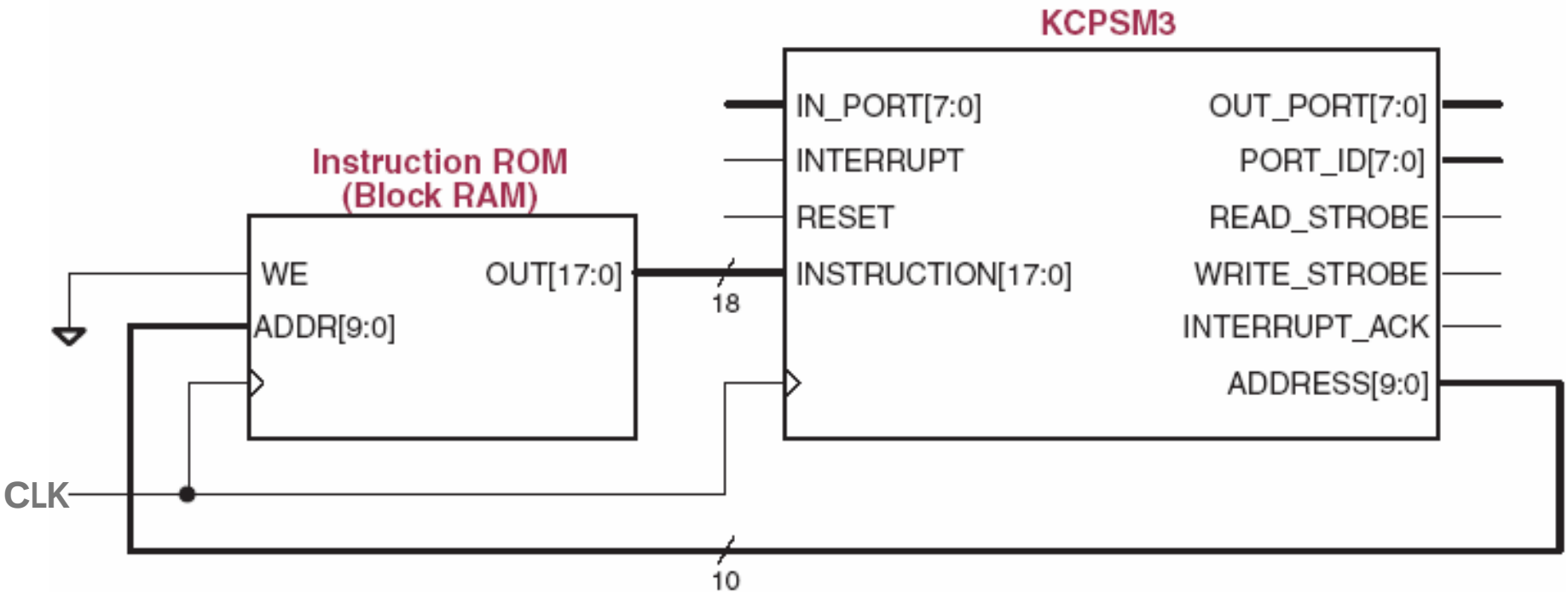
PicoBlaze + Program Memory



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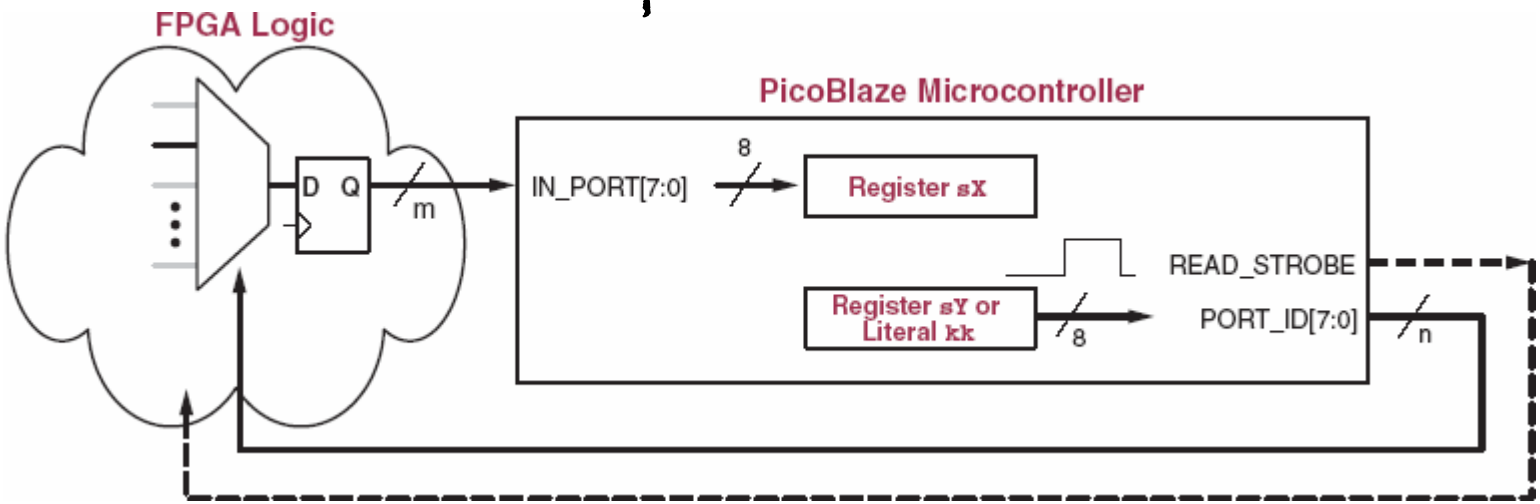
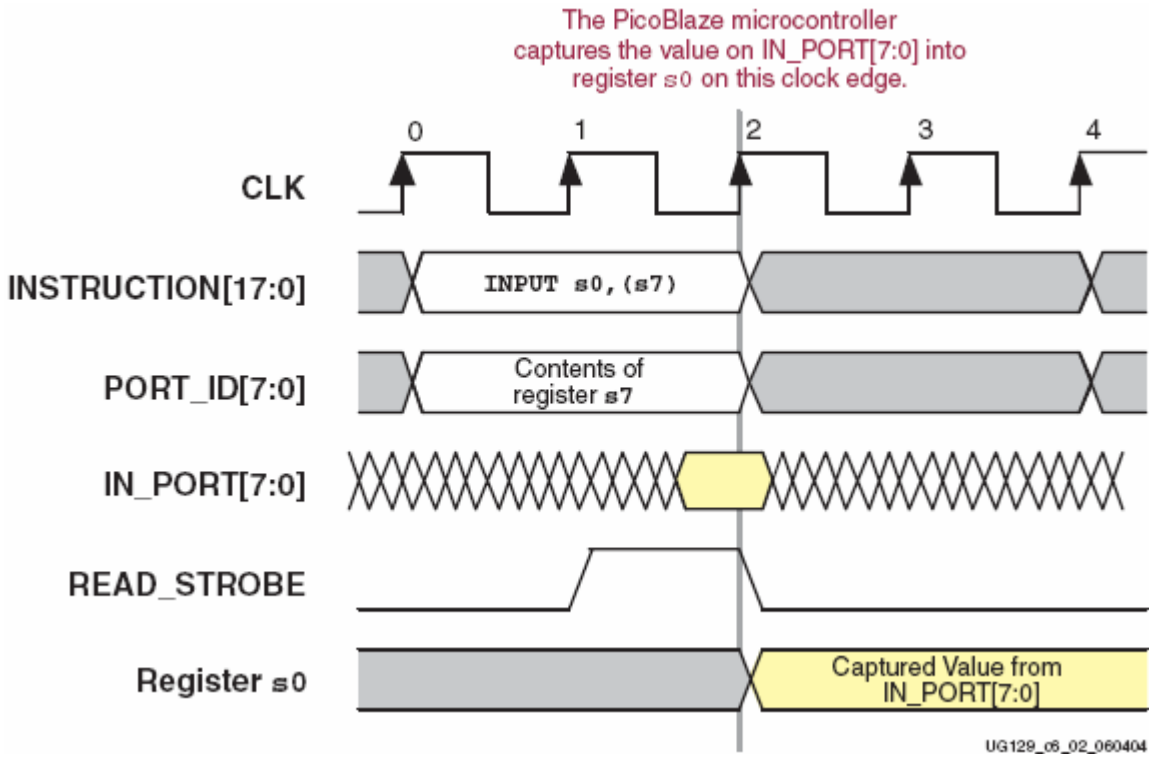
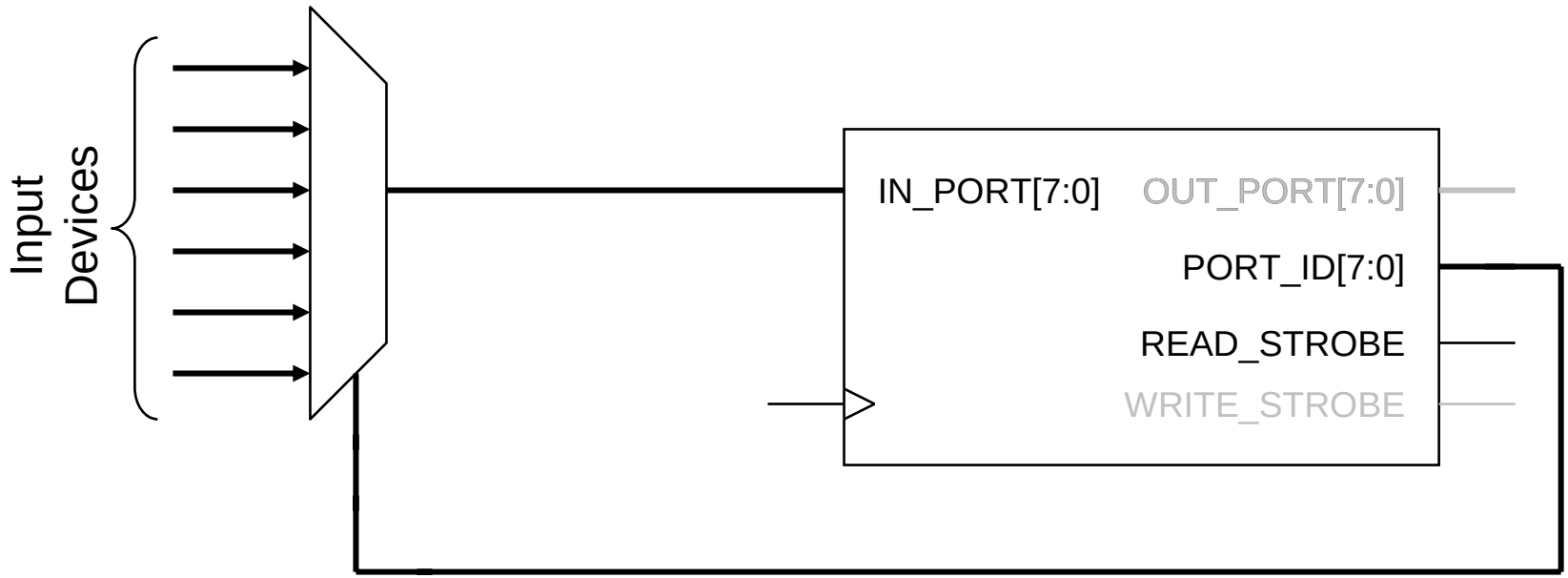
Input Port


FPGA Logic
D
Q
m
PicoBlaze Microcontroller
IN_PORT[7:0]
8
Register sX
READ_STROBE
Register sY or
Literal kk
8
PORT_ID[7:0]
n


The PicoBlaze microcontroller
captures the value on IN_PORT[7:0] into
register s0 on this clock edge.
0
1
2
3
4
CLK
INSTRUCTION[17:0]
INPUT s0,(s7)
PORT_ID[7:0]
Contents of
register s7
IN_PORT[7:0]
READ_STROBE
Register s0
Captured Value from
IN_PORT[7:0]
UG129_c6_02_060404

Input Port Decoding

MUX selects which device's signals are fed into IN_PORT



READ_STROBE can be used to indicate that something has been read…

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Use of READ_STROBE

- **Some devices <u>don't</u> care when you read them…**
  - Switches
  - No need to even look at READ_STROBE
- **Some devices <u>do</u> care when you read them…**
  - FIFO
  - Use READ_STROBE to indicate when a data value has been consumed so it can be removed

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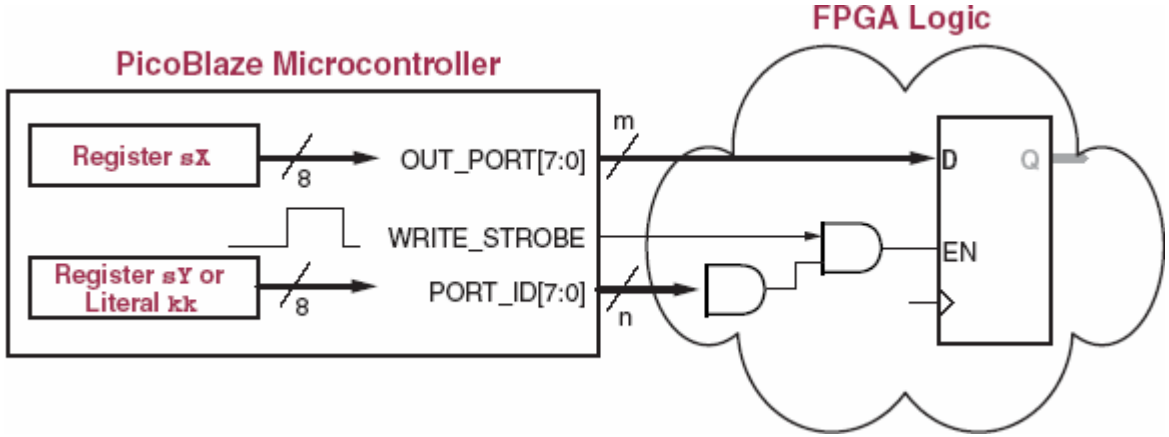
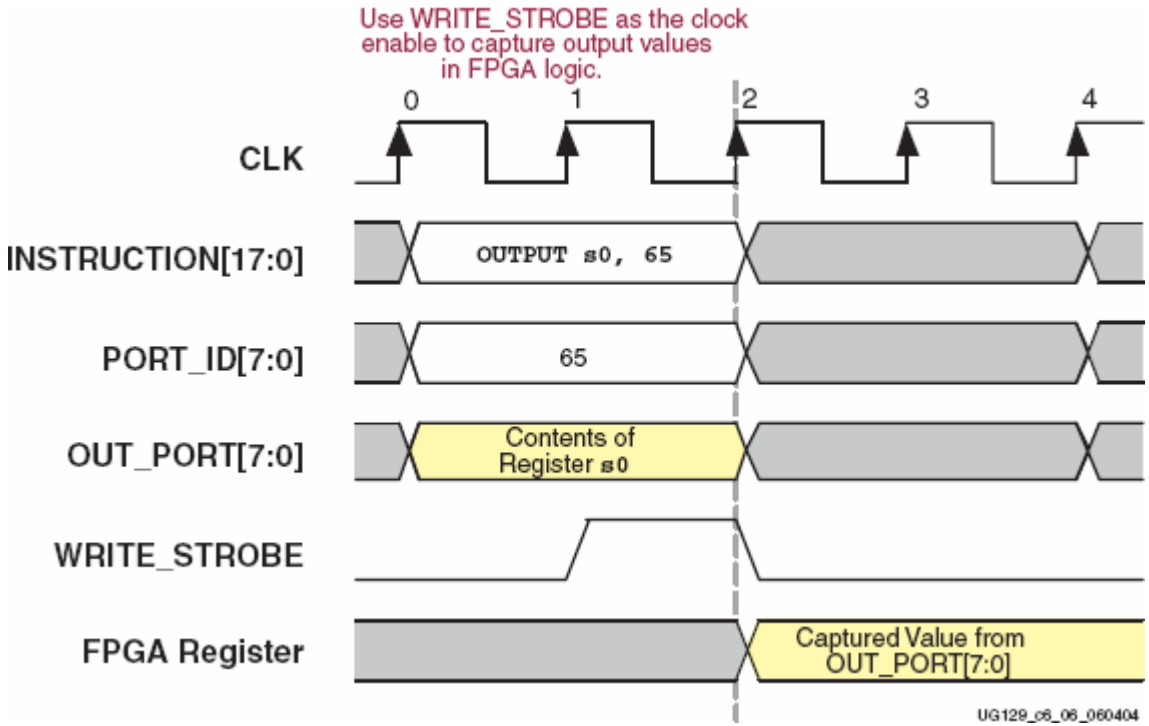
Output Port


FPGA Logic
PicoBlaze Microcontroller
Register sX
8
OUT_PORT[7:0]
m
WRITE_STROBE
Register sY or Literal kk
8
PORT_ID[7:0]
n
D
Q
EN


Use WRITE_STROBE as the clock enable to capture output values in FPGA logic.
0
1
2
3
4
CLK
INSTRUCTION[17:0]
OUTPUT s0, 65
PORT_ID[7:0]
65
OUT_PORT[7:0]
Contents of Register s0
WRITE_STROBE
FPGA Register
Captured Value from OUT_PORT[7:0]
UG129_c6_06_060404

How to Use a PicoBlaze

- **Insert PicoBlaze and its memory into design**
- **Insert FPGA logic into design**
  - Registers
  - UART
  - FIFO's
  - …
- **Create logic to decode bus and control FPGA**
- **Create logic to decode bus and have FPGA respond**
- **Program the PicoBlaze with a program**

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Going Forward

- **There is lots of PicoBlaze documentation available**
  - Go to Xilinx and look for it
- **We are *not* going to focus on programming the PicoBlaze**
  - We are going to use canned PicoBlaze designs + programs to drive our hardware designs
  - If you want to learn to program it, can do on your own

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