Future Computing with the Rogues Gallery

VIP Team Advisors: Dr. Jeffrey Young (CoC) & Dr. Jason Riedy (CoC)

Project Goals:

We are looking to design tools, software interfaces, and demos for novel and unique hardware or “rogues” that will be important for future computer systems.

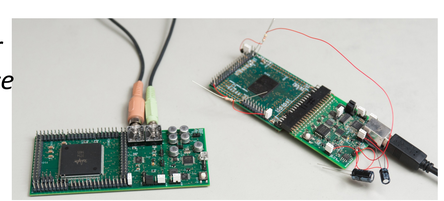
Project Overview:

Computing is changing - energy constraints and performance bottlenecks create new opportunities for *unique* and *novel* hardware designs. However, these new systems require new approaches for application development, management, and visualization.

Our teams are working in the following areas:

1) **Neuromorphic** or “brain-inspired” computing that can perform machine learning tasks with very little power
2) **Reconfigurable computing** for flexible accelerators that can be customized for a specific task
3) **Quantum computing** which does computation using qubits and superposition of electron/photon states rather than semiconductors
4) **Near-memory computing** using novel architectures like the Emu Chick to move computation to data, instead of using traditional data caching techniques.

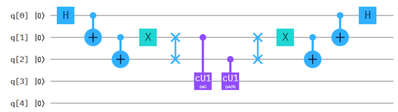
Right: The low-power FPAA prototype device used for ML and neuromorphic apps



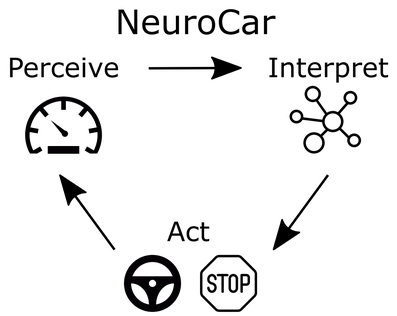
What Are Our Students Working On?

(In Their Own Words)

Quantum: We are working with the XACC quantum compiler to create a solution for the issue of qubit allocation at the compiler level. We are visualizing the coupling graph for quantum circuits, building and using the Linear Systems Algorithm to test our solution, and utilizing the IBM Q experience to build our quantum circuits.



Above: Output from IBM’s quantum circuit composer

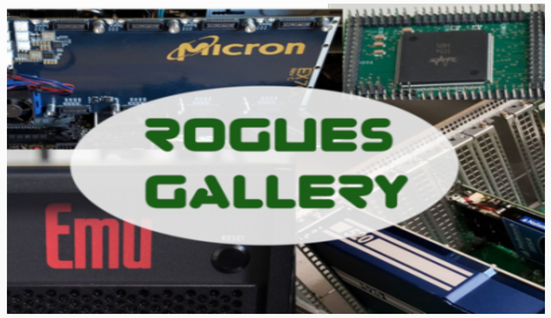


Right: NeuroCar’s ML-inspired workflow

Neuromorphic: Currently, the Neuro Team is working on an autonomous vehicle called NeuroCar, which utilizes brain-inspired spiking neural networks and software like ROS and Gazebo to power its computer vision and machine-learning-based decision-making capabilities. The team’s eventual goal is to create a physical prototype and test it on the Georgia Tech Autonomous Racing Facility.

Left: A typical desktop and reconfigurable FPGA board like those used in this course

Reconfigurable: Our team is about challenging conventional hardware design and finding new competitive methodologies that can seamlessly integrate into current standards. We are currently working on a no-history branch predictor that "sorts" the register file on-the-fly to assist with branch prediction.



Majors

CS, CM, ECE, and ME are all welcome as well as anyone with an interest in working with novel technologies.

Skills and Interests Needed

- *C or Python, git, and Linux familiarity are highly recommended*
- Machine learning experience with Scikit, PyTorch, or Tensorflow
- FPGA/FPAA programming (ECE 3400)
- High-performance computing (HPC)
- High-performance data analysis (HPDA)
- High-level languages like Julia and OpenCL
- Internet of Things (IoT), physical sensors, and embedded systems
- Power monitoring
- Workflow design

Contact Information

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