FC with RG – Reconfiguration Subteam (Spring 2024)

Brian Ok, Evan Merritt, Hansoo Kim, Ian Crombie, Kelvin Hau, Luke Dean, Manuel Thomas, Sarita Botero, Vivien Orellana

Introduction & Goals

Introduction

The Reconfiguration team investigated the use of the Chipyard ecosystem in order to develop custom hardware that we can deploy to FPGAs

Semester Goals

- Create documentation for the process of running our own modules on the cluster
- Create a Verilog implementation of the ChaCha20 Cipher and run it on the cluster FPGAs

Project Overview and Methods

Methods

- ***Chipyard***
  - A suite for writing, composing, and testing hardware
- ***Firesim***
  - FPGA-accelerated hardware simulation
- **Chisel**
  - The language of Chipyard
- ***Verilog***
  - Wrote out a ChaCha20 Cipher Module in Verilog

Progress

Implemented a BlackBox with ChaCha20 Cipher in Chipyard with Chisel and Verilog.

```
dramsim.39.log  dramsim.9.log
dramsim.4.log   dramsim.log
dramsim.40.log  generated-src
dramsim.41.log  output
dramsim.42.log  simulator-chipyard-RocketConfig
dramsim.43.log
<e/riscv-tests/isa/rv64ui-p-simple
This emulator compiled with JTAG Remote Bitbang clien
t. To enable, use +jtag_rbb_enable=1.
Listening on port 43255
[UART] UART0 is here (stdin/stdout).
<-design/chipyard/sims/verilator$
```

Experiments and Results

Verilog Blackbox

- That includes only HDL input/output port definitions for subsystem
- Can use Verilog IP for chip design flow
- Allows Chipyard modules to be written in Verilog but still leverage the capabilities of the ecosystem
- The Rocket chip allows the use of Verilog black boxes as accelerators

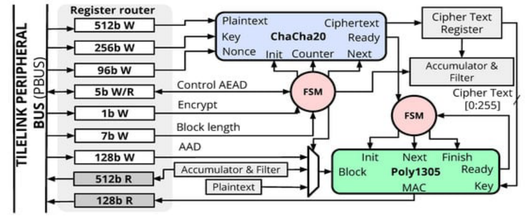
ChaCha20 Accelerator

- A encryption algorithm which is more secure than AES
- More software-friendly due to its limited set of needed operations
- Has potential for a substantial speedup through the use of a dedicated hardware accelerator
- We designed the accelerator using Verilog and plan to incorporate it into existing Chipyard projects by using Chipyard's black box feature

Firesim Container

- We got an Apptainer working to run FireSim, which is an FPGA simulator which can use hardware acceleration to simulate with real FPGAs
- We got the demo simulator running on the cluster, which simulates a basic processor with UART output
- We improved the accessibility of the container so less command line arguments are needed for our team's folder to be bound to the Apptainer environment
- We improved the documentation so it is easier to navigate the server containers and run simulations

ChaCha20 Block Diagram



Lessons learned

- **HDL**

Our team members furthered our understanding of Verilog, the industry standard HDL.

- **Virtualization**

We learned the process of using Apptainer, a lightweight and rootless virtualization technology, on the team cluster

- **Chipyard**

We learned about integration with Chipyard, a framework for RISC-V designs

Future projects

- Building specialized accelerator for:
  - PID
  - Hardware Sorting
  - Multimedia Encoding/Decoding
- Integrate our current ChaCha20 accelerator with the Rogues Gallery cluster to explore real world performance
- Create an interface between our existing hardware design and pre-existing RISC-V cores
- Explore FPGA-specific acceleration