FC with RG – Reconfiguration subteam (Fall 2023)

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Introduction & Goals

Introduction

The Reconfig team focused on hardware based technology and worked on topics from Chisel which is a hardware description language (HDL) to using Chisel to implement RISC-V hardware within the cluster

Semester Goals

- Create documentation for an easier setup of Chisel for future VIP students
- Research RISC-V architecture and how we can implement it within our projects
- Set up Docker containers to run in our cluster

Project Overview and Methods

Methods

- To build a container the method followed began creating a docker image to make a CHISEL environment.
- The Apptainer Definition file, also known as a "def file," details regarding the basic container to start from or it include specifics about the base OS to build.

Result

- Created Docker image for CHISEL.

```
[hkim3190@frozone1 chisel_project_f23]$ ls
build.sbt   hsdocker.     hsdocker.sif  riscv-mini
Dockerfile  hsdocker.def  lolcow.sif    ubuntu
[hkim3190@frozone1 chisel_project_f23]$ salloc -prg-gpu -wfrozone1
salloc: Pending job allocation 67110600
salloc: job 67110600 queued and waiting for resources
salloc: job 67110600 has been allocated resources
salloc: Granted job allocation 67110600
salloc: Nodes frozone1 are ready for job
[hkim3190@frozone1 chisel_project_f23]$ apptainer run hsdocker.sif
[hkim3190@frozone1 chisel_project_f23]$ apptainer shell hsdocker.sif
Apptainer>
```

Experiments and Results

Chisel

- Hardware Design Language, used to describe digital circuits
- Can be converted into Verilog
- Allows the use of object-oriented programming
- Influenced by Scala

Docker-Container

- Containers have the benefits of a virtual machine without the overhead
- Allow for consistent and reproducible environments across personal or remote machines
- Produced an image (a container is a running image) with the necessary installations to run CHISEL
- Specifically an Apptainer image which is more scalable than the more well known Docker images
- Users must only run the image or build their own images to run from the prepared definition file
- Definition, or def, files are blueprints for creating images which include the base OS, environment settings and installations

RISC-V – RISC-V accelerators

- RISC-V is an open-source instruction set architecture used to develop processors for applications.
- It has become popular due to its simplified instructions to create custom processors.
- Chisel can be used to create RISC-V IPs.
- RISC-V accelerators are used for neural networks and convolution neural networks(CNNs).
- Would be a good bridge between accelerators and machine learning frameworks and compilers.

Lessons learned

- **HDL**

All our team members learned how to use and understand Chisel/Scala.

- **Docker**

Experienced how to use Docker to create a Chisel working container.

- **RISC-V**

For the coming steps, we also studied RISC-V structures and accelerators.

Future projects

- Implement the RISC-V 3 stage pipeline mini project.
- Build our own RISC-V accelerators using Chisel.
- Try out various projects including Chisel, FIRRTL, Strober, simulation and verification methodologies.
- Study Rocket-chip generator which is a Scala program that invokes the Chisel compiler to emit RTL describing a complete SoC.