FC with RG – Near Memory

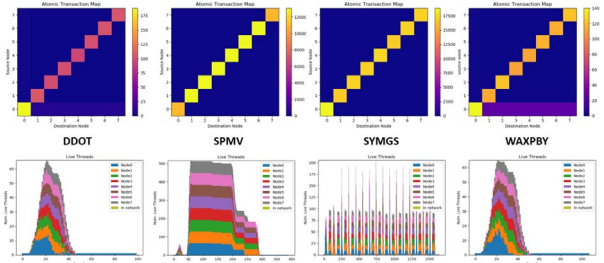
Bryson Bennett, Alexander Contratti, Charles McHenry, Marcello Palucci,
Mitchell Teunissen, Jeremy Wang, Matthew Withka, Yongnuo Yang

Goals

- Wrapping up and refining data from previous semesters' work
- Trying to run simulations based on known configuration to explore parallel computing pattern of Lucata architecture

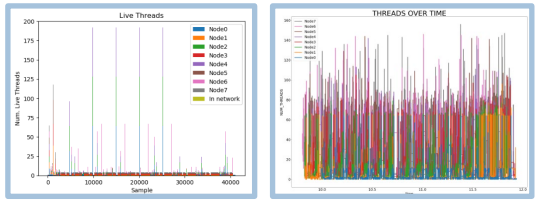
HPCG Project

- HPCG is a new metric for supercomputing that stresses irregular data accesses
- Refine profiling for four linear algebra kernels
- Healthy live threads pattern on each nodes, showing balanced workload
- Atomic transaction maps enable the local data access and minimize remote r/w across the nodes



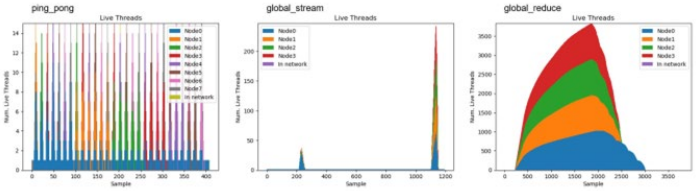
Hardware Analysis

- Observing the thread graphs in HW run (right) vs simulation run (left) shows good multi-processing and parallelization, and the maximum thread spawn is in a comparable range



Microbenchmark Project

- Small, specific piece of code to demonstrate near-memory computation.
- Well parallelized Cilk-enabled code gives good workload distribution across the nodes.
- The profiling graphs showcase how thread migration and data allocation work on a multi-node configuration



Student Experiences

- Student-led nature of the projects provided a high degree of flexibility and independence in defining project goals and working as a team
- The specificity of the content area offered exposure to various academic fields and an introduction to student research
- Technical work with the Pathfinder was especially challenging due to the product being both experimental and proprietary.
- Challenges in hardware stability, limited support, and porting developed our abilities to adapt around external limitations and intermittent hardware issues.