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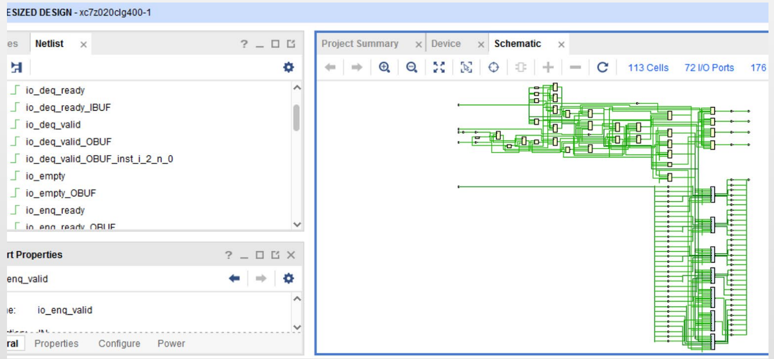
Project Goals

The goal which we laid out for ourselves this project was to learn Chisel, a high level hardware description language, and its surrounding framework. We aim to learn how to synthesize a circuit originally written in Chisel onto a PYNQ-Z2 FPGA to prepare us for creating hardware-based accelerators.

What is Chisel?

Chisel is a hardware construction language that is based off of Scala, a Java like object oriented language. As shown below, Chisel code can generate Verilog code from these descriptions via elaboration. HDLs are primarily limited to creating hardware instances - Chisel's feature of parameterization addresses this to allow creation of hardware generators.



Schematic FIFO Queue for PYNQ-Z2

Semester Progress and Results

Chisel Project

- Worked through HDLBits to have a solid foundation with Verilog and hardware description languages in general.
- All members completed basic Chisel bootcamp from GitHub.
- Prototyped basic FIFO queue in Chisel.
- Learned to compile Chisel code down to Verilog.

Lessons Learned

- FPGA basics.
- System Prototyping on FPGA.
- CLI Tools (SSH, git, objdump).
- Scala and Chisel.
- Online on-demand FPGA access.

Setting up PYNQ-Z2 for RISC-V

- Installed riscv-gnu-toolchain and compiled it onto the PYNQ-Z2.
- Synthesized PicoRV32 processor and generated a bitstream for the PYNQ-Z2.

Hardware Design Flow

- Learnt how to design real life hardware systems on FPGAs, and how to progress a project through the entire design flow.
- Walked through the FPGA design process to generate a bitstream for our FIFO Queue for the PYNQ-Z2 board.
- Looking to add overlays in order to be able to interact with the design through AXI LITE protocol.

Documentation

- Created background resources that introduces FPGAs, HDLs, and Chisel for sub-team members unfamiliar with those topics
- Added documentation regarding FPGA synthesis using the FIFO Queue created in Chisel for PYNQ-Z2 on Xilinx Vivado with setup

Next Steps and Future Challenges

- Perform RTL simulation on the synthesised circuit.
- Compare to Verilog implementation.
- Learn entire FPGA design flow using Vivado.
- Benchmark critical path latency using synthetic benchmark.
- Create and design a matrix multiplication accelerator using ChipYard and Chisel.