FC with RG – Reconfigurable Computing

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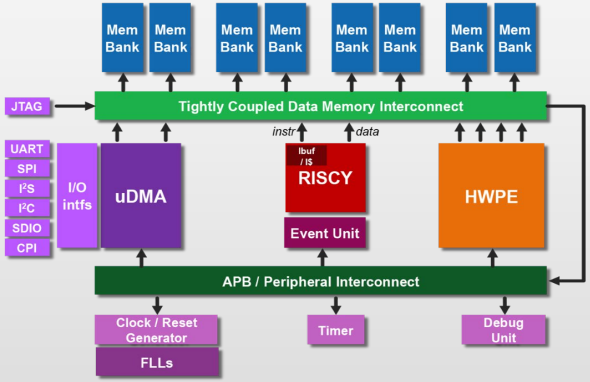
Project Goals

A drone has three fundamental modules: compute, flight controller, and electronic speed controller. Our goal is to accelerate the drone's PU via the compute module using a PULP RISC-V architecture on a PYNQ-Z2 FPGA.

What is open-source hardware?

As opposed to proprietary HW designs, open-source hardware are microarchitecture designs and IP that are available for the public to implement. We used the **pulpissimo** architecture created by the PULP (Parallel Ultra Low Power) platform.



Experiments and Results

Toolchain Preparation

- Successfully set up and validated the pulp-riscv toolchain.
- Compiled local test programs.
- Toolchain primarily acts as a compiler for the pulpissimo.
- Used *objdump* to verify that compiled binaries are for the RISC-V architecture.

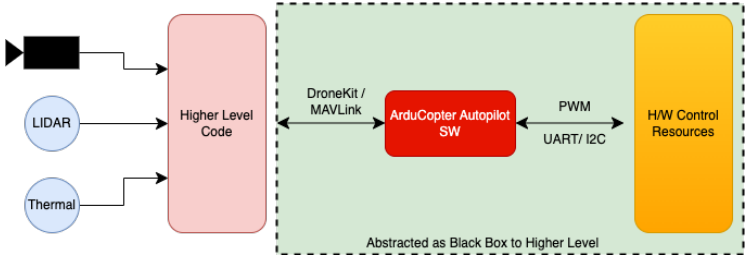
Bitstream Generation

- The HDL code for the pulpcore needs to be synthesized and compiled into a bitstream file.
- The bitstream file is necessary to program the FPGA.
- We are modifying the scripts provided by PULP to generate a bitstream for the pynq-z2.

Hardware Design Flow

- Learnt how to design real life hardware systems on FPGA's, and how to progress a project through the entire design flow.
- Explored rapid system prototyping concepts to develop our system.

Drone Flight Overview



Lessons Learned

- System Prototyping on FPGA.
- CLI Tools (SSH, git, objdump).
- Compiling for RISC-V using the RISC-V toolchain and PULP.

Next Steps and Future Challenges

- Create drone controller program for pulpissimo.
- Perform RTL simulation of pulpissimo.
- Run power and area analysis.
- Benchmark critical path latency using synthetic benchmark.