Back-side Delivery Networks with Integrated Voltage Regulator

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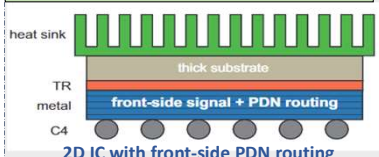
Motivations & Objectives

- Develop BS-PDN EDA flow;
- Address PDN challenges;
- Enable Back-side DC-DC unit converter (BS-UC) for BS-PDN.

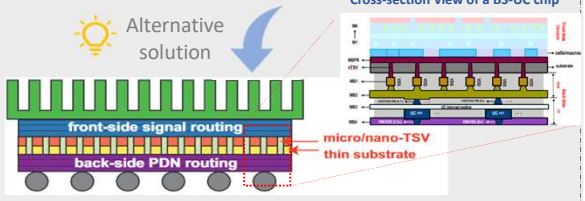
An overview of FS- and BS-PDN



Challenges:
1. High power density;
2. Voltage drop;
3. Congestion…

2D IC with front-side PDN routing

Alternative solution



Cross-section view of a BS-UC chip

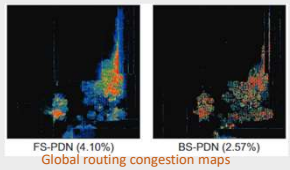
2D IC with back-side PDN routing

Recent Results

- Design implementation (Benchmark: OpenPiton)
  - BS-PDN → shorter wirelength (-14%) → less congestion.

	FS-PDN	BS-PDN	Δ
Footprint (mm²)	0.13		-
Metal stack	6M	6M+2MB	-
Rail pitch (CPP)	32	3	(-90.6%)
# Cells	317061	307123	(-3.1%)
Area Utilization (%)	71.12%	77.05%	(+8.3%)
WL (m)	1.52	1.30	(-14.3%)
PDN area (mm²)	0.15	0.21	(+39.0%)
Fmax (GHz)	0.97	1.05	(+8.2%)
Total power (mW)	92.4	85.9	(-7.0%)
Static IR-drop (mV)	69.3	33.7	(-51.4%)

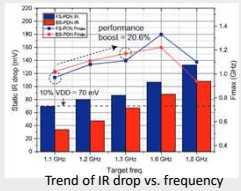
Routing wirelength distribution



Global routing congestion maps

FS-PDN vs. BS-PDN

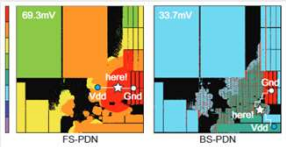
- PPA comparisons:
  - Timing improvement (+8.2%);
  - Power saving (-7.0%);
  - Cell area increase (+8.2%).
- Static IR drop analysis:
  - IR drop reduction (-51%);
  - Performance boost (20.6%).



Trend of IR drop vs. frequency

	FS-PDN	BS-PDN	Δ(%)
Type			
Internal (mW)	61.5	59.2	-3.7%
Switching (mW)	30.6	26.5	-13.4%
Leakage (mW)	0.3	0.3	-3.6%
Component			
Memory (mW)	36.5	35.4	-3.0%
Clock (mW)	13.4	12.5	-6.7%
Sequential (mW)	11.8	11.4	-3.4%
Combinational (mW)	30.8	26.5	-14.0%
Total (mW)	92.4	86.0	-6.9%

Power consumption breakdown



Static IR drop map

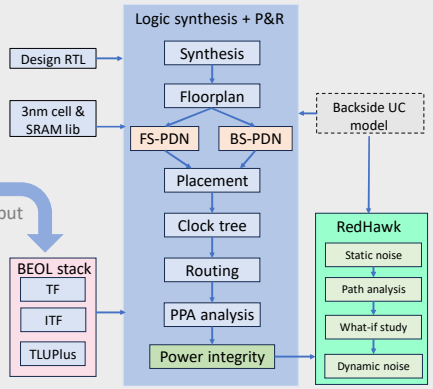
Technical Approach

- Technology setup: Based on in-house 3nm PDK.

Metals				
	Group	Layer	Width (nm)	Resistivity (Ω/um)
back-side	MB	MB2-MB1	40	34
	BPR	MBPR	25	65
front-side	Mx	M1-M3	12	347
	My	M4-M5	18	101
	Mz	M6-M7	24	44

Vias				
	Size (um)	Pitch (um)	Resistance (Ohm)	KOZ (um)
micro-TSV	1.00	5.00	0.29	2 x 2
MB via	0.020	0.012	56.0	-
Mx via	0.012	0.024	63.5	-
My via	0.018	0.036	19.3	-
Mz via	0.024	0.048	10.8	-

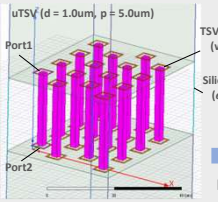
Technology setup for 3nm PDK



Design and analysis flow

- Design flow development:
  - Commercial tools and customized scripts;
  - Pattern-based PDN design;
  - Detailed IR-drop analysis, etc.

- TSV and BS-PDN modeling:
  - Based on Ansys HFSS and RedHawk;
  - Physical model → electrical model → tech file → full chip simulation.



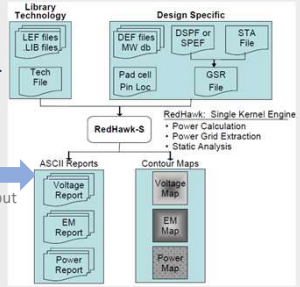
TSV array model

Extract

	nano-TSV	micro-TSV
Diameter (um)	0.06	1.0
KoZ width (um)	0.12	2.0
Pitch (um)	0.5	5.0
Length (um)	0.6	10.0
R (Ohm)	3.81	0.29
L (pH)	0.72	6.25
C (fF)	0.27	7.59

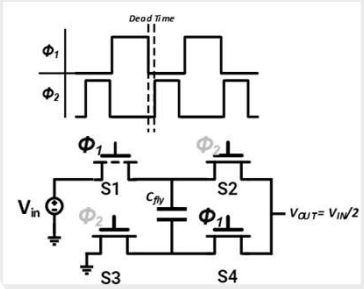
TSV lumped parasitics

Input

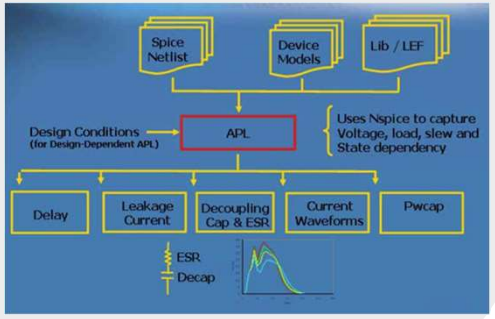


Ansys RedHawk full-chip simulation flow [1]

- BS-UC design and modeling:
  - Using SPICE simulation and cell characterization;
  - Key output: transient response, current switching behavior.

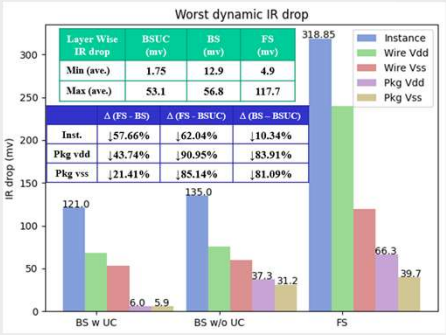


DC-DC converter circuit and schematic [5]



Characterization flow [1]

BS-UC benefits



Layer Wise IR drop	BSUC (mv)	BS (mv)	FS (mv)
Min (ave.)	1.75	12.9	4.9
Max (ave.)	53.1	56.8	117.7

	Δ (FS - BS)	Δ (FS - BSUC)	Δ (BS - BSUC)
Inst.	↓57.66%	↓62.04%	↓10.34%
Pkg vdd	↓43.74%	↓90.95%	↓83.91%
Pkg vss	↓21.41%	↓85.14%	↓81.09%

- BS-UC can mitigate 10.34% worst instance IR-drop compared to backside without UC.
- BS-UC can mitigate more than 80% IR drop from pkg.
- BS-UC reduce the overall IR drop for all instance (min layer wise drop) because pkg IR drop propagates to every layer.

Comparison with the SOTA

Reference	Strength	Weakness
[2]	Enabled BS-PDN for a 2D commercial CPU design.	Have not considered impacts of BS-PDN on design PPA, have not included BS-UC.
[3]	Enabled BS-PDN for a 3D IC design.	
[4]	Enabled BS-PDN for both 2D and 3D ICs at A14 node.	
This study	Enabled BS-PDN, performed detailed PPA and IR drop analysis.	BS-UC is not yet included.

Key accomplishment

- Implemented an EDA flow for BS-PDN design & analysis:
  - Highly configurable;
  - BS-UC integration.
- Evaluated the benefits of BS-PDN and BS-UC in CPU design:
  - Routing congestion reduced;
  - Explainable performance and power improvements.
- Detailed IR drop analysis:
  - Identify the bottleneck for front-side power delivery;
  - DSE between performance and power integrity.

Reference

[1] Ansys, "RedHawk User Manual", 2022.
[2] Prasad, Divya, S. S. Teja Nibhanupudi, Shidhartha Das, Odysseas Zografos, Bilal Chehab, Satadru Sarkar, Rogier Baert, et al. "Buried Power Rails and Back-Side Power Grids: Arm ® CPU Power Delivery Network Design Beyond 5nm." In 2019 IEEE International Electron Devices Meeting (IEDM), 19.1.1-19.1.4. San Francisco, CA, USA: IEEE, 2019. https://doi.org/10.1109/IEDM19573.2019.8993617.
[3] Sisto, G., B. Chehab, B. Genneret, R. Baert, R. Chen, P. Weckx, J. Ryckaert, et al. "IR-Drop Analysis of Hybrid Bonded 3D-ICs with Backside Power Delivery and μ- Amp; n- TSVs." In 2021 IEEE International Interconnect Technology Conference (IITC), 1–3, 2021. https://doi.org/10.1109/IITC51362.2021.9537541.
[4] Chen, R., M. Lofrano, G. Mirabelli, G. Sisto, S. Yang, A. Jourdain, F. Schleicher, et al. "Power, Performance, Area and Thermal Analysis of 2D and 3D ICs at A14 Node Designed with Back-Side Power Delivery Network." In 2022 International Electron Devices Meeting (IEDM), 23.4.1-23.4.4, 2022. https://doi.org/10.1109/IEDM45625.2022.10019349.
[5] Kwak, et al. A Reconfigurable Monolithic 3D Switched Capacitor DC-DC Converter with Back-End-of-Line Oxide Channel Transistor, MWSCAS, 2023.