

Flexagon: A Reconfigurable Sparse Multi-dataflow Accelerator for DNNs

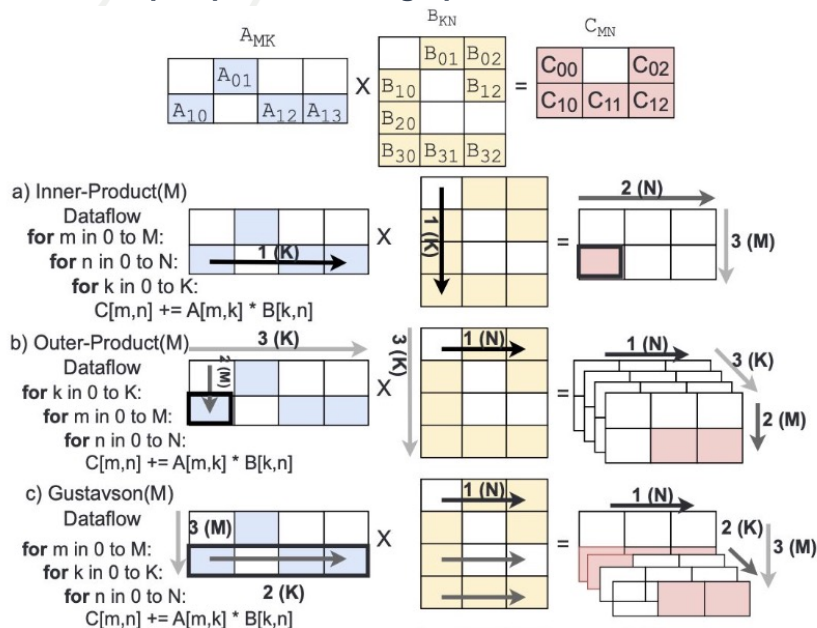


Georgia Tech College of Computing
Center for Research into
Novel Computing Hierarchies

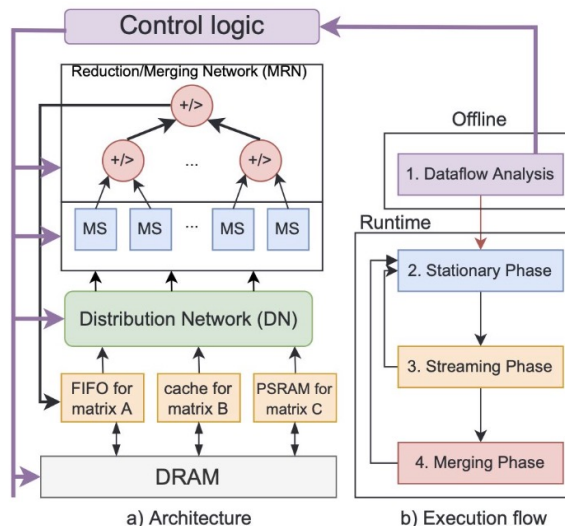
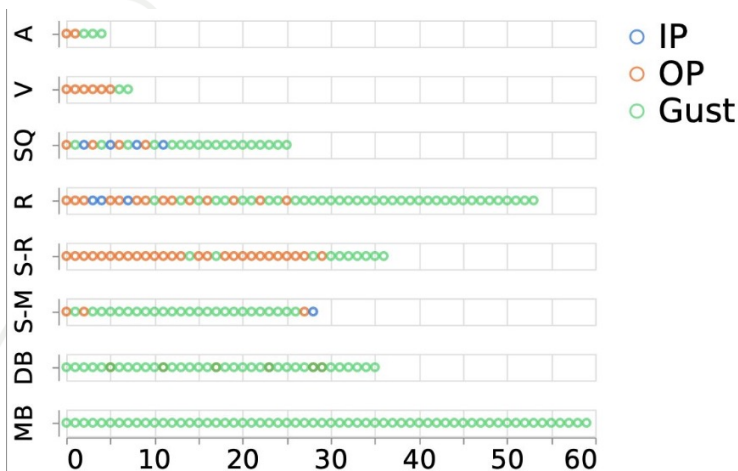
Francisco Muñoz-Martínez¹, **Raveesh Garg**², Michael Pellauer³, José L. Abellán¹, Manuel E. Acacio¹, and Tushar Krishna²

¹Universidad de Murcia, ²Georgia Institute of Technology, ³NVIDIA

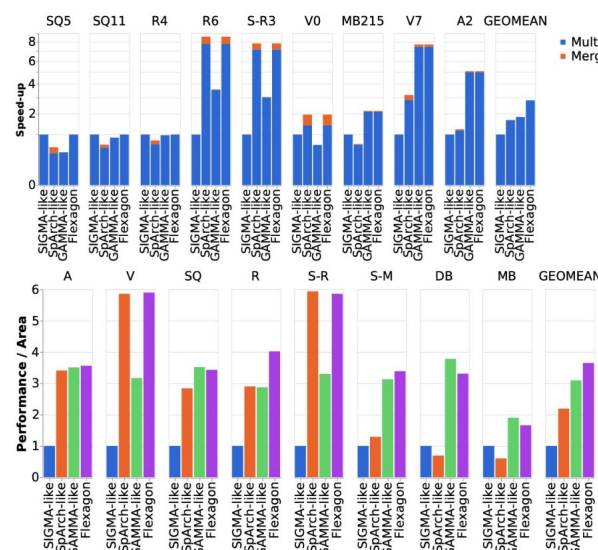
SpMSpM scheduling options



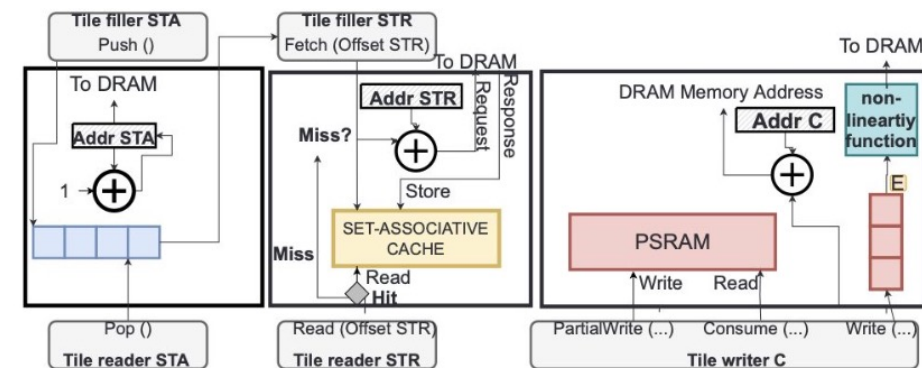
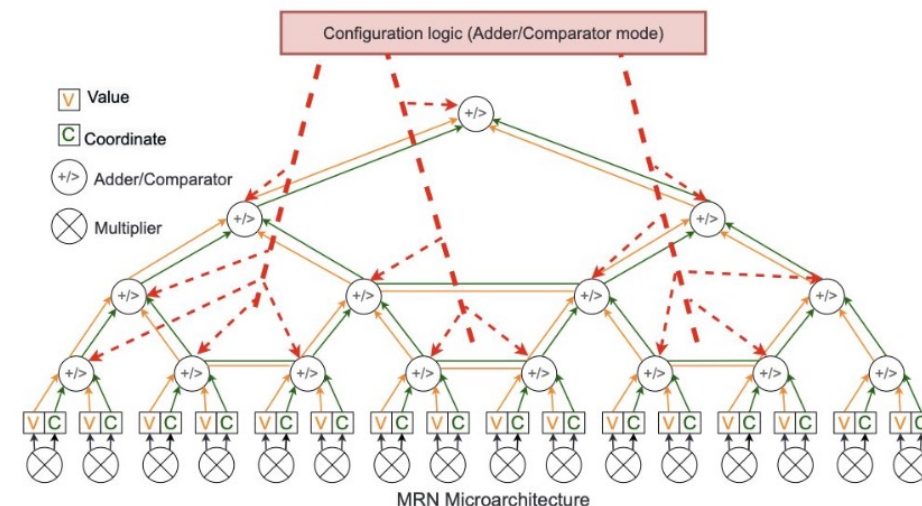
One Size Does Not Fit All



Results



Flexagon Architecture



Artifacts

We model
Flexagon in
SST-
STONNE.

