

Homework 3

4.10

AND ~ 2ns

OR ~ 1ns

XOR ~ 3ns

total delay is 24ns

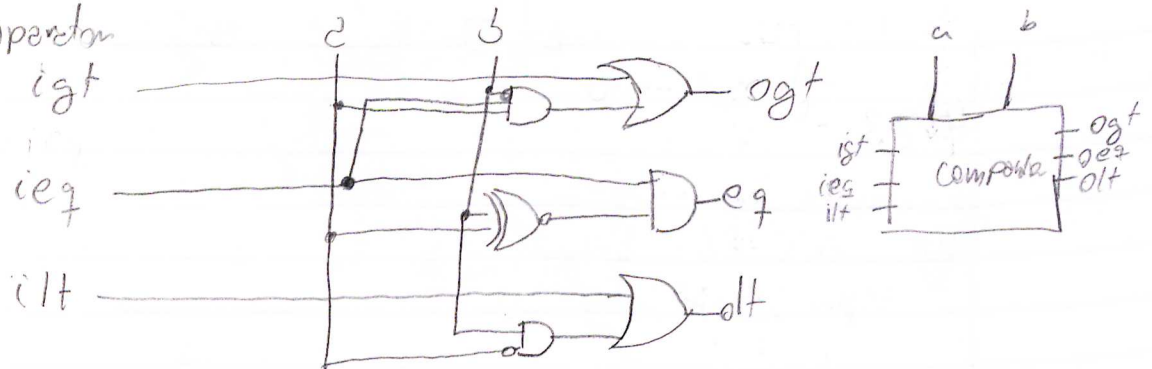
The delay of the full adder is 3ns (XOR or AND + OR).

Since we have 8 bits, the

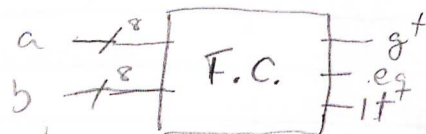
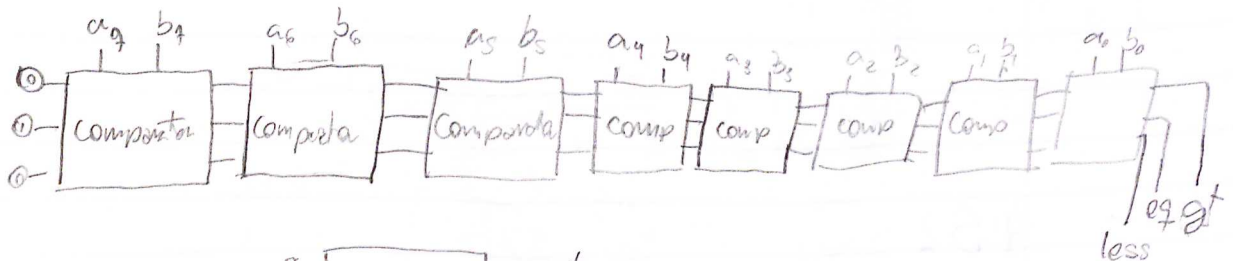
~~4.14~~

4.20

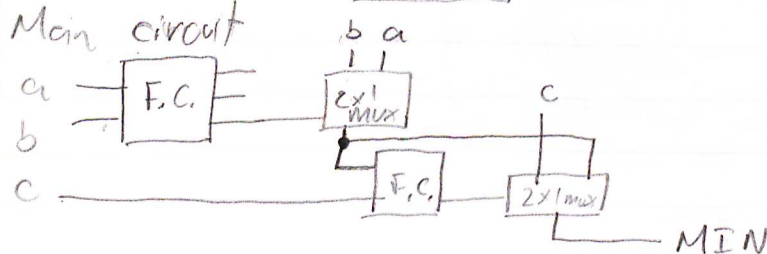
Comparator



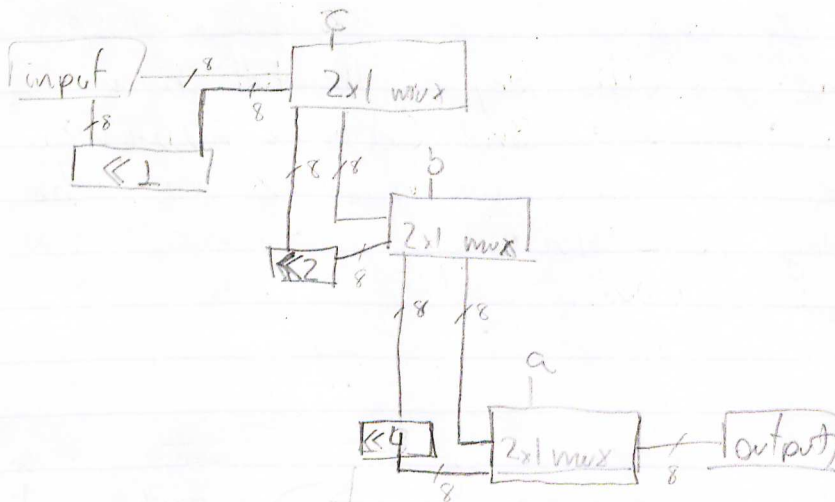
8-bit comparator



Main circuit

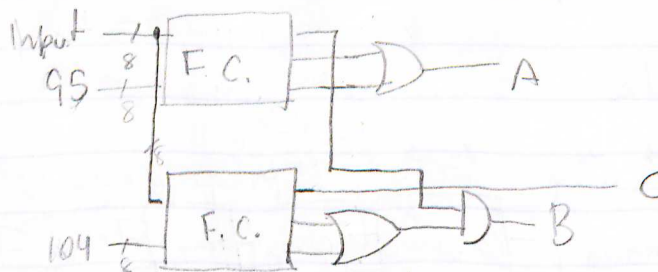


4.46



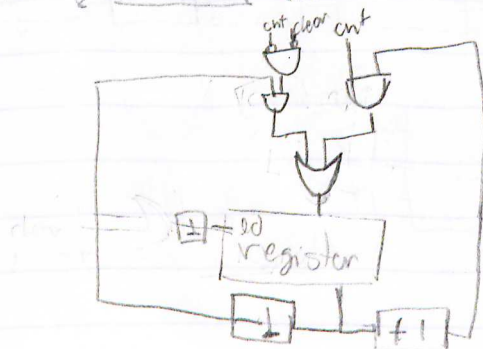
4.23

input ≤ 95 $A=1$
 $95 < \text{input} \leq 104$ $B=1$
 input > 104 $C=1$



4.52

a)



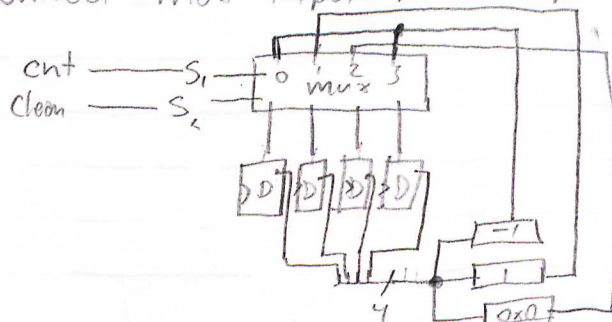
b)

1. size = 3 operations — down / up / clear

2. create mux operation table

| S ₁ | S ₂ | operation |
|----------------|----------------|------------|
| 0 | 0 | down count |
| 0 | 1 | up count |
| 1 | 0 | clear |
| 1 | 1 | down count |

3. connect mux inputs / 4- Map lines



| clear | cnt | S ₁ | S ₂ |
|-------|-----|----------------|----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

4.32

a) $2 = 00000010$

b) $-1 = 11111111$

c) $23 = 00010111 \Rightarrow -23 = 11101001$

d) $+128 = 10000000 \Rightarrow -128 = 10000000$

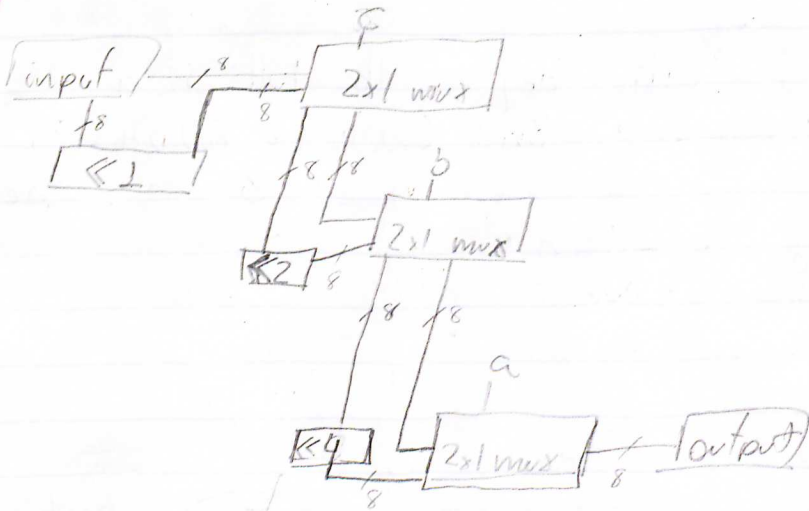
this number is not represented in 8 bit arch, too

e) $126 = 01111110$

f) $127 = 01111111$

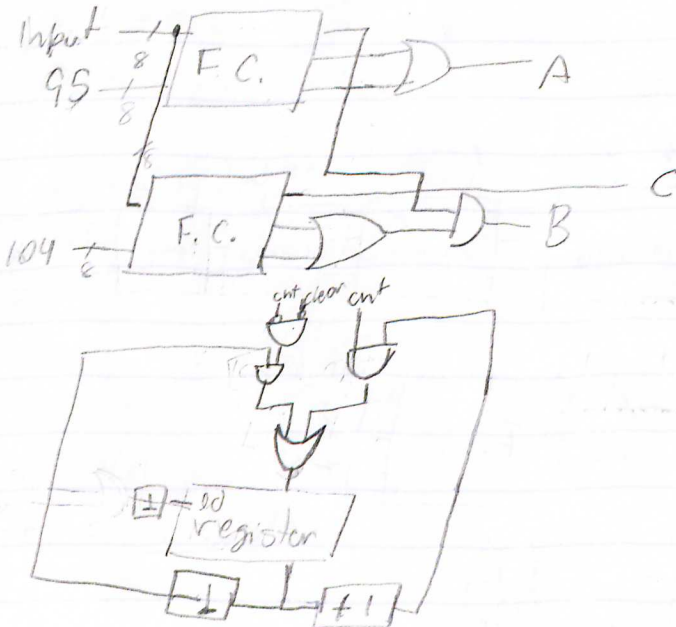
g) $0 = 00000000$

4.46



4.23

input ≤ 95 $A=1$
 $95 < \text{input} \leq 104$ $B=1$
 input > 104 $C=1$

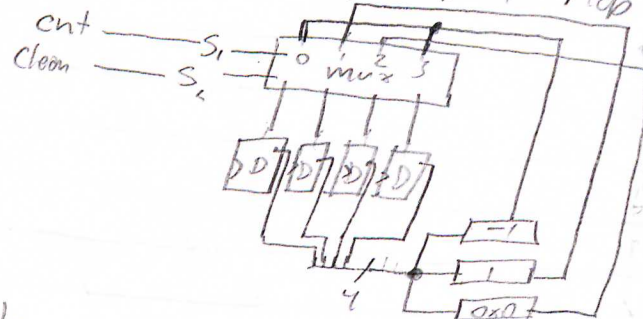


b)

1. Size = 3 operations — 1: down / up / clear
2. create mux, operation table

| S ₁ | S ₂ | operation |
|----------------|----------------|------------|
| 0 | 0 | down count |
| 0 | 1 | up count |
| 1 | 0 | clear |
| 1 | 1 | down count |

3. connect mux inputs / 4- Map lines



| clean | cnt | S ₁ | S ₂ |
|-------|-----|----------------|----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

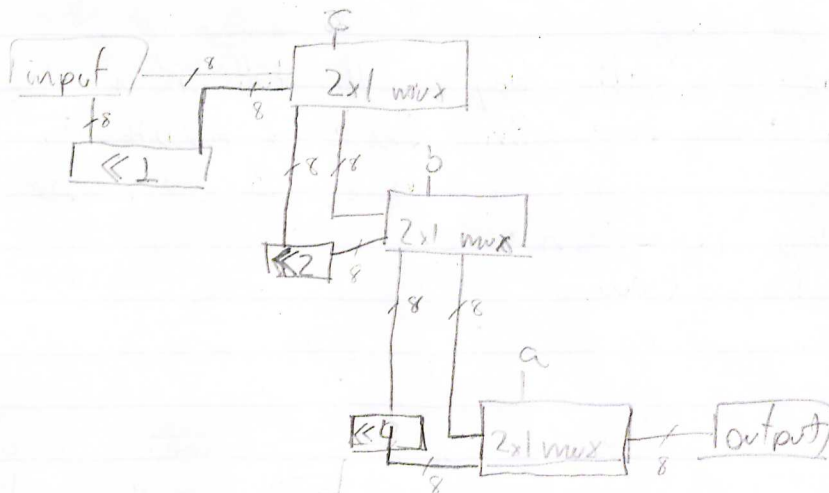
4.32

- a) 2 = 00000010
- b) -1 = 11111111
- c) 23 = 00010111 ⇒ -23 = 11101001
- d) +128 = 10000000 ⇒ -128 = 10000000

this number is not represented in 8 bit arch, te

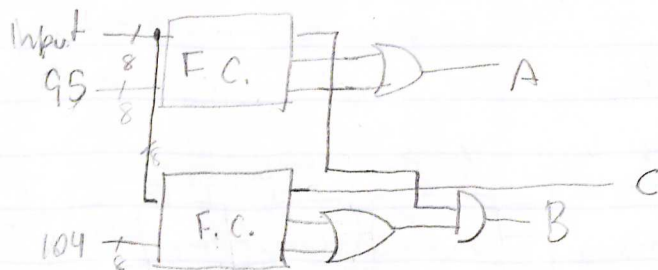
- e) 126 = 01111110
- f) 127 = 01111111
- g) 0 = 00000000

4.46



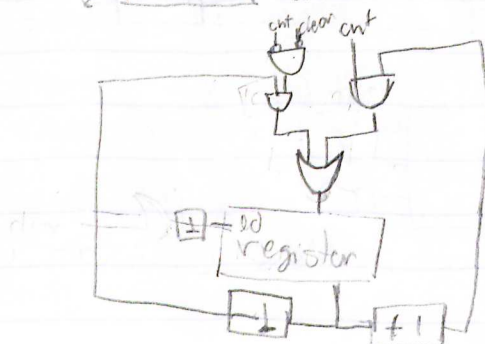
4.23

$\text{input} \leq 95 \quad A=1$
 $95 < \text{input} \leq 104 \quad B=1$
 $\text{input} > 104 \quad C=1$



4.52

a)



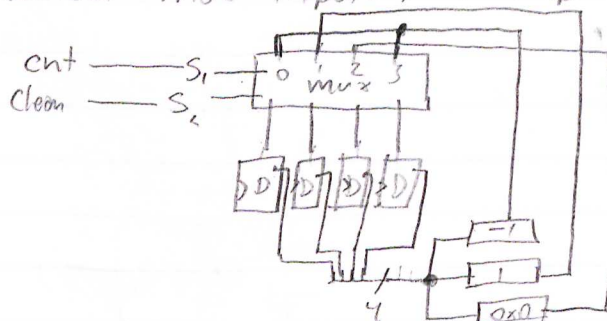
b)

1. size = 3 operations — down / up / clear

2. create mux operation table

| S ₁ | S ₂ | operation |
|----------------|----------------|------------|
| 0 | 0 | down count |
| 0 | 1 | up count |
| 1 | 0 | clear |
| 1 | 1 | down count |

3. connect mux inputs / 4-Map lines



| clean | cnt | S ₁ | S ₂ |
|-------|-----|----------------|----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

4.32

a) $2 = 00000010$

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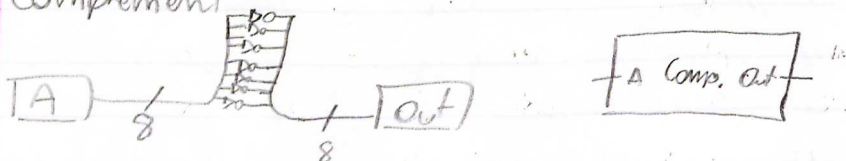
e) $126 = 01111110$

f) $127 = 01111111$

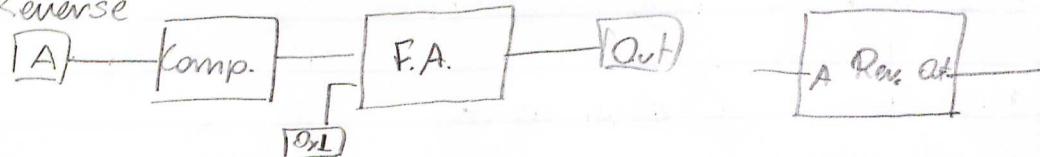
g) $0 = 00000000$

4.40

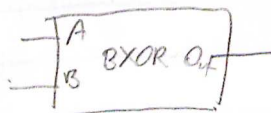
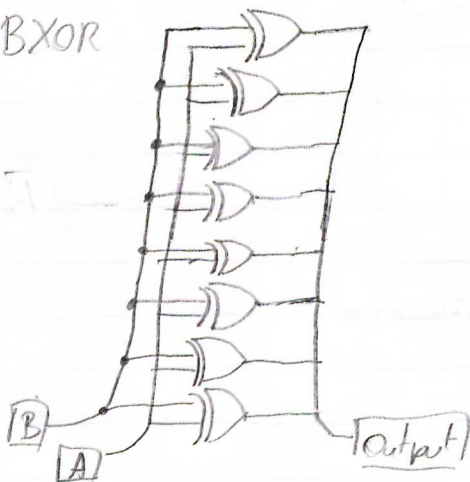
Complement



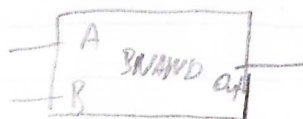
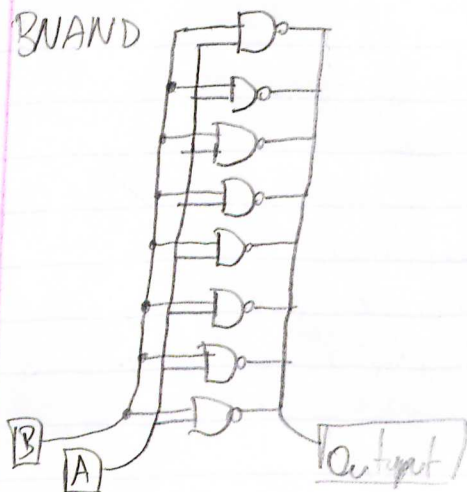
Reverse



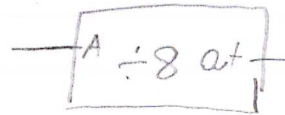
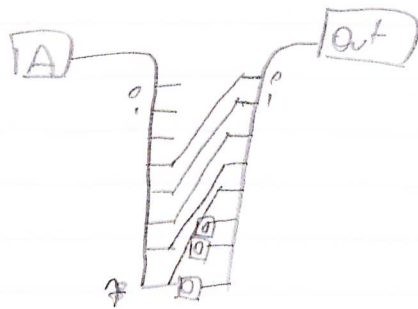
BXOR



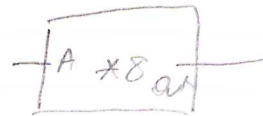
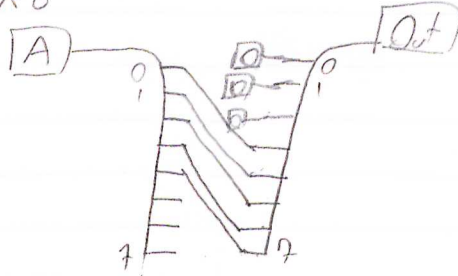
BNAND



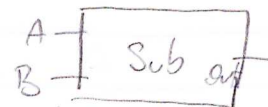
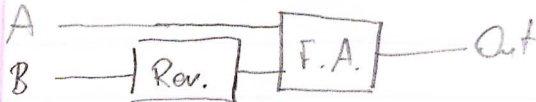
$\div 8$



$\times 8$



Subtractor



ALU

