ORTA DOĞU TEKNİK ÜNİVERSİTESİ
MIDDLE EAST TECHNICAL UNIVERSITY

EE445- Computer Architecture I

(HDL Homework)

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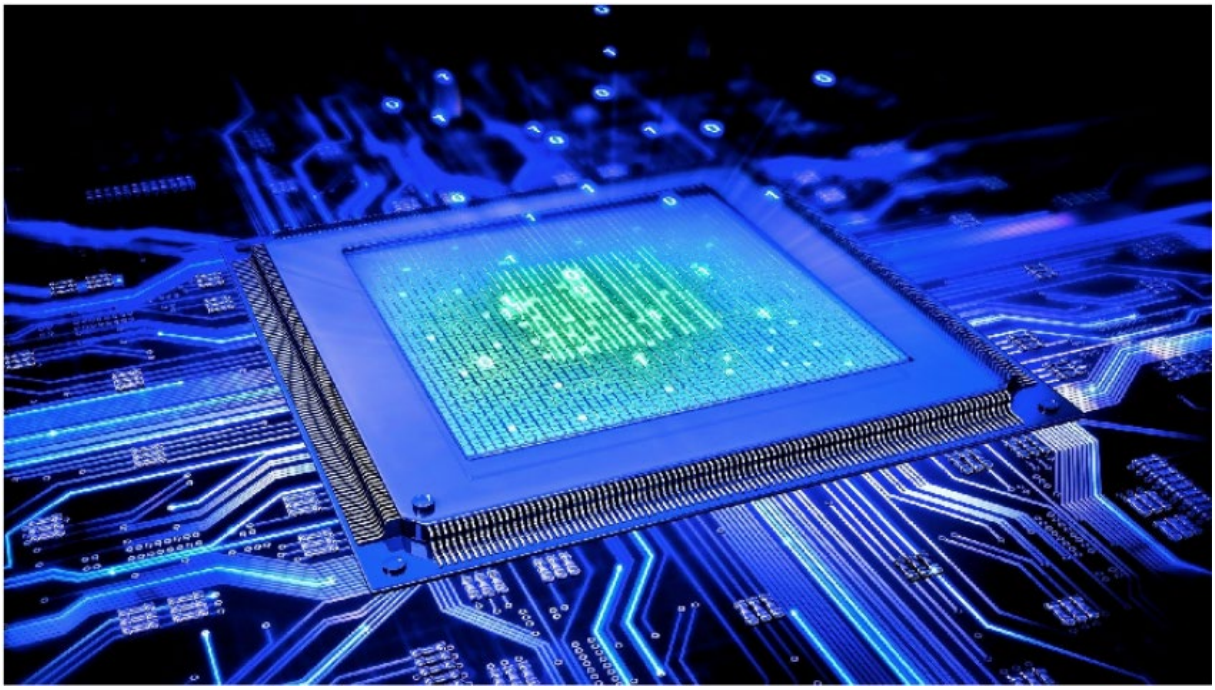

PART 1) Operations to Be Implemented

- With related to this part I thought that I can implement the given specifications in the memory unit that I created and using them them in initial begin but, I could not manage the create controller. Therefore I could not do this part.

PART 2) Module Design with Verilog HDL (20% Credits)

- I created four different modules. “data_Mux_8x1.v”,” ALU.v”,” registers.v”,” memory.v” respectively.

PART 2-1) data_Mux_8x1.v

- I created a verilog HDL which is called “data_Mux_8x1.v” and its inputs and outputs are can be seen in this file

PART 2-2) ALU.v

- I created a verilog HDL which is called ” ALU.v”and its inputs and outputs are can be seen in this file

PART 2-3) registers.v

- I created a verilog HDL which is called ” registers.v” and its inputs and outputs are can be seen in this file

PART 2-4) memory.v

- I created a verilog HDL which is called ” memory.v” and its inputs and outputs are can be seen in this file

PART 3) Datapath Design (10% Credit)

- I created a verilog HDL which is called ” basiccomputerdatapath.v” and its inputs and outputs are can be seen in this file. Also note that I created .v file from the block diagram schematic below in figure1.

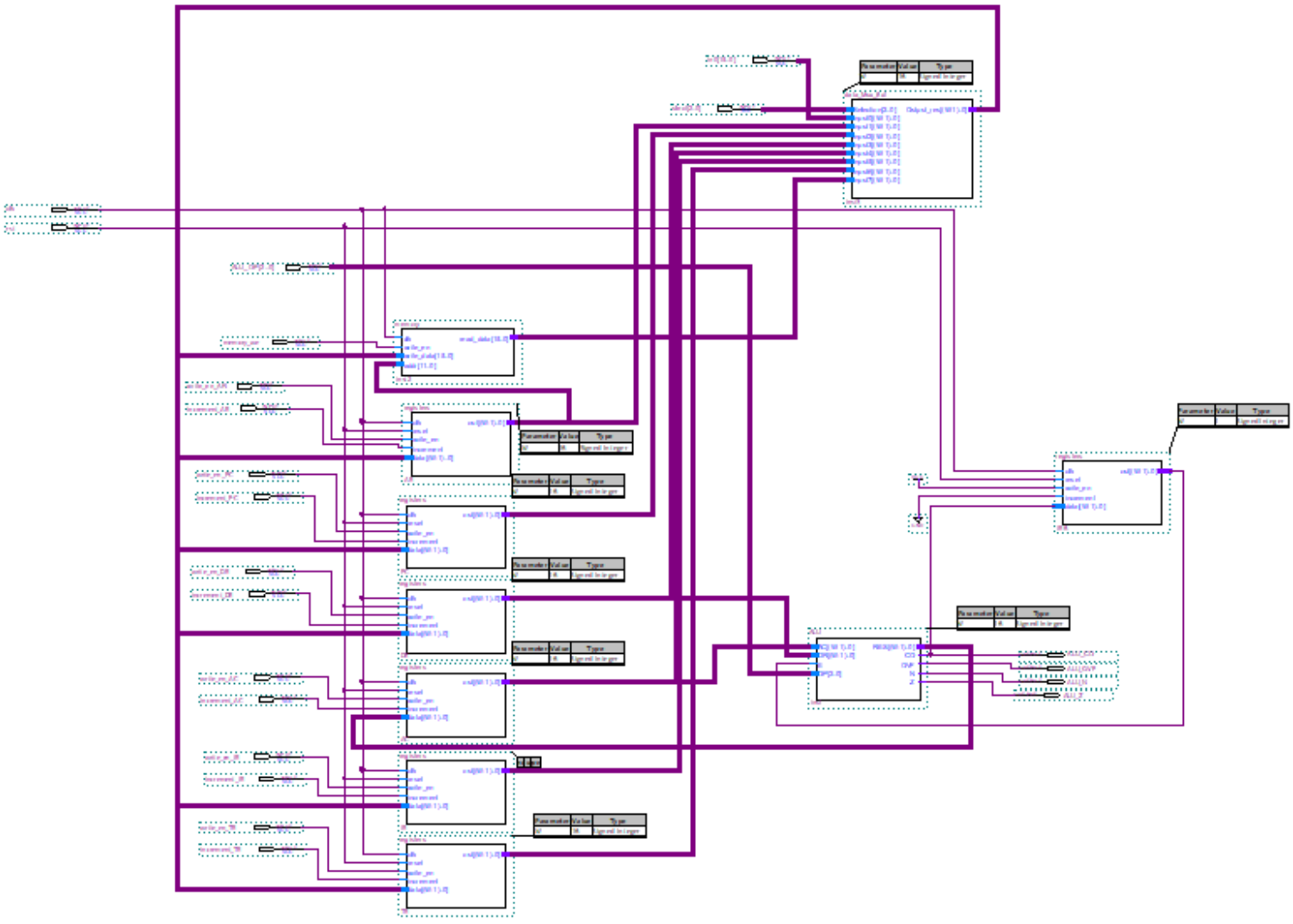

Figure 1: Datapath design.bdf file

PART 4) Controller Design (40 % Credit)

- I created a verilog HDL which is called “basiccomputercontroller” and its inputs and outputs are can be seen in this file. I could not solve the errors related to this part and and it did not work correctly.

PART 5) Putting The Computer Together

- I put the modules I created together in both datapath and in controller design.

PART 6) Simulation (30% Credit)

- No simulation results are present. ☹

PART 7) Deliverables

- 6 .v file related parts explained above, 1.bdf file
- A report.