Grégory Vaumourin

HPC Engineer at ATOS Bull (France)

Topic of Research

- Persistent Memory Technology for HPC
- I/O profiling, analysis and acceleration
- Cache Memory Based Optimizations (Data locality, Coherency protocol)
- Compilation analysis and data locality optimization

Education

2019- **HPC Engineer** in the Data Management Team, at ATOS Bull Company (France)
Description: Contribute as a member of the Data Management team to develop a framework for I/O profiling, analysis and acceleration. This includes the C/Python based SW implementation of an ephemeral Flash-Based Burst Buffer within the **SLURM** Workload Manager

2017-2019 **Associated Researcher** in the Uppsala Architecture Research Team (**UART**), Uppsala University (Sweden)
Description: Analyzing the opportunity of the new non-volatile memories technologies (NVM) for cache-based memory systems both in hardware and software point of views with Pr. Black-Schaffer and Pr. Jimborean.

2013-2016 **PhD Degree in Electrical Engineering** from the University of Bordeaux (France).
Description: Hardware/Software co-design for data locality and coherence optimization in memory system for energy efficiency
Thesis done under the supervision Pr. **Denis Barthou** and Thomas Dombek at **CEA LIST** and **INRIA Bordeaux** and defended the 4th October 2016. Details avalaible **here**
Tools: **Gem5 simulator**, **McPAT/CACTI**, **Pintools**, **GCC**

2013 **6 months Internship** at CEA-LETI Grenoble (France)
Description: Participation in the national research project **GRECO** (GReen wireless Communicating Object) targetting low-power communicating networks. Developpement in the **WSNet simulator** for an industrial use-case simulation of an energy harvesting wireless sensor network (EH-WSN)

2008-2013 **Master degree** in Computer Engineering at National Institute of Applied Science (INSA) – Rennes (France)

Scientific Publications

2019 **Which Memory Abstraction for NVDIMM on Object Storage**
Vaumourin G., Laferriere C. Couvee P. and Valat Presentation at ECMWF for the NEXTGenIO Workshop on applications of NVRAM storage to exascale I/O Slides and Presentation available **here**

2018 **DB-AMB: Dataset-Based Allocation, Migration, and Bypassing in hybrid non-volatile/SRAM caches**
Vaumourin G., Jimborean A. and Black-Schaffer D.
Under Review at IEEE Transaction on Computers **pre-print**

2017 **Dedicated read-only/read-write cache design for data locality and coherence optimization**
Vaumourin G., Dombek T., Guerre A., Barthou D.
Technical Report **print**

2016 **Specific Read-only Data Management for Memory System Optimization**
Vaumourin G., Dombek T., Guerre A., Barthou D.
The 24th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP'16)

2015 **Co-simulating complex energy harvesting WSN applications: an in-tunnel wind powered monitoring example**
Le Quang V., Didioui A., Vaumourin G., Bernier C., Broekaert F., Fritsch A.
International Journal of Sensor Networks (IJSNet)

2014 **Specific read only data management for memory hierarchy optimization**
Vaumourin G., Dombek T., Guerre A., Barthou D.
EWiLi'14, The 4th Embedded Operating Systems Workshop [**pdf**]

Research & Teaching Activities

2019 Contribution to the Sage European Project (**SAGE2**): studying the usage of persistent memory (DCPMM) within a multi-tiers object storage system (MERO) for Exescale

2018 Co-Supervision of a PhD Student: Analyzing SPEC2017 benchmarks memory behavior

2018 Sub-Reviewer of the International European Conference on Parallel and Distributed Computing Conference (**EuroPar'18**)

2017 Co-organizer of the 10th edition of the Scandinavian Multi-Core Workshop, the **MCC workshop**

2017 Member of the ACM's Women in Computing **Uppsala Chapter** and organization of the **Ada Lovelace Celebration**

2016 Teacher Assistant for Embbeded system and Hardware Programmation at IUT de Cachan (France)

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