THE AMERICAN UNIVERSITY IN CAIRO
الجامعة الأمريكية بالقاهرة

CSCE2303 - Computer Organization & Assembly Language Programming

Project II

Memory Hierarchy Simulator

Fall 2022

Submitted To: Dr. Nourhan Zayed

Submitted By:

Laila El Saeed - 900191891
Mohamed Hashish - 900201220
Sherif Wessa - 900203171

Implementation:

- Project is a memory cache simulator that traces the behaviour of the memory cache given the the cache information including: memory cache size (S), line size (L), and number of cycles to access memory (clk)
- Input is divided into 2 text files:
    - First one is: “input.txt” which includes: memory cache size (S), line size (L), and number of cycles to access memory (clk)
    - Second one is: “Memory Addresses.txt” for user to input sequence of 20 memory addresses in bytes
- The program traces and stores no. of accesses and no. of hits/misses, it displays the cache index alongside the valid bit and tag for each index. The hit/miss ratio is calculated as well as Average Memory Access Time (AMAT) value using the value of 100 clock cycles provided in the project description.

Design Decisions and Assumption:

- We decided to create a cache as a struct which contains the tag with a bool called valid bit.
- User enters cache data as well as memory addresses in the right format as seen in the .txt files

Bugs or Issues in simulator:

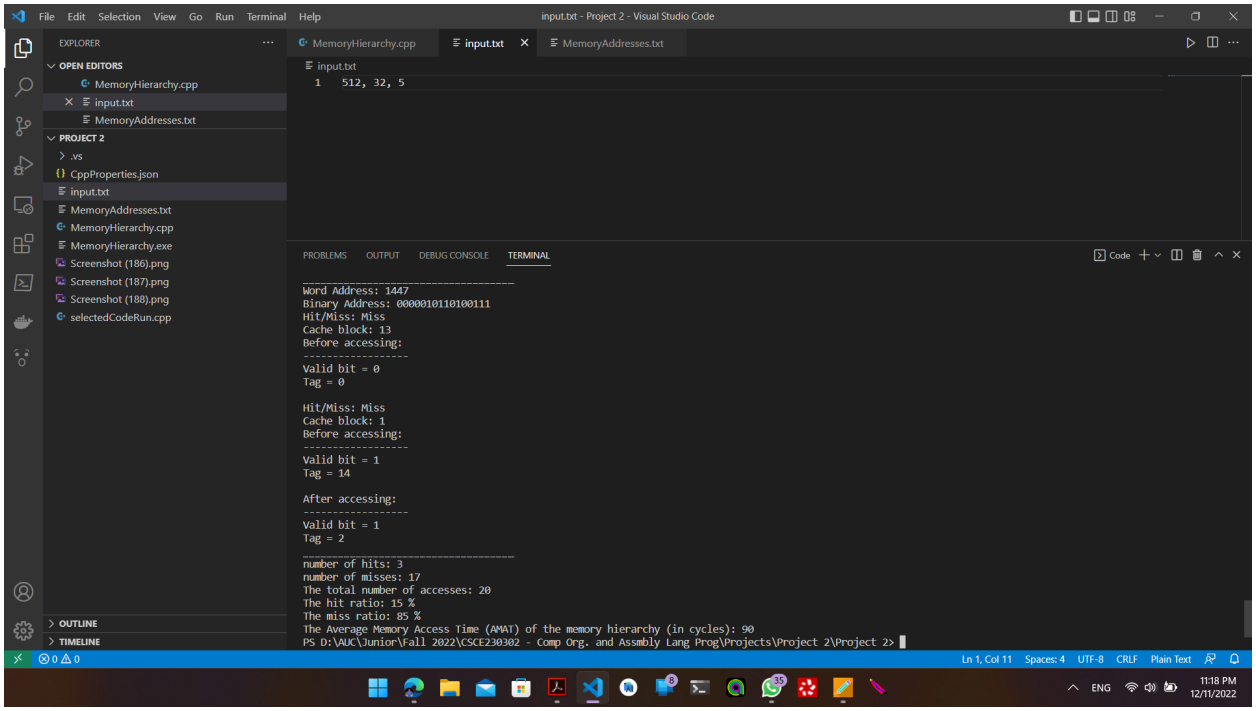
- While using the 2 test cases, no bugs/issues were found

Bonus:

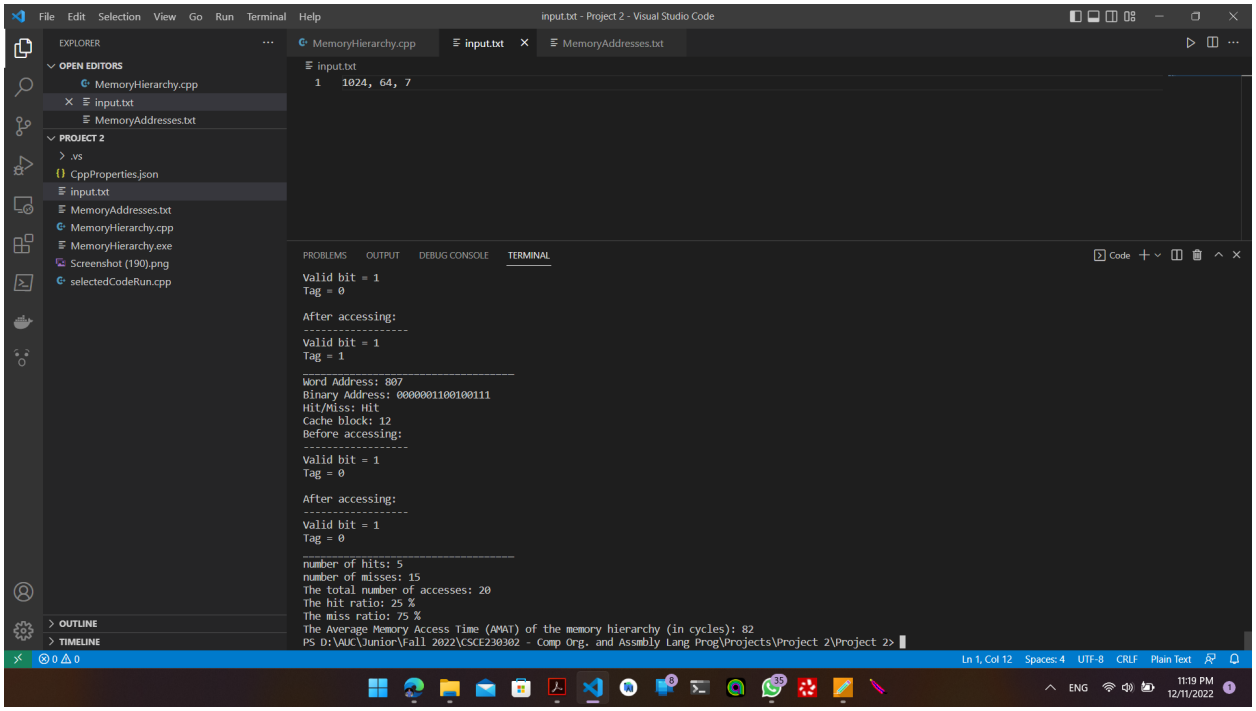
- We created a GUI app which implements the same code using Qt Framework, with some minor modifications to adapt the new style/framework

User guide with screenshots:

Example 1: S=512, L=32, clk=5



Example 2: S=1024, L=64, clk=7



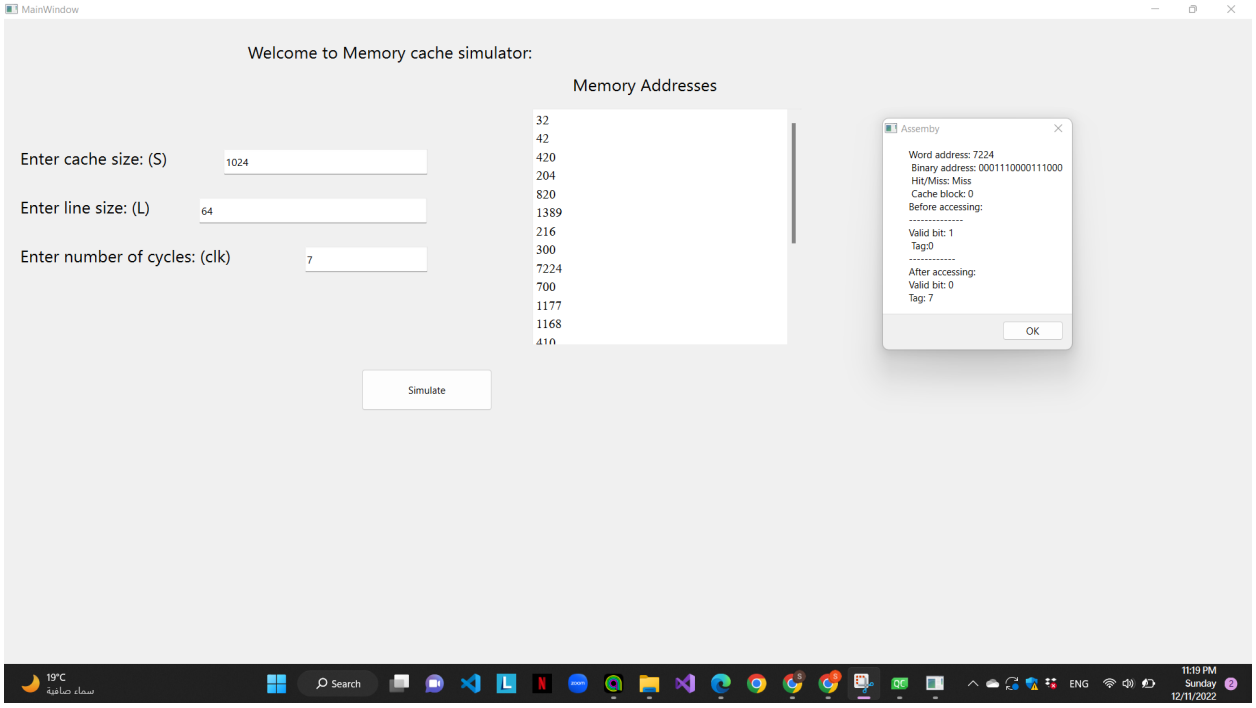
List of sequences simulated: (at least provide two 20 access sequences)

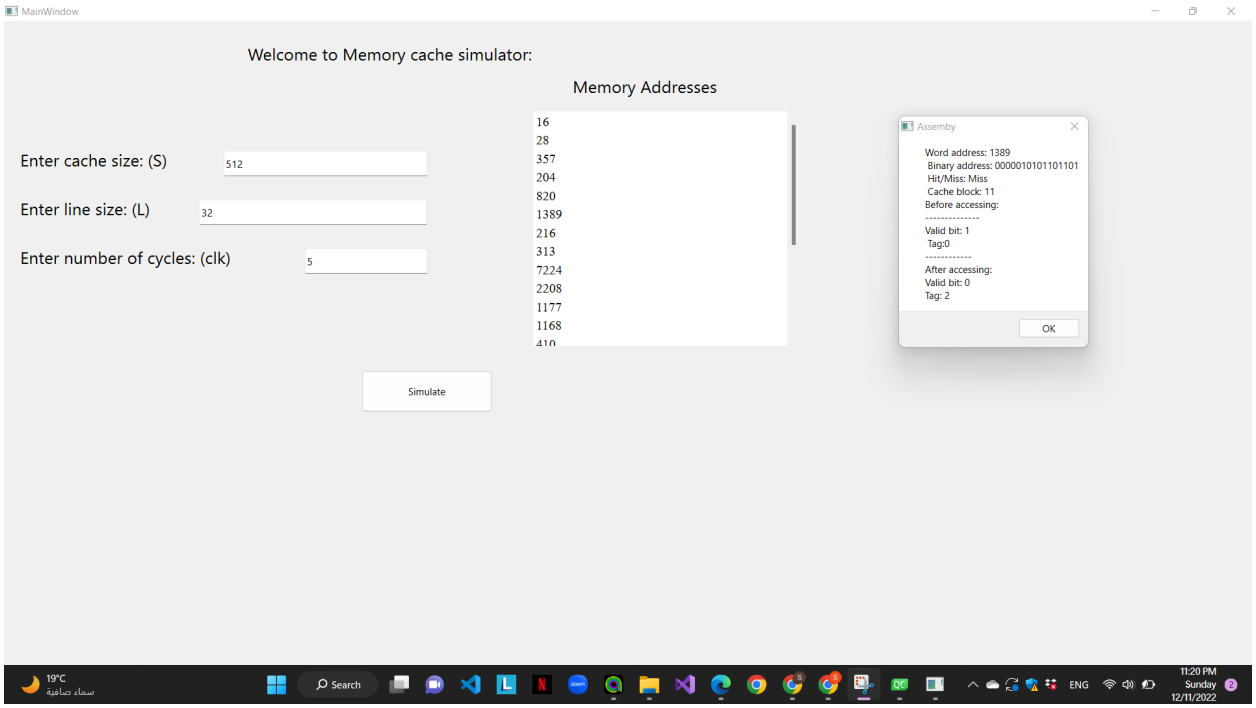
- **Sequence of memory addresses used in test case 1:**

16
28
357
204
820
1389
216
313
7224
2208
1177
1168
410
108
8900
3709
5004
2022
1447
1079

- **Sequences of memory addresses used in test case 2:**

32
42
420
204
820
1389
216
300
7224
700
1177
1168
410
455
8900
600
73
2022
1447
807




MainWindow
Welcome to Memory cache simulator:
Memory Addresses
Enter cache size: (S)
512
Enter line size: (L)
32
Enter number of cycles: (clk)
5
16
28
357
204
820
1389
216
313
7224
2208
1177
1168
Simulate
Assemby
Word address: 1389
Binary address: 0000010101101101
Hit/Miss: Miss
Cache block: 11
Before accessing:

Valid bit: 1
Tag:0

After accessing:
Valid bit: 0
Tag: 2
OK
19°C
Search
ENG
11:20 PM
Sunday
12/11/2022