

A

LTDC\_R[0..7] — (i) TFT\_LCD  
LTDC\_G[0..7] — (i) TFT\_LCD  
LTDC\_B[0..7] — (i) TFT\_LCD  
LTDC\_HSYNC — (i) TFT\_LCD  
LTDC\_VSYNC — (i) TFT\_LCD  
LTDC\_CLK — (i) TFT\_LCD

A

B

FMC\_A[0..11] — (i) SDRAM  
FMC\_D[0..15] — (i) SDRAM  
NA[0..15]  
FMC\_SDNRAS — (i) SDRAM  
FMC\_SDNCAS — (i) SDRAM  
FMC\_SDNWE — (i) SDRAM  
FMC\_SDCLK — (i) SDRAM  
FMC\_SDNE0 — (i) SDRAM  
FMC\_SDCKE0 — (i) SDRAM

B

C

QUADSPI\_BK1\_IO[0..3] — (i) QSPI\_BK1  
QUADSPI\_BK1\_CLK — (i) QSPI\_BK1  
QUADSPI\_BK1\_NCS — (i) QSPI\_BK1

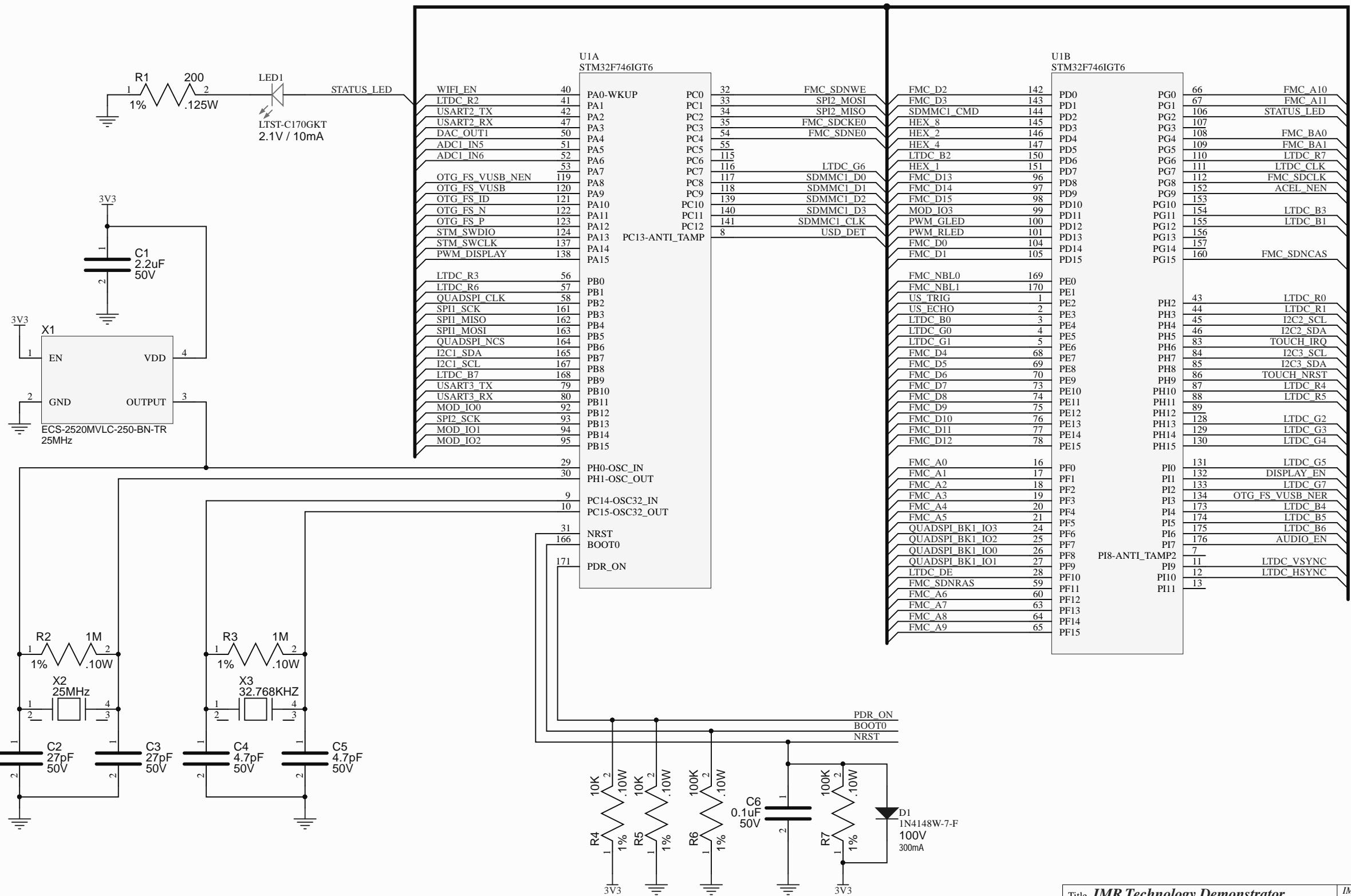
C

D

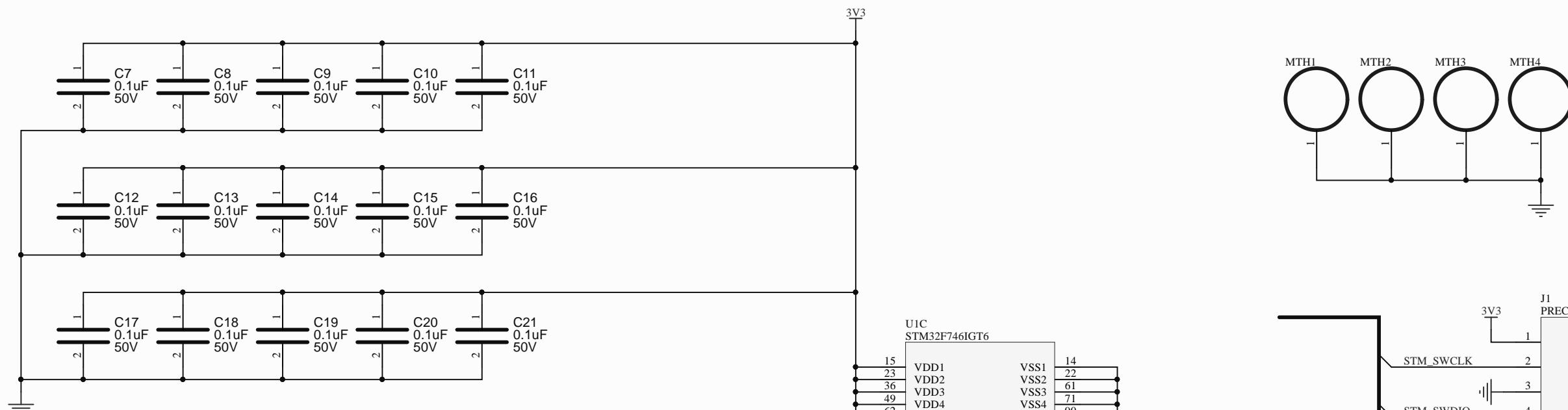
SDMMC1\_D[0..3] — (i) SDMMC1  
SDMMC1\_CLK — (i) SDMMC1  
SDMMC1\_CMD — (i) SDMMC1

D

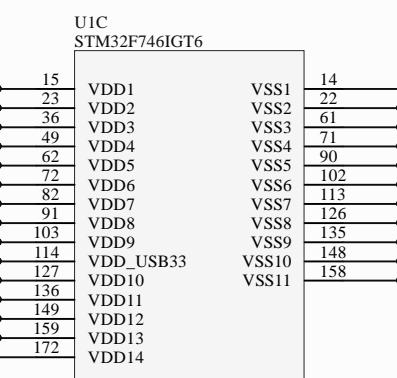
Title <b>IMR Technology Demonstrator</b>			IMR Engineering
Size: B	Number: IMR_002	Revision: 1	3621 Gin Way Snellville, GA 30039 USA
Date: 10/29/2020	Engr: H. Collector	Sheet 1 of 10	
File: TitleBlock.SchDoc			IMR Engineering <small>Ideas Made Real</small>



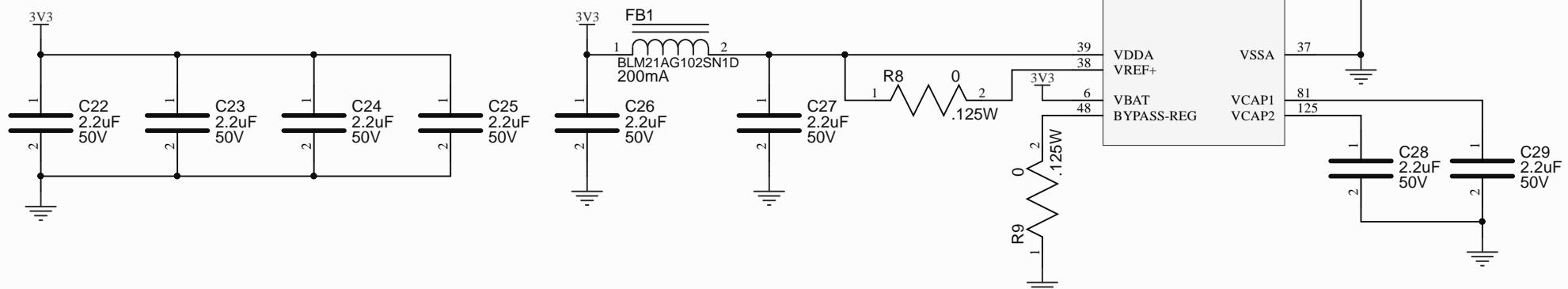
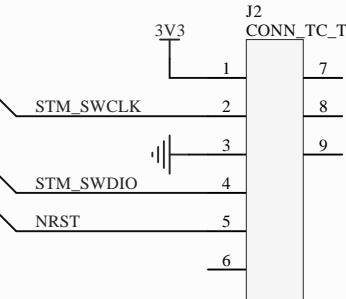
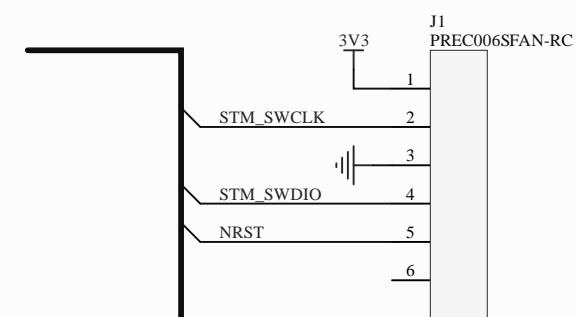
A

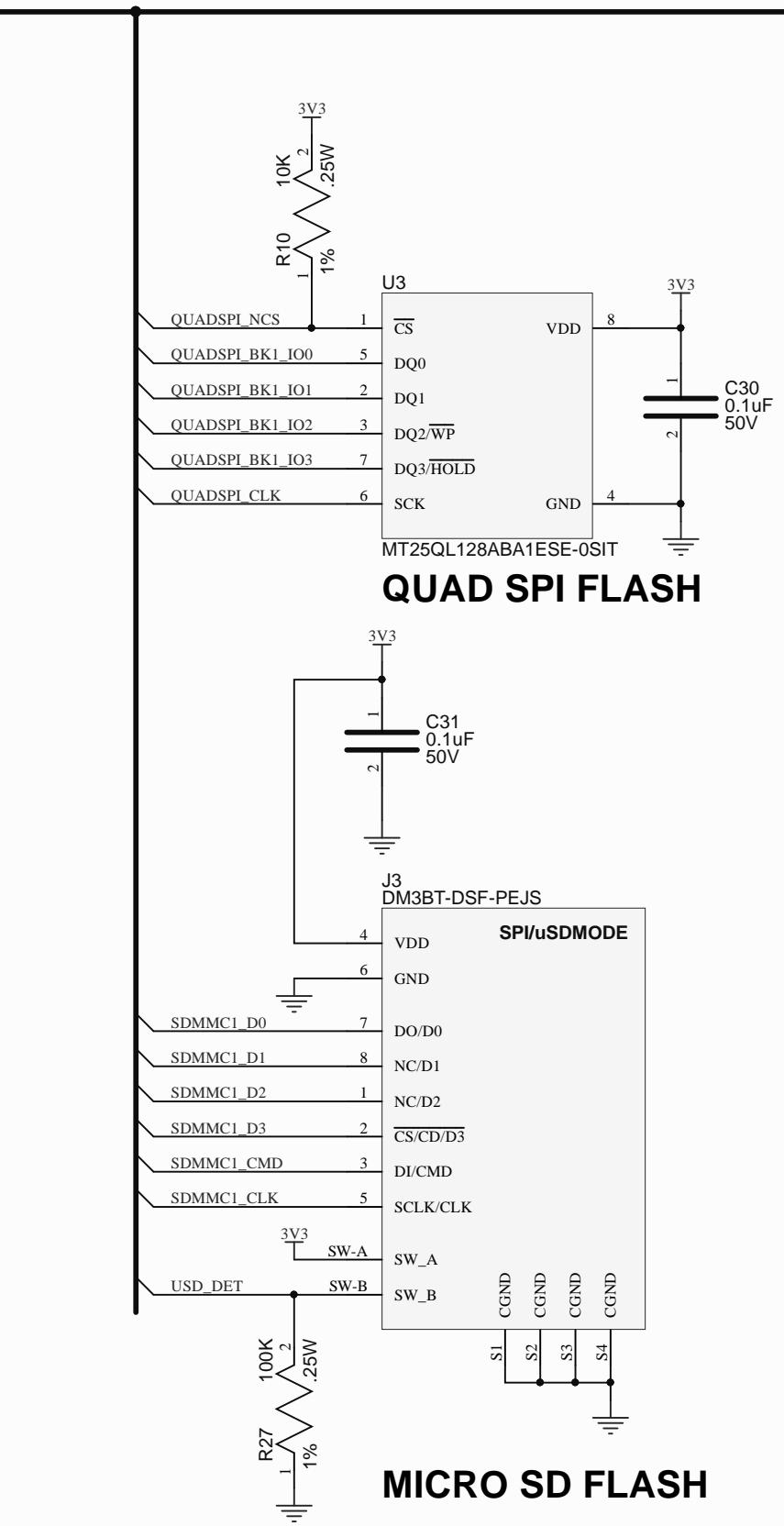


B

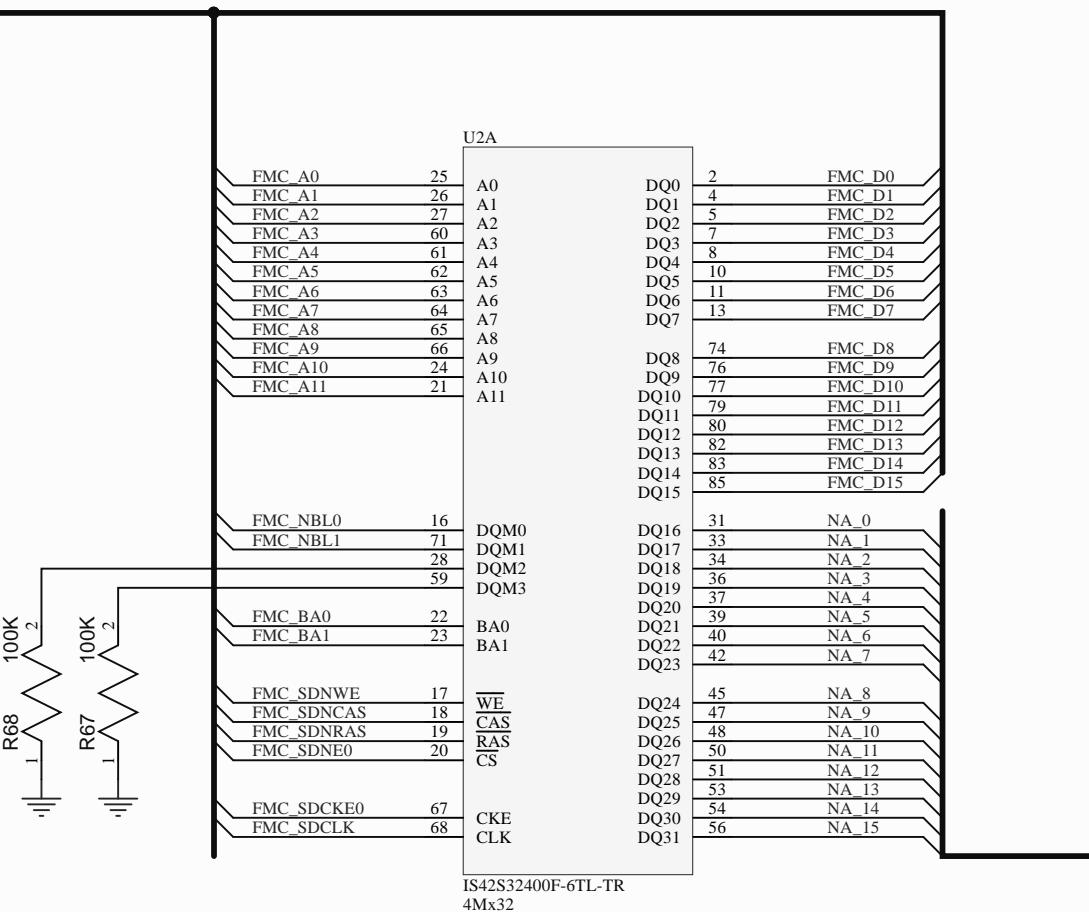


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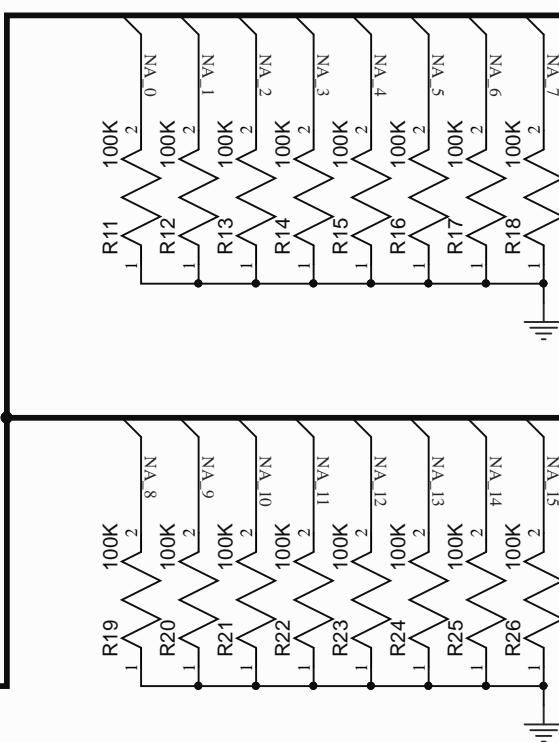
**JTAG**



## MICRO SD FLASH

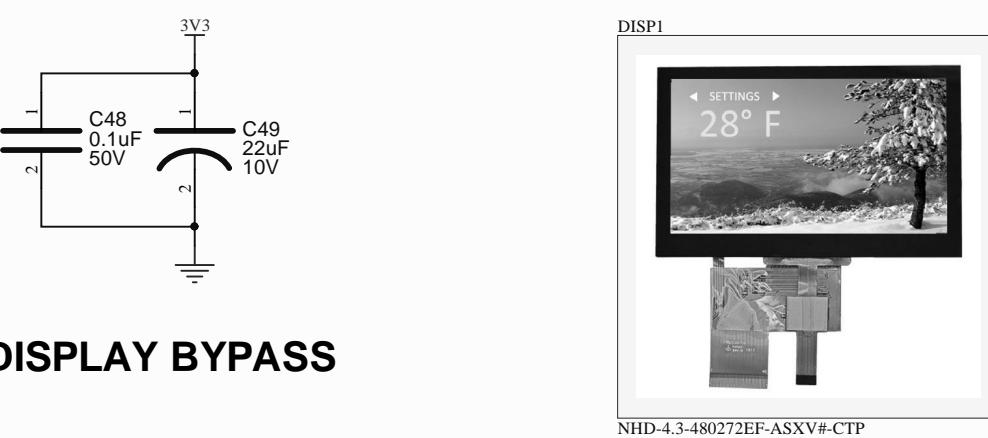
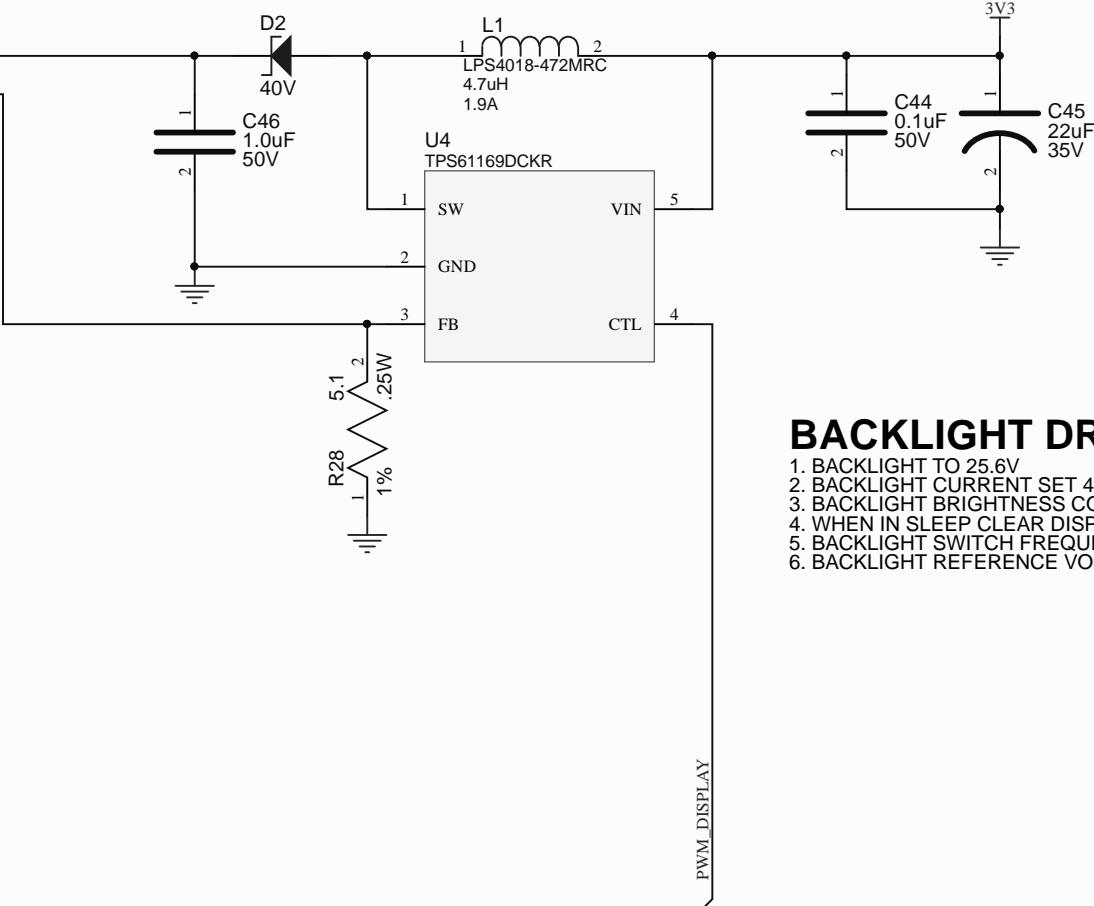
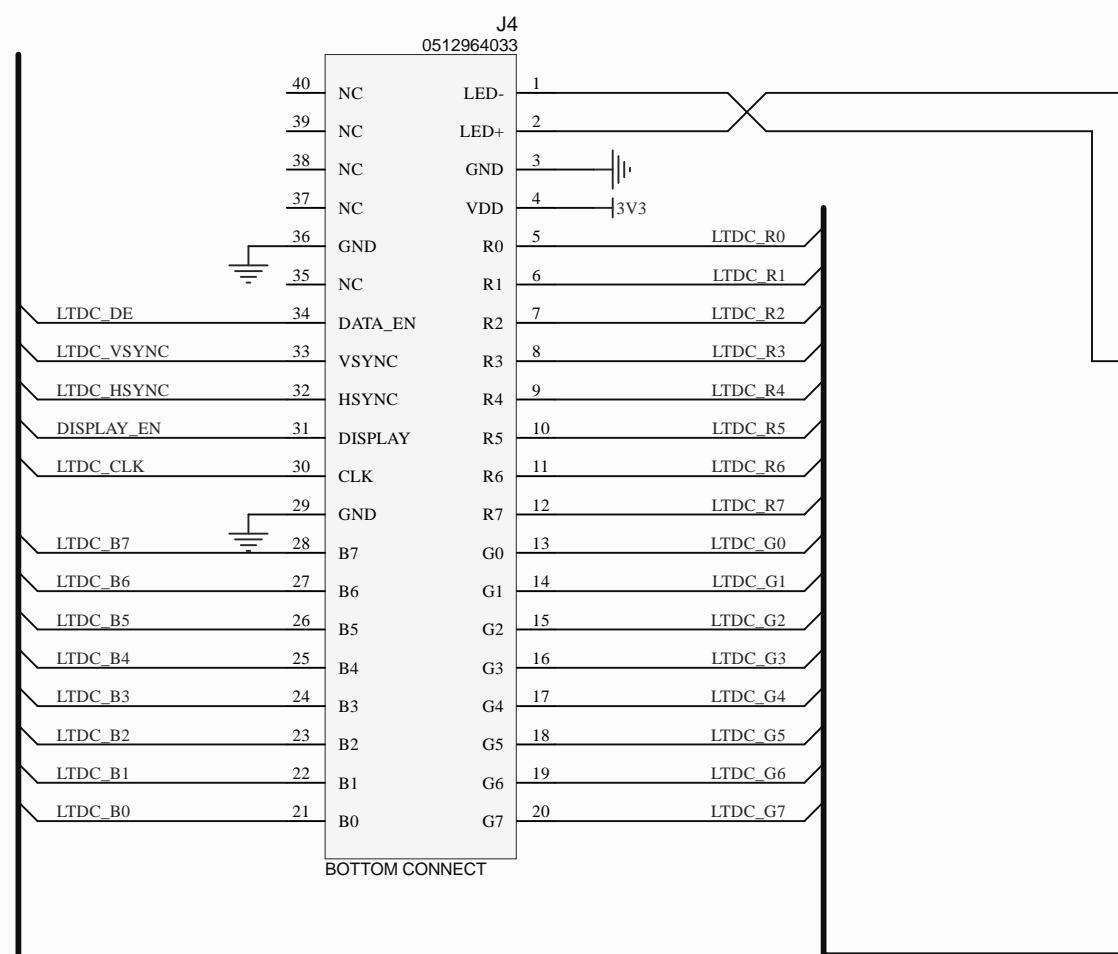


## **SD RAM**



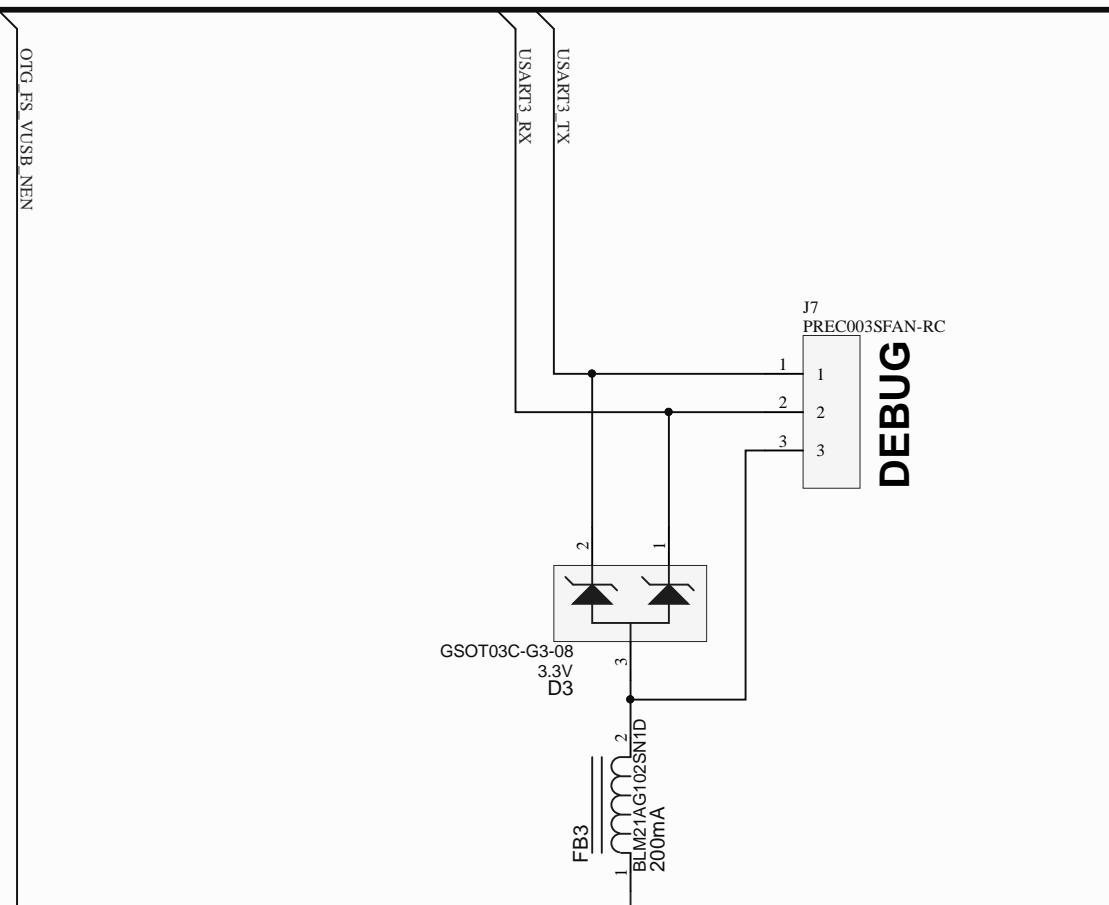
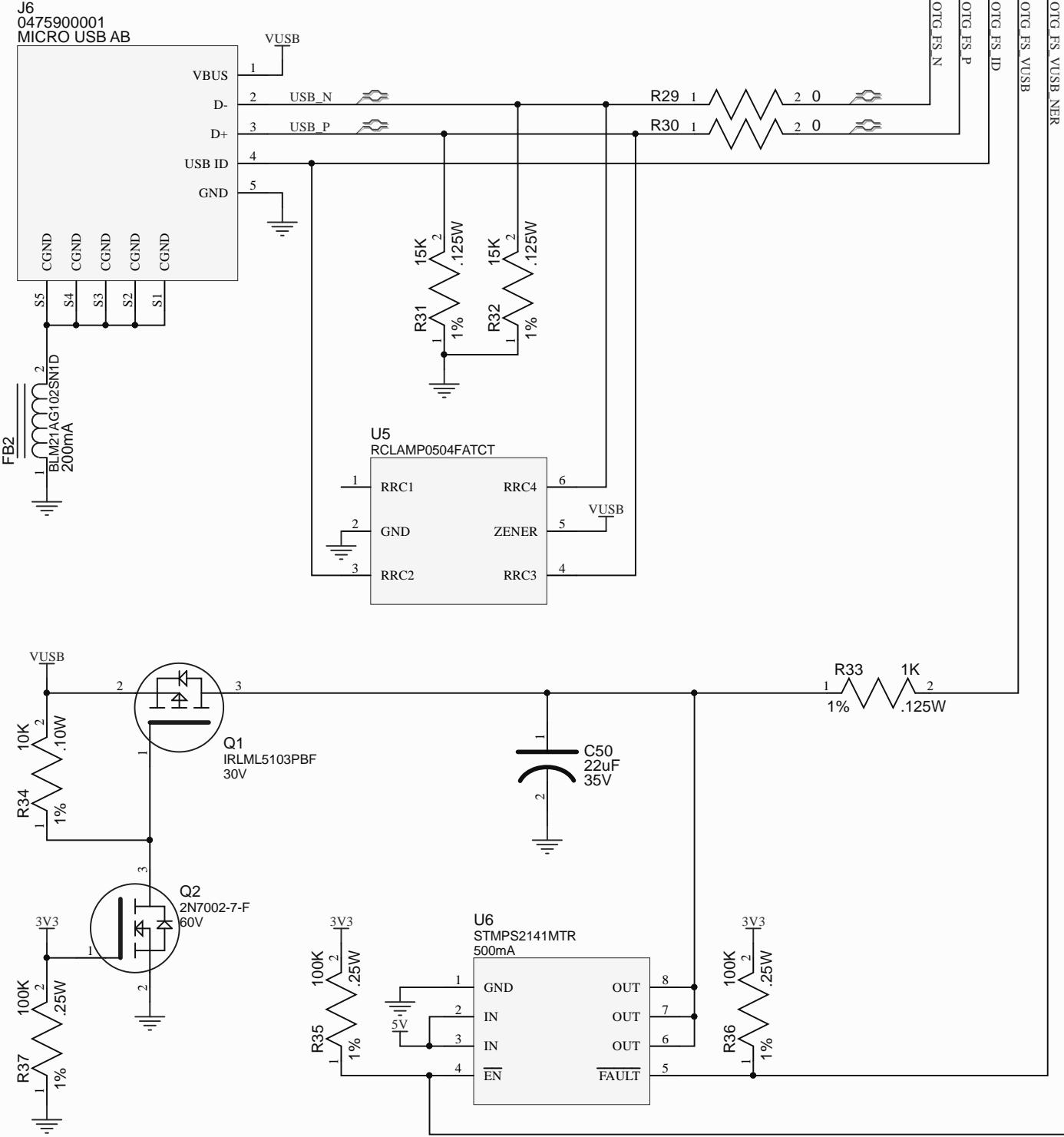
## **SD RAM BYPASS CAPS**

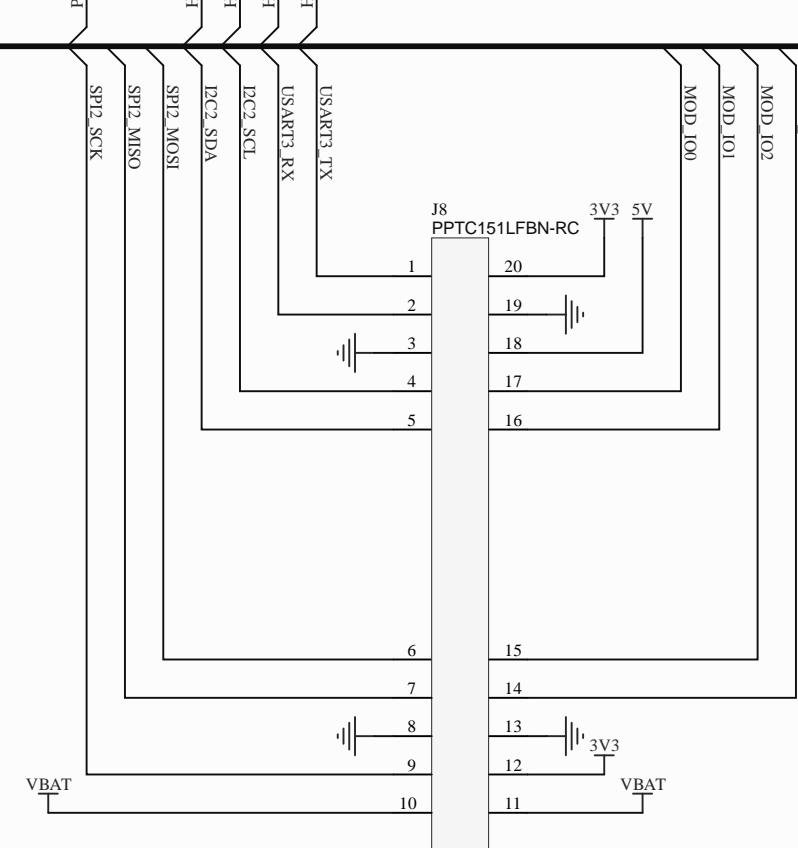
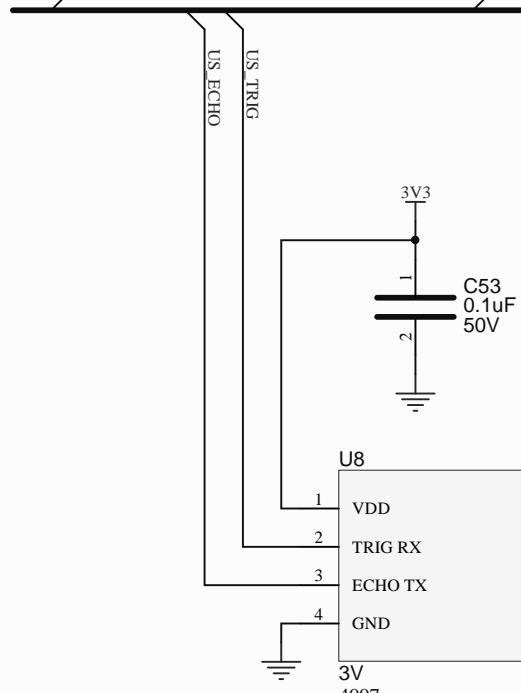
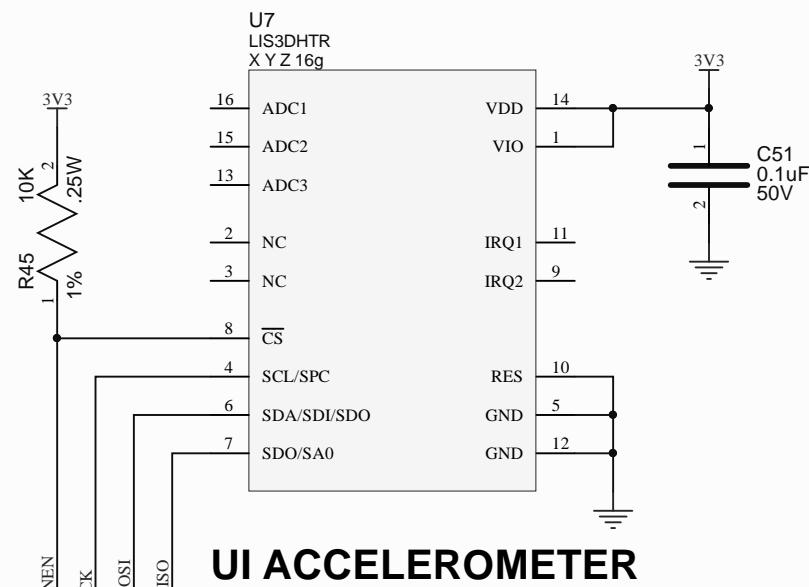
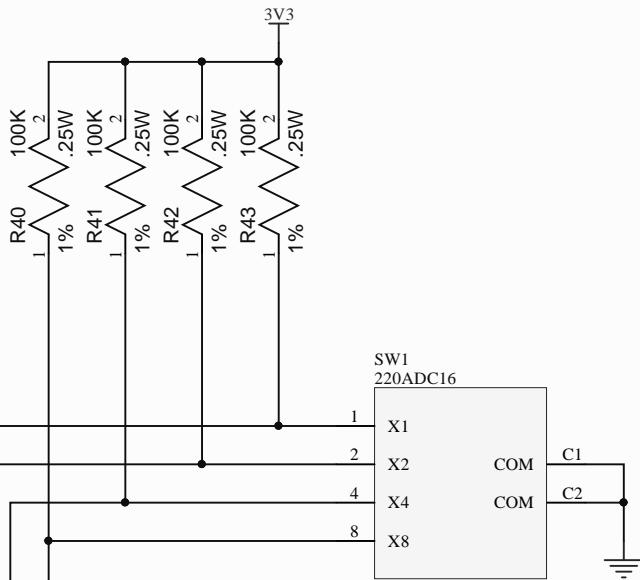
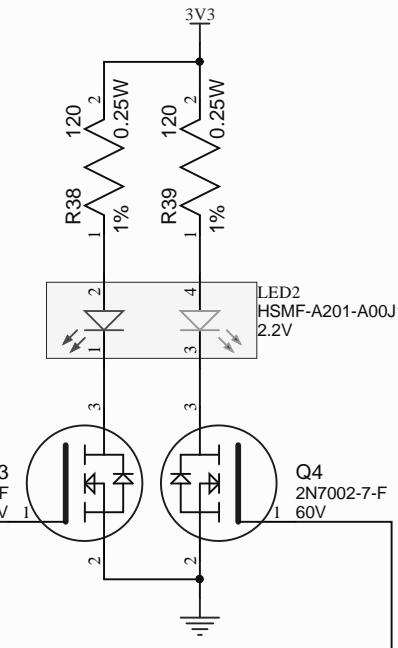
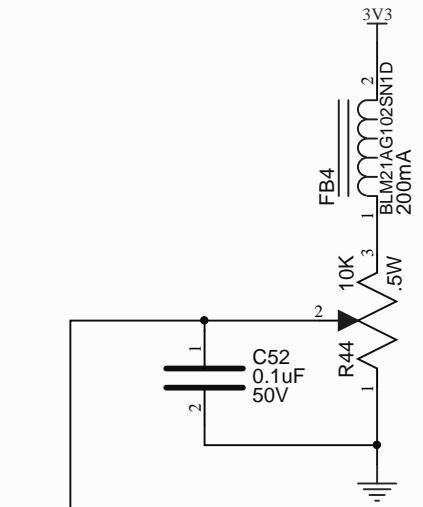
Title <b><i>IMR Technology Demonstrator</i></b>			<i>IMR Engineering 3621 Gin Way Snellville, GA 30039 USA</i>	<b>IMR Engineering</b> <small>Ideas Made Real</small>
Size: B	Number: IMR_002	Revision: 1		
Date: 10/29/2020	Engr: H. Collector	Sheet 4 of 10		
File: SystemMemory.SchDoc				

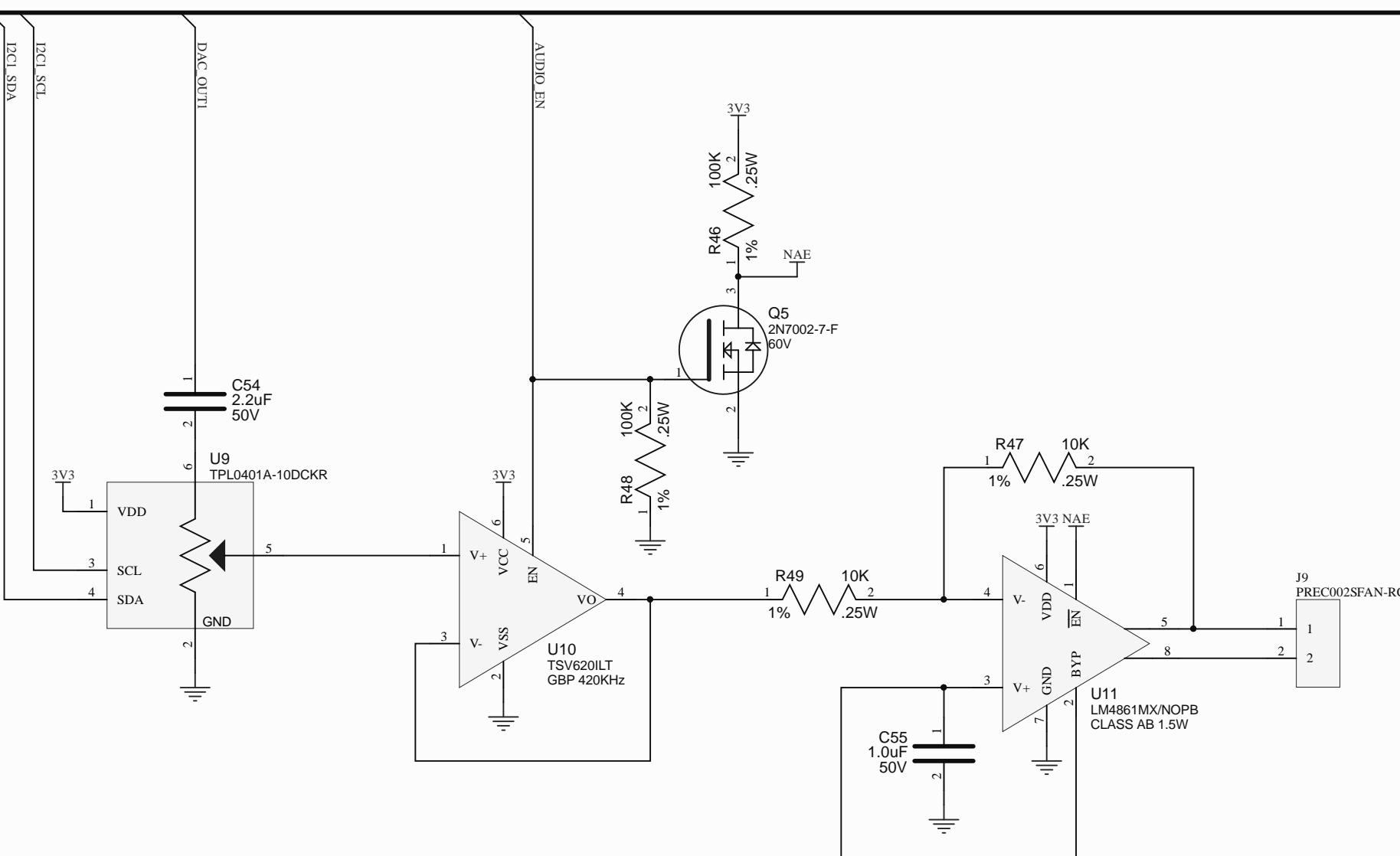


Title: <b>IMR Technology Demonstrator</b>	IMR Engineering
Size: B	Number: IMR_002
Date: 10/29/2020	Engr: H. Collector
File: LCD_TouchBackLight.SchDoc	Revision: 1
File: LCD_TouchBackLight.SchDoc	Sheet 5 of 10
File: LCD_TouchBackLight.SchDoc	USA
File: LCD_TouchBackLight.SchDoc	IMR Engineering

# USB OTG FS

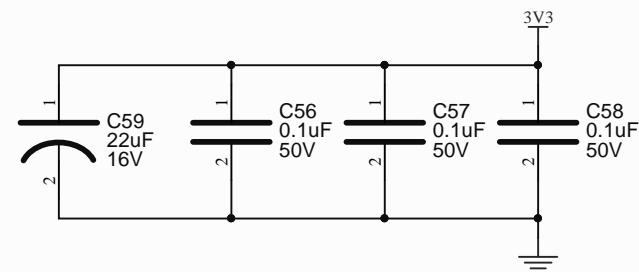






## AUDIO NOTES:

1. AUDIO BYPASS CAPS
  2. AUDIO OUTPUT AT 1.5W INTO 8 OHM
  3. INTENDED SPEAKER: PUI AUDIO, ASE02808MR-LW150-R
  4. AUDIO POT IS LINEAR SOFTWARE MUST CONVER TO LOG



A

A

B

B

C

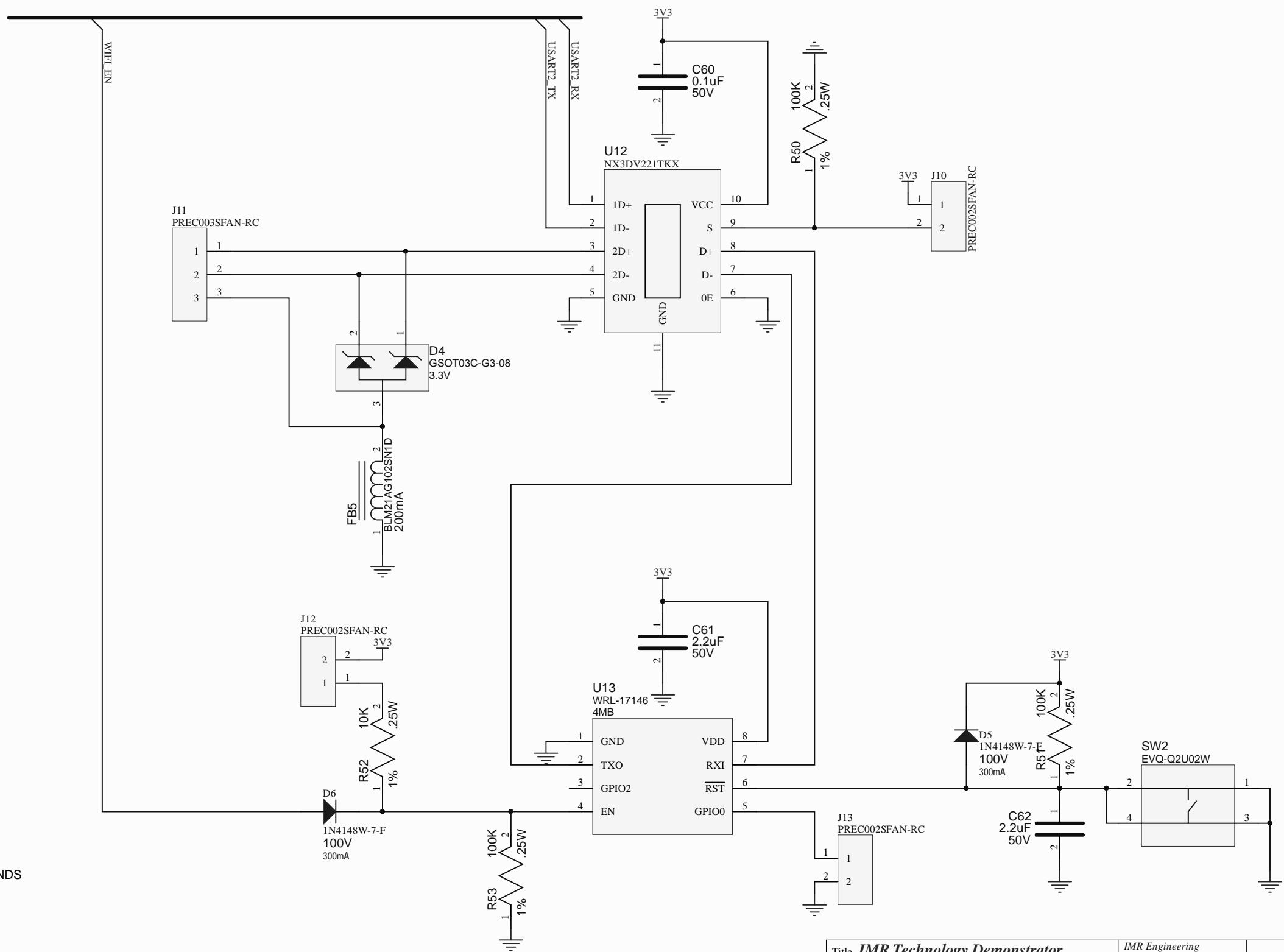
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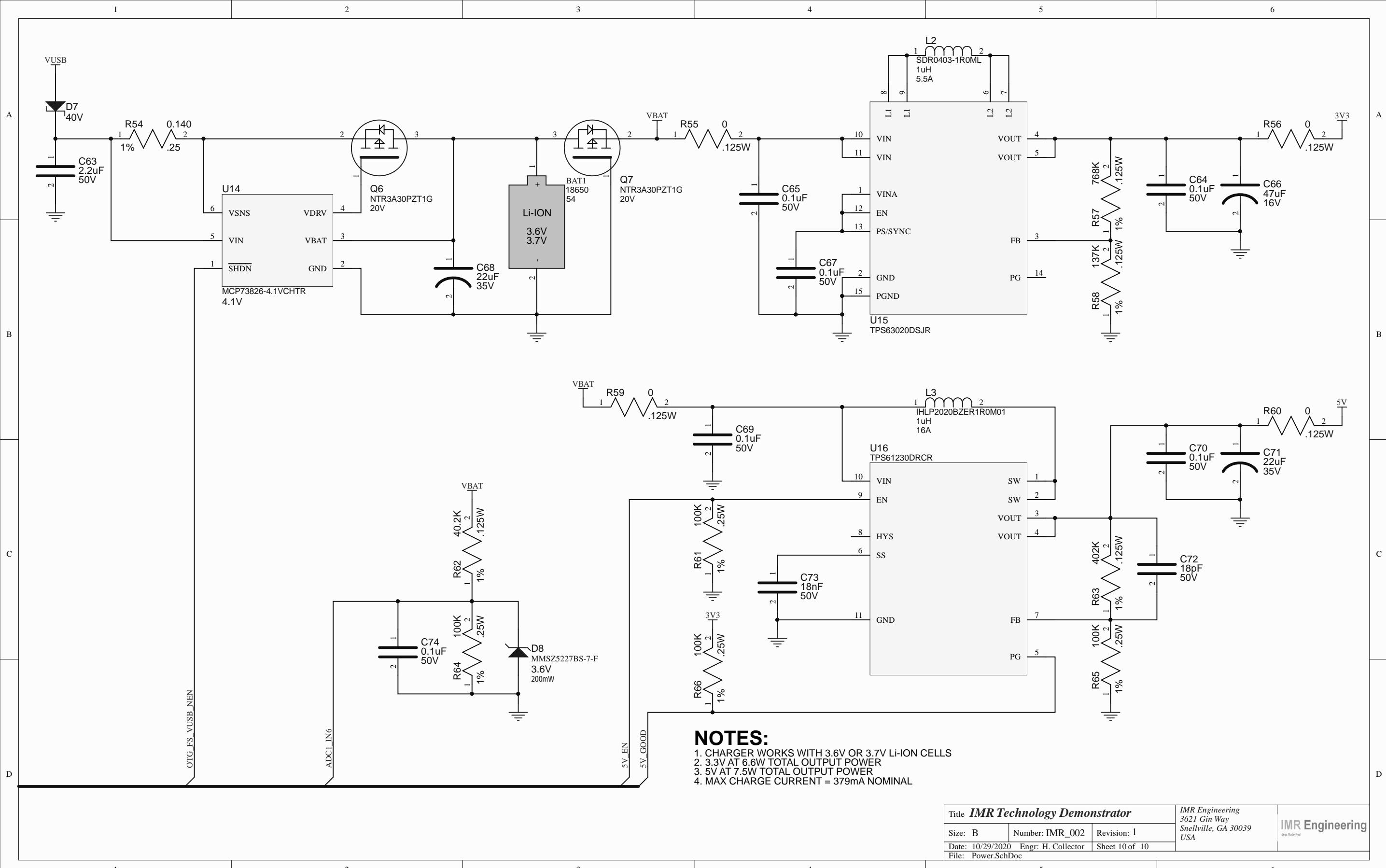
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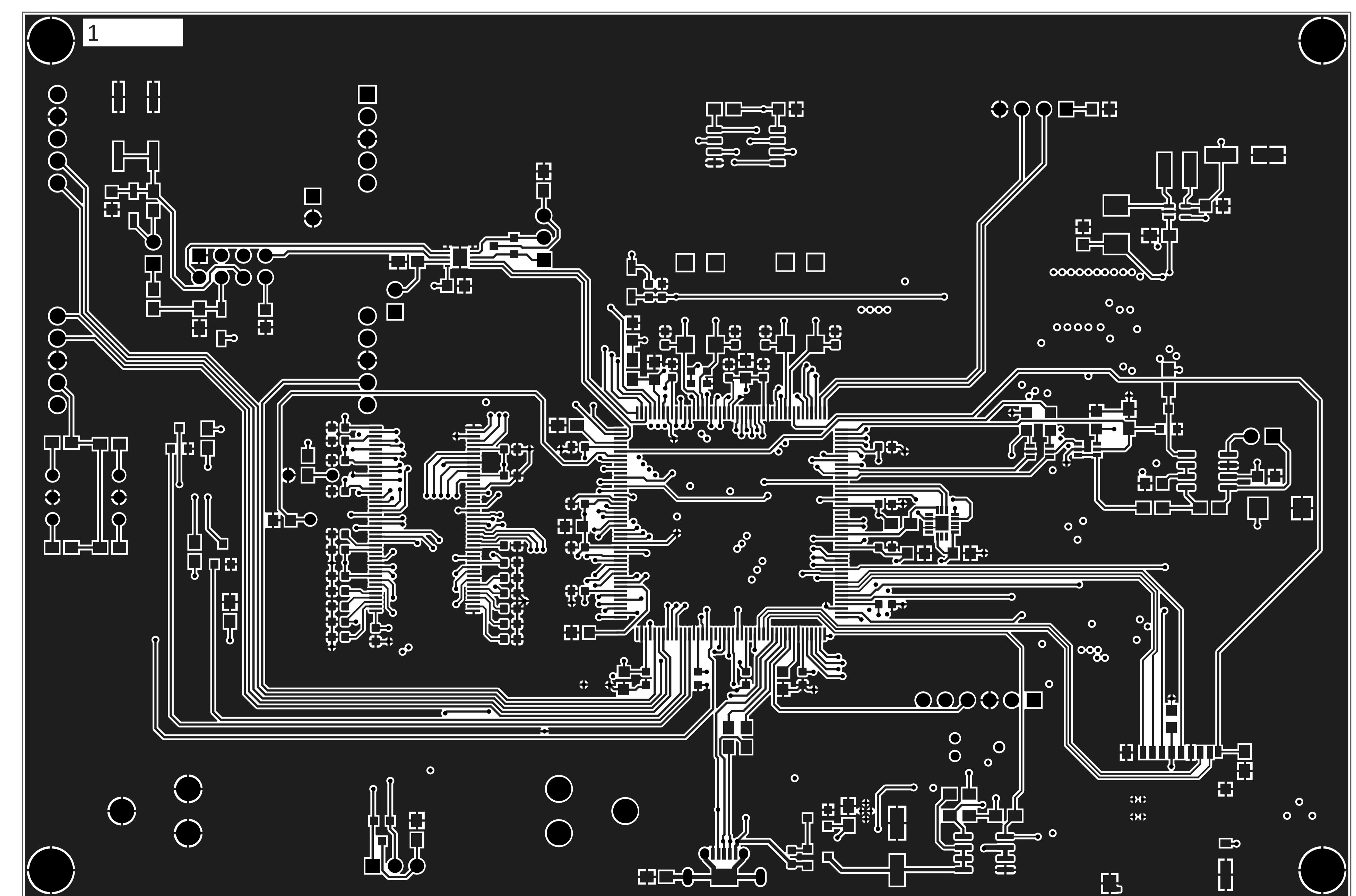
D

## WIFI ACCESS NOTES:

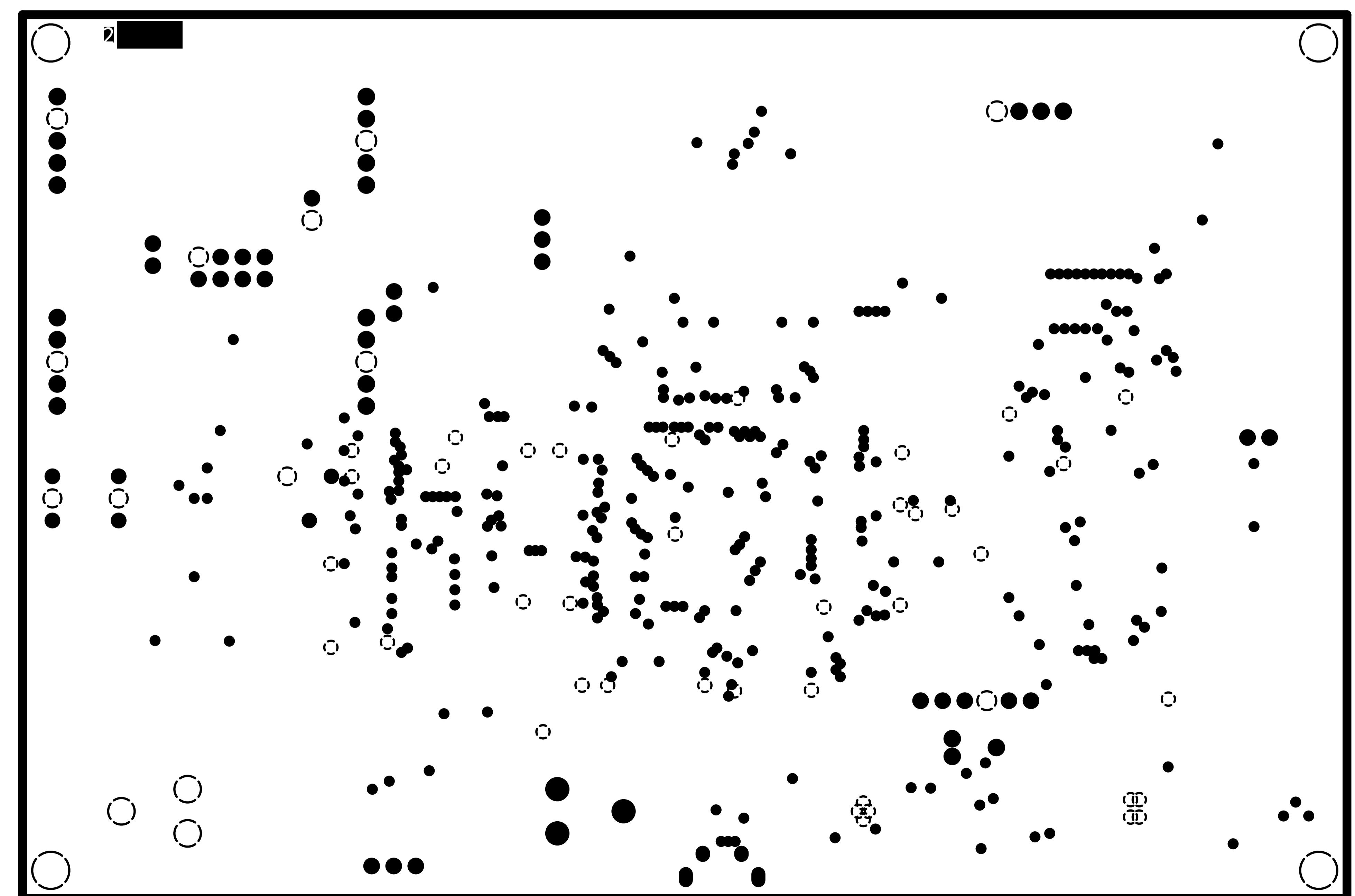
1. SYSTEM ACCESS:  
DO NOT INSTALL JUMPER JA, JB, JC  
DO NOT RESET VIA SW#
2. EXTERNAL UART ACCESS:  
RESET VIA SW#  
INSTALL JUMPER JA AND JB FOR AT COMMANDS  
INSTALL JUMPER JC TO PROGRAM



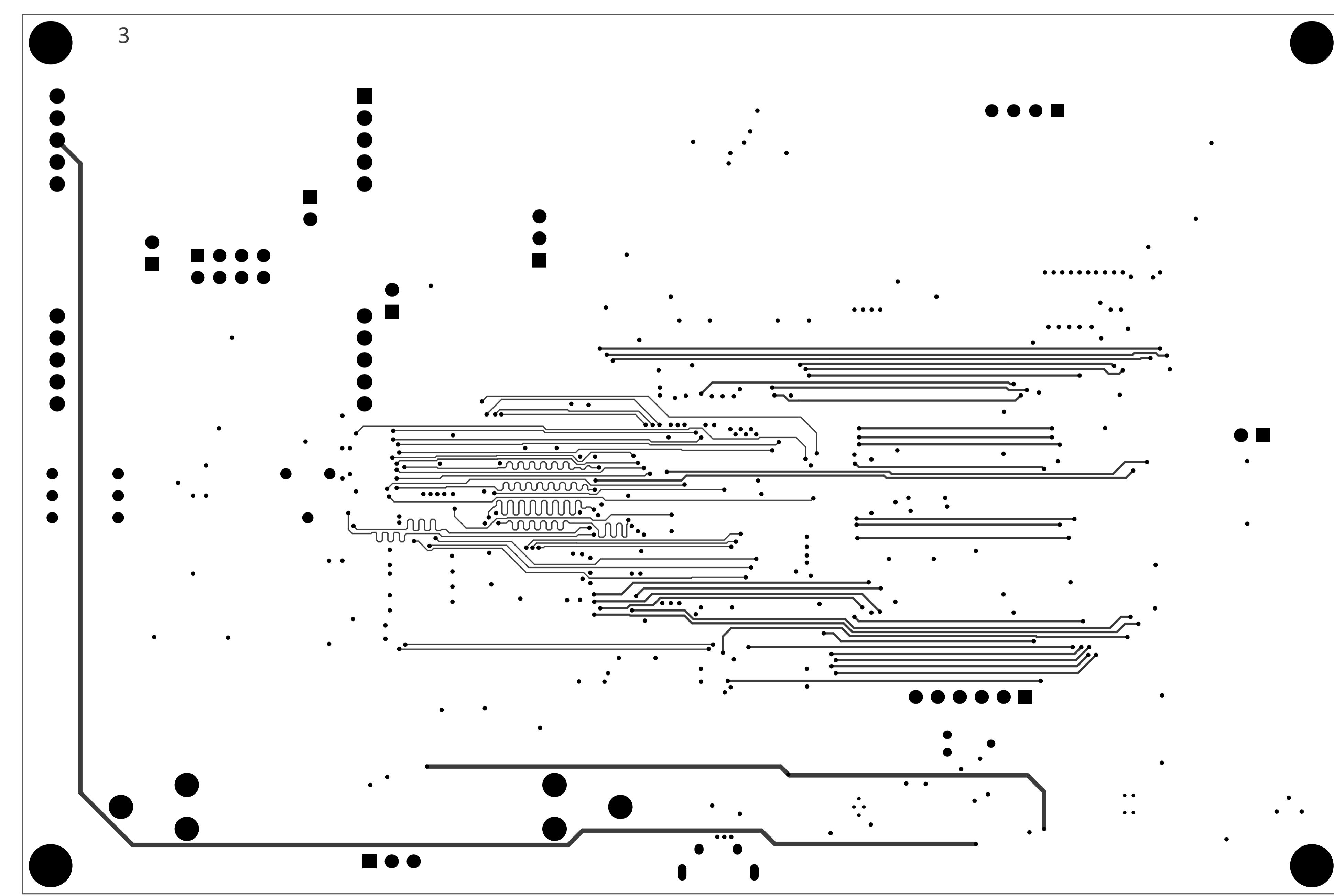




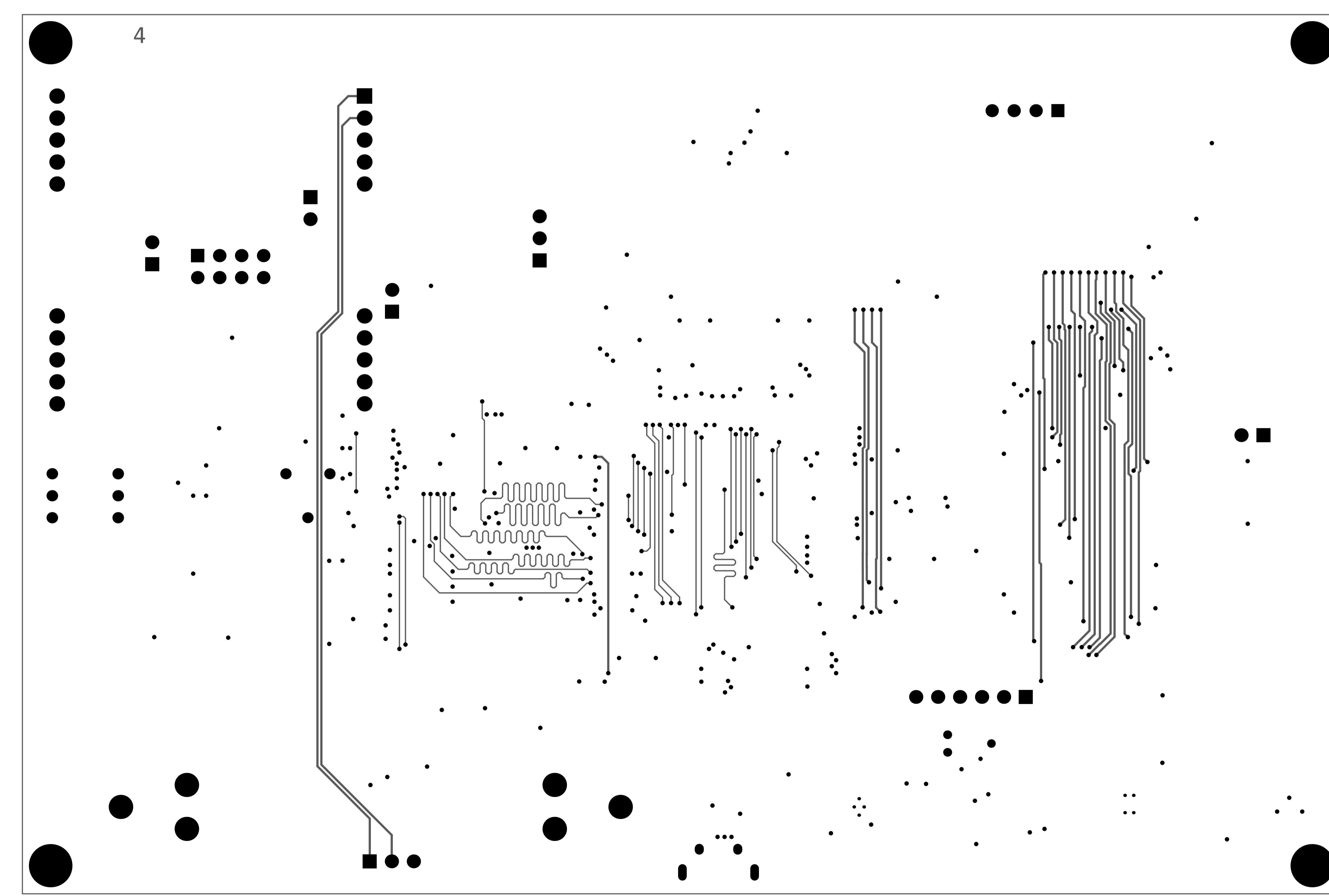
TOP



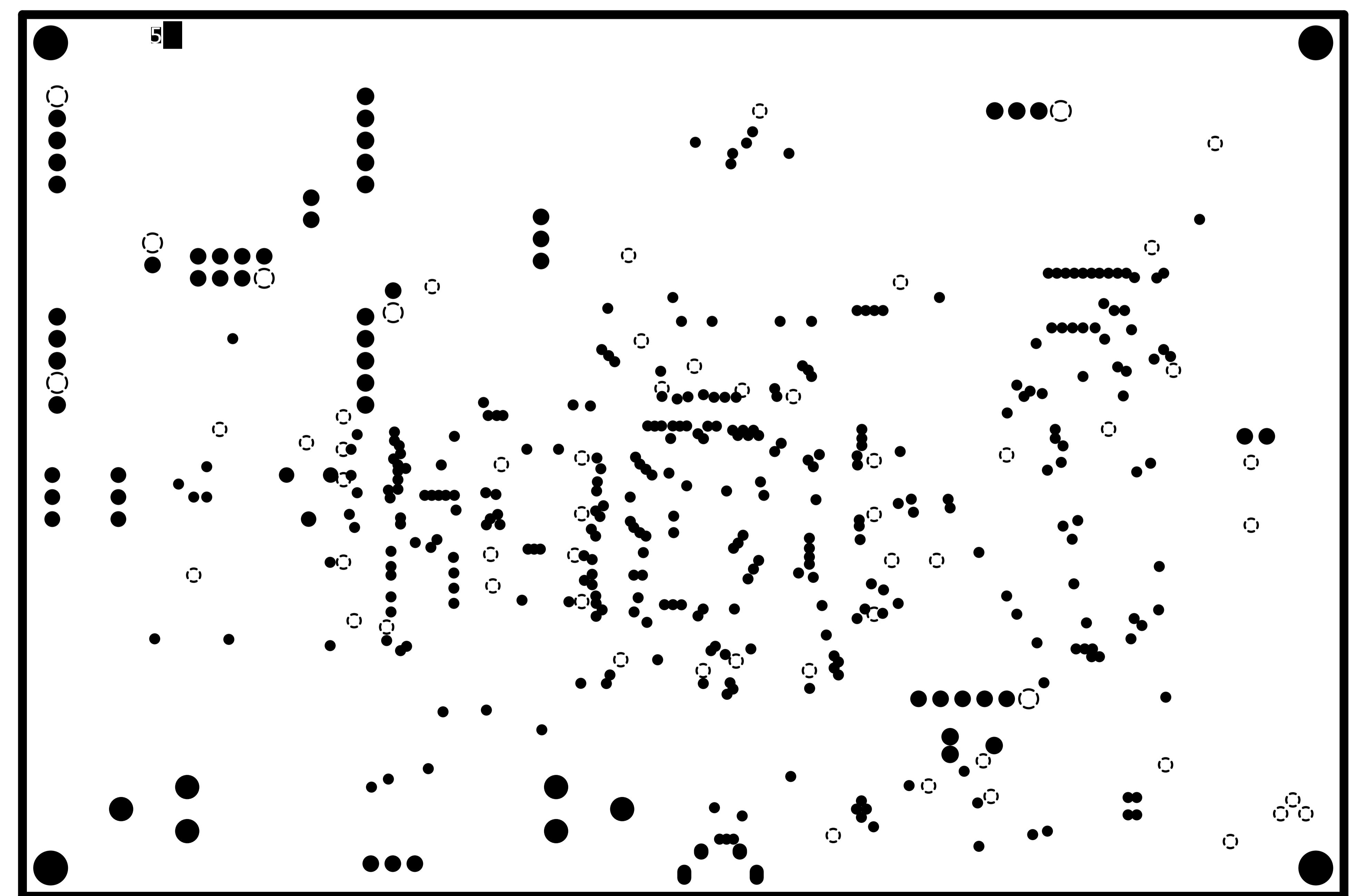
GND PLANE



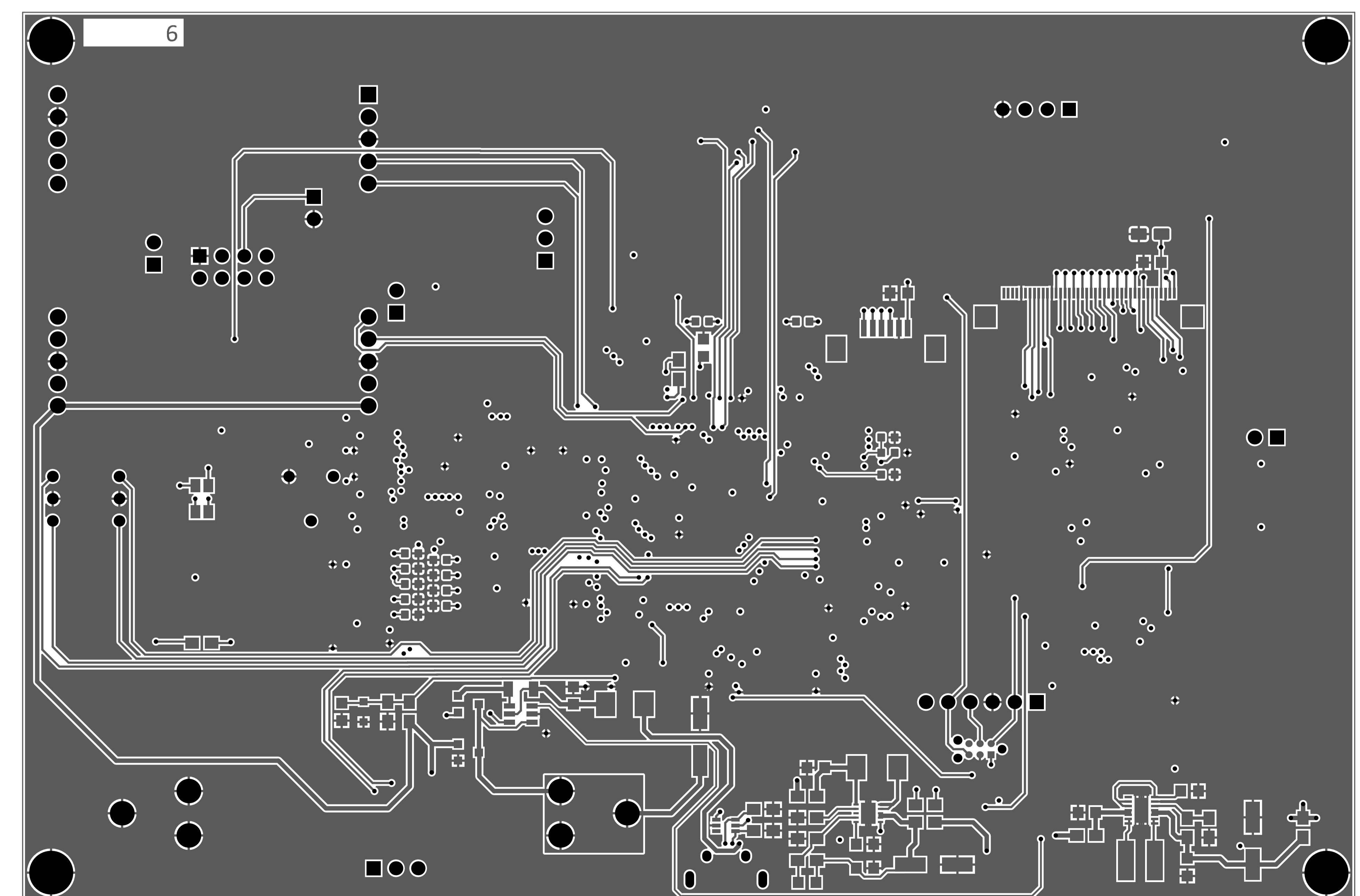
INNER SIGNAL 2



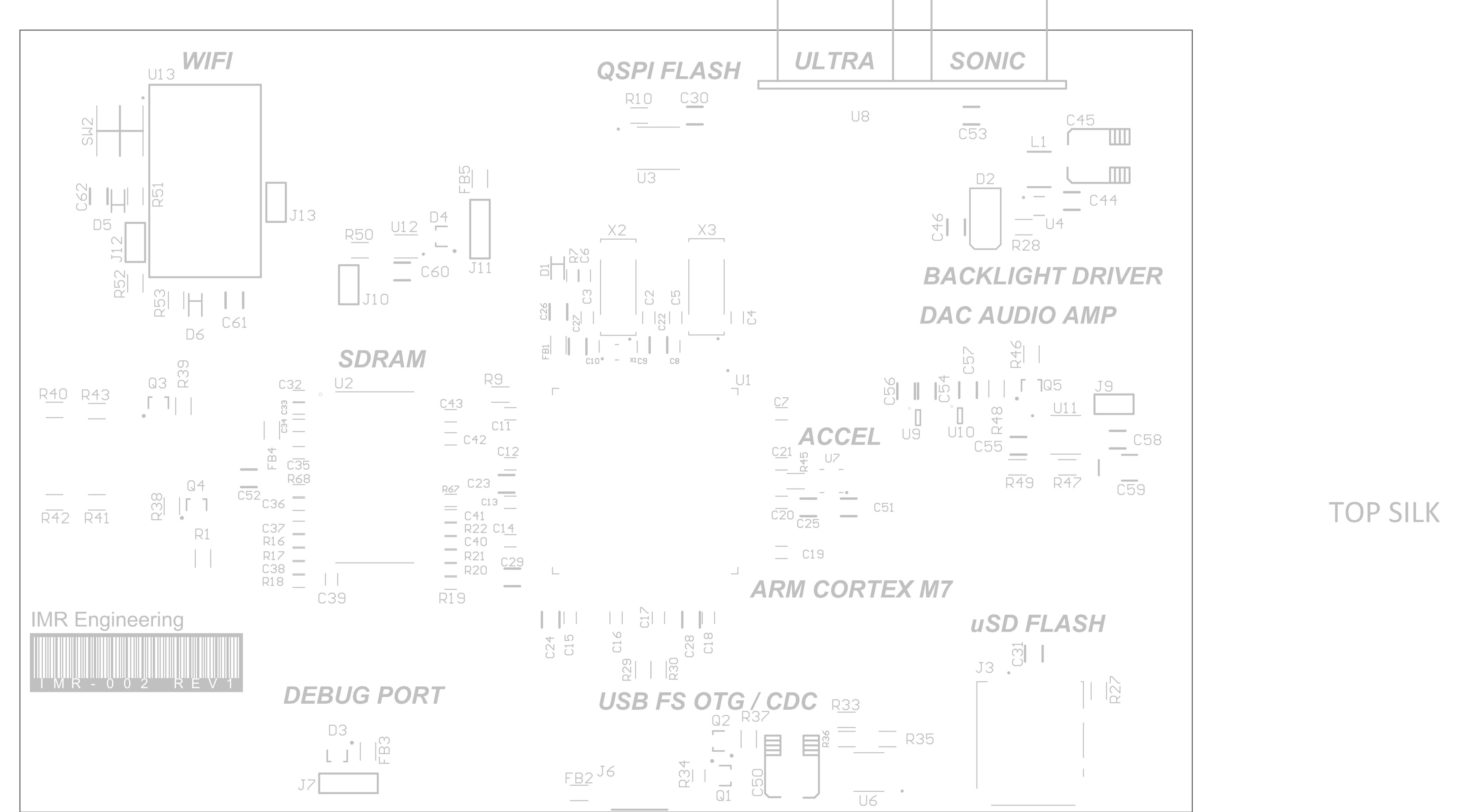
INNER SIGNAL 3

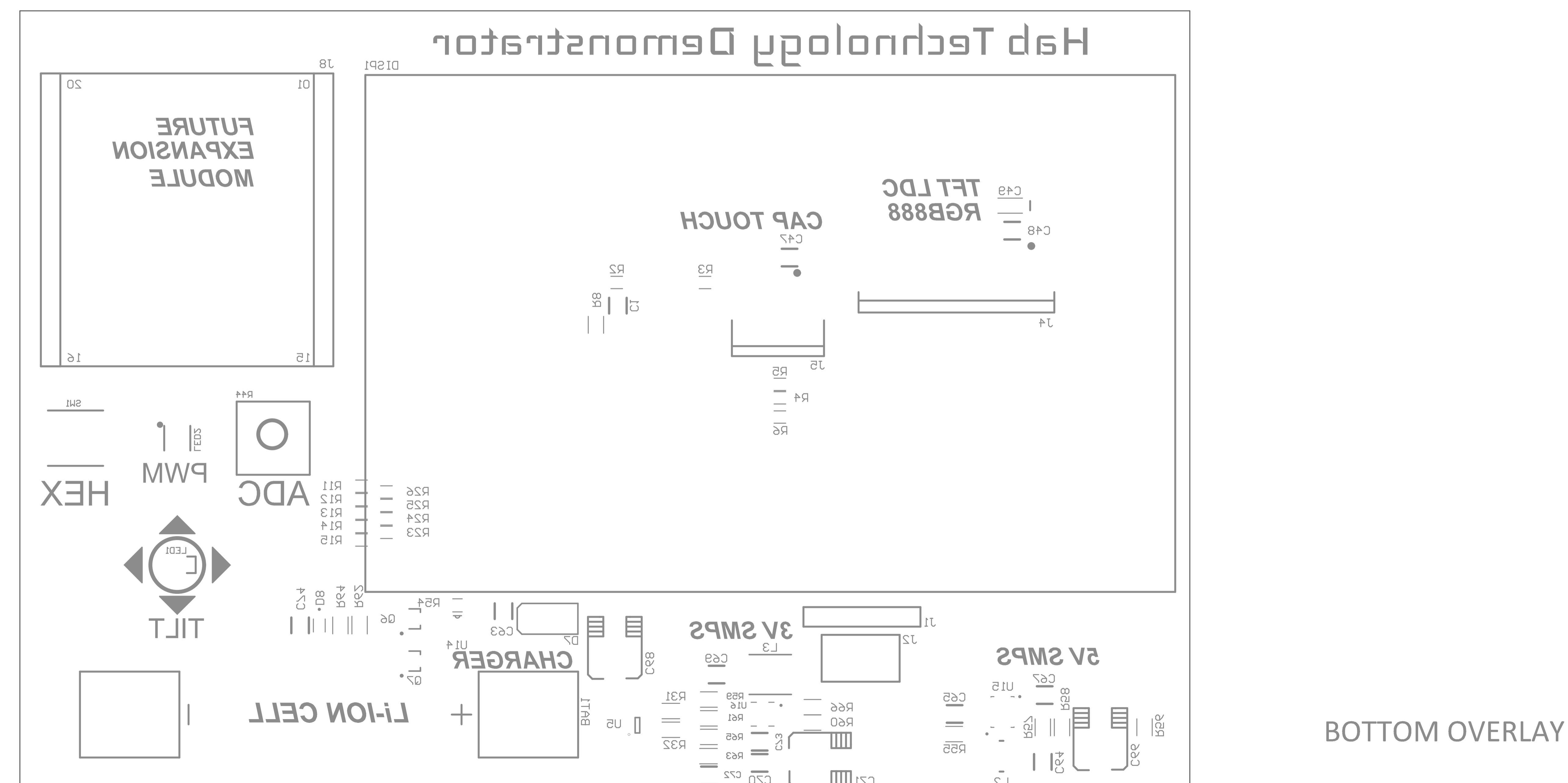


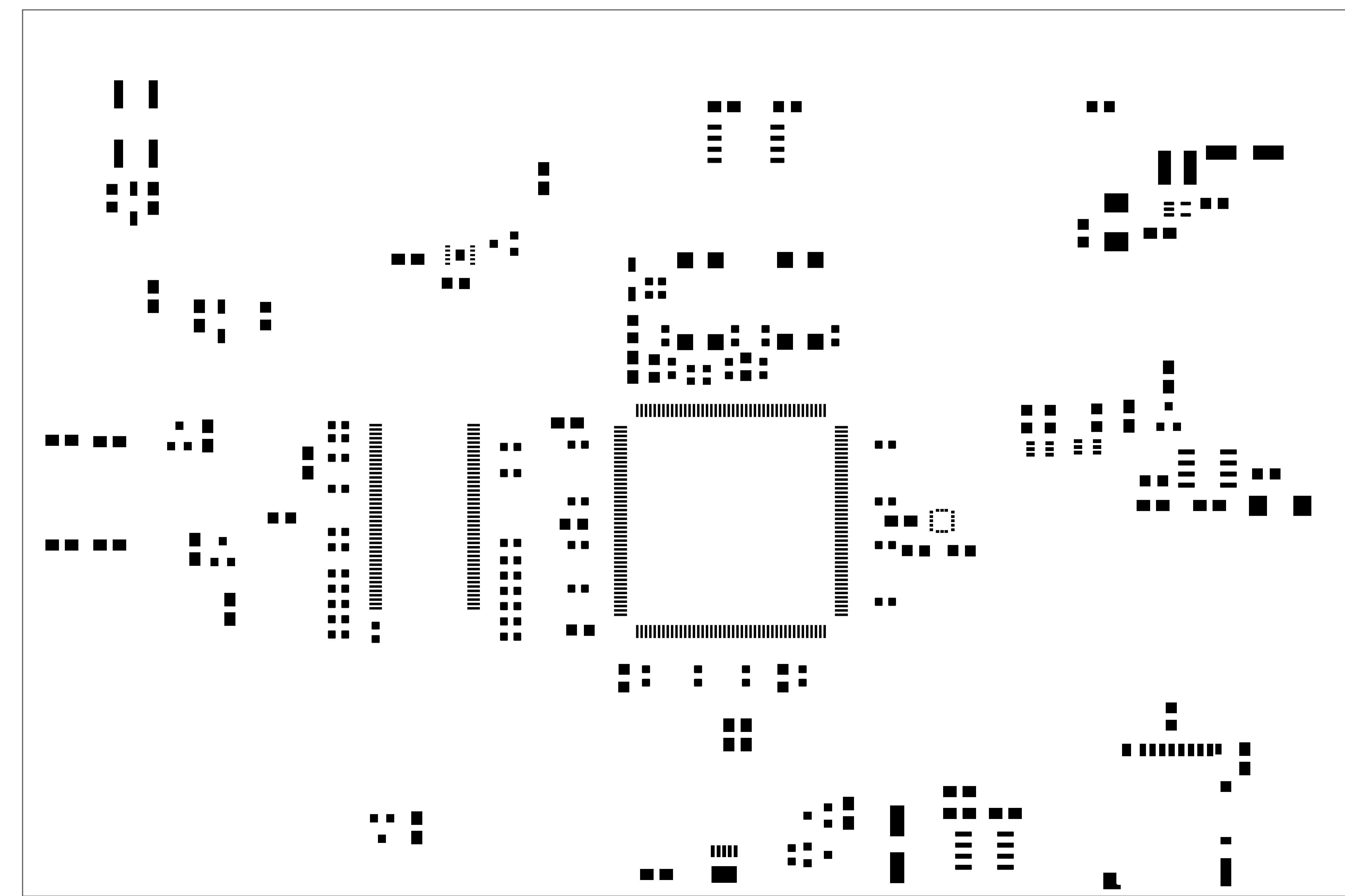
PWR PLANE



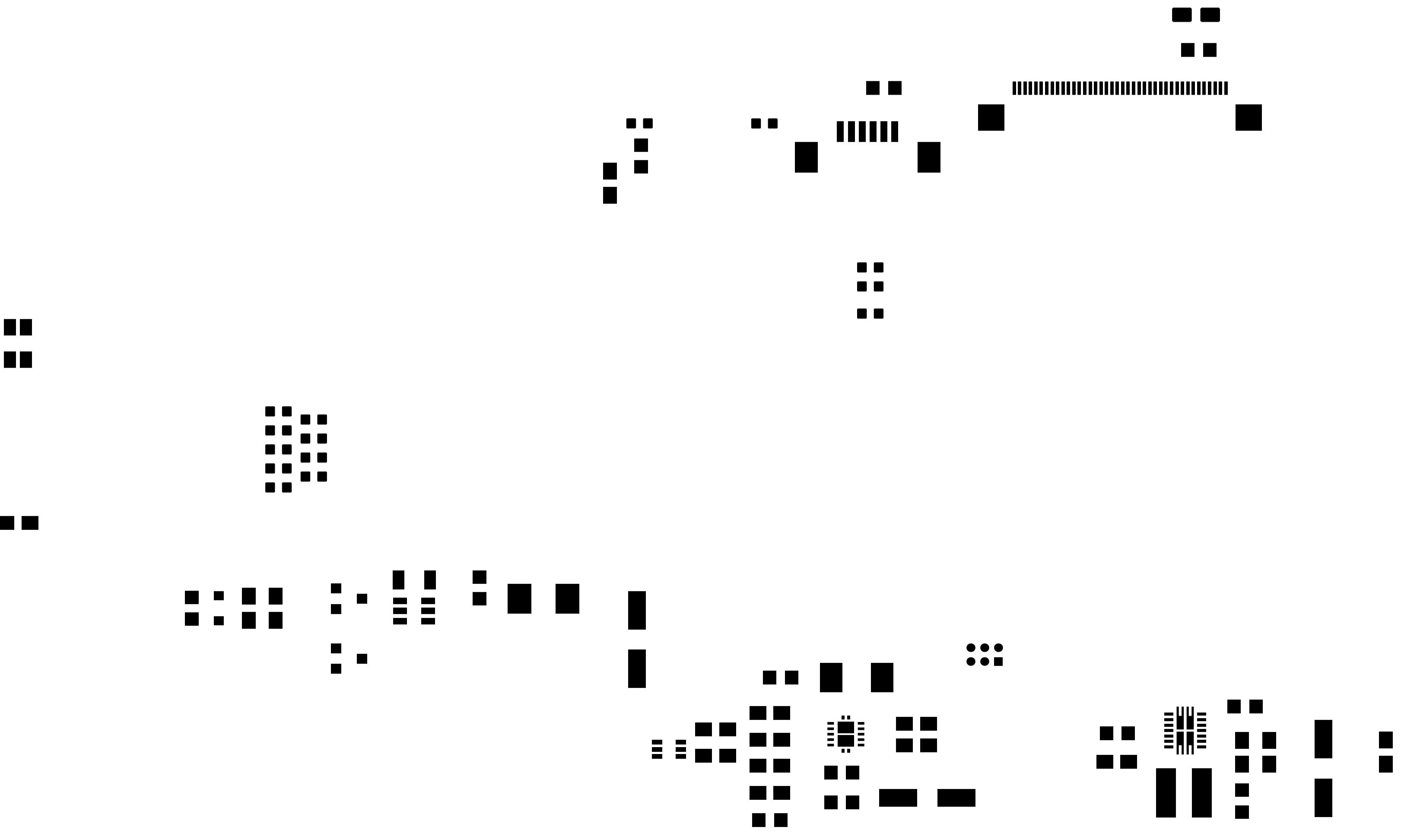
BOTTOM SIGNAL



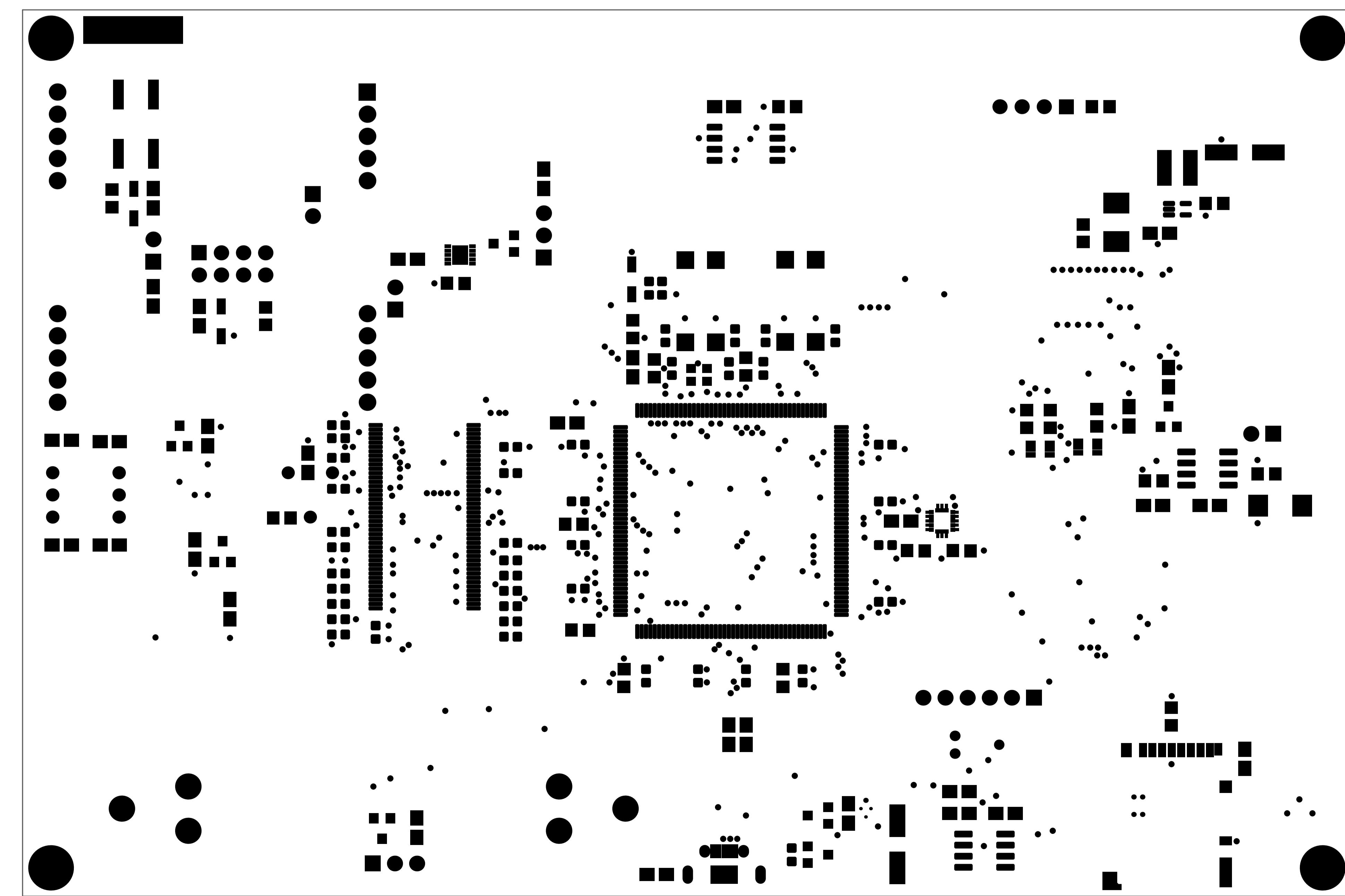




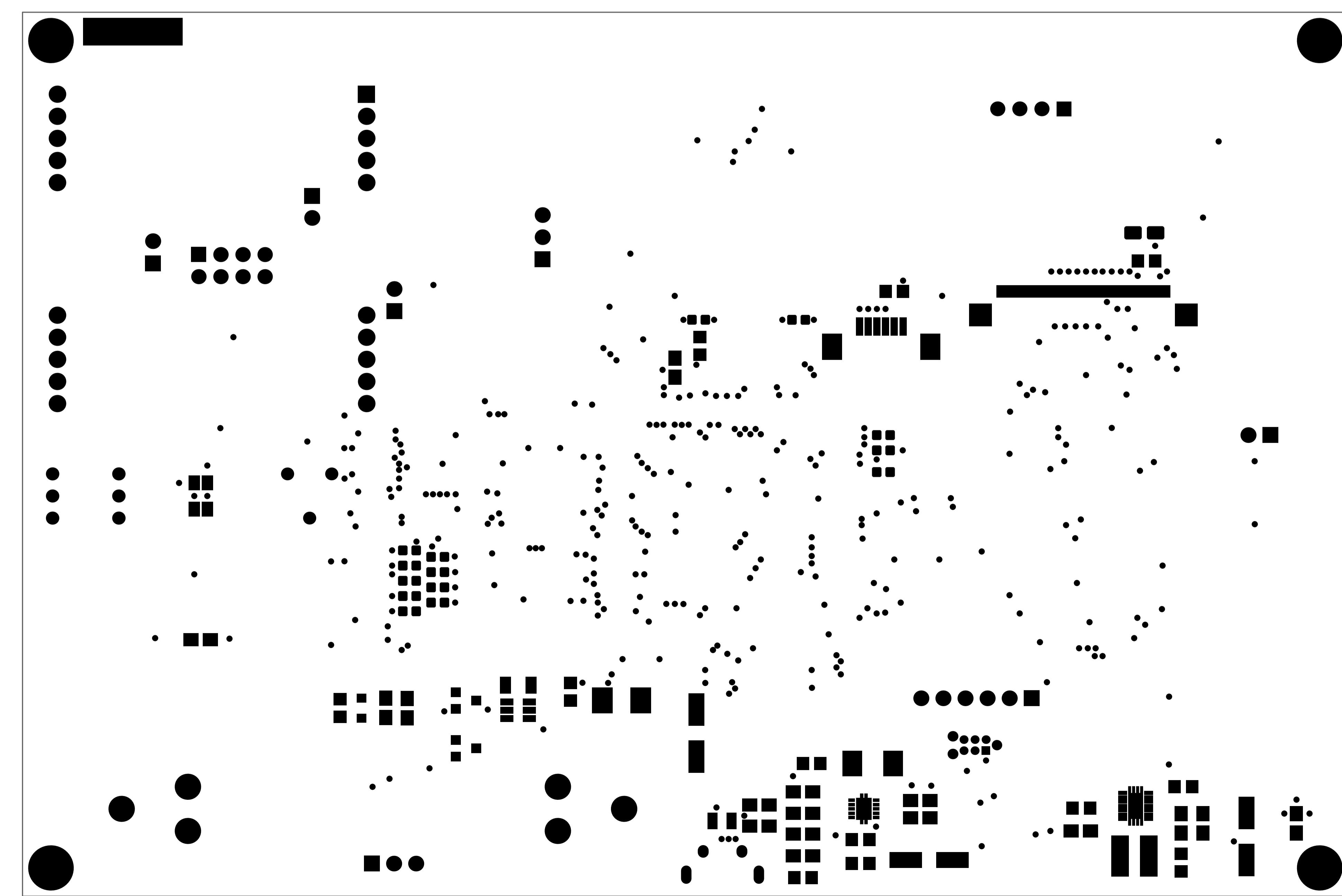
TOP PM



BOTTOM PM



TOP SM



BOTTOM SM

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Hole Tolerance (+)	Hole Tolerance (-)
x	366	10.00mil <0.254mm>	PTH	Round	Top Layer - Bottom Layer	(Mixed)	Rounded	(Mixed)		
◊	2	23.62mil <0.600mm>	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r100_190h60_130r100		
x	2	25.59mil <0.650mm>	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r105_125h65_85r100		
◊	3	30.00mil <0.762mm>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c127h76		
▽	6	31.50mil <0.800mm>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c130h80		
○	8	35.00mil <0.889mm>	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)		
□	20	35.43mil <0.900mm>	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)		
◊	3	39.37mil <1.000mm>	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)		
+	4	39.37mil <1.000mm>	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)		
x	20	40.00mil <1.016mm>	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)		
□	6	70.00mil <1.778mm>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c279h178		
▽	4	118.11mil <3.000mm>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c500h300		
444 Total										

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.  
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	SM-001	1.00mil	4		
3	Top Layer	Copper	1.38mil			
4	Dielectric 1	PP-006	2.80mil	4.1		
5	Dielectric 2	PP-006	2.80mil	4.1		
6	GND_Plane	Copper	1.38mil			
7	Dielectric 3	Core-035	18.00mil	4.7		
8	Int2 (Sign)	Copper	1.38mil			
9	Dielectric 4	PP-006	2.80mil	4.1		
10	Dielectric 5	PP-006	2.80mil	4.1		
11	Int3 (Sign)	Copper	1.38mil			
12	Dielectric 6	Core-035	18.00mil	4.7		
13	PWR_Plane	Copper	1.38mil			
14	Dielectric 7	PP-006	2.80mil	4.1		
15	Dielectric 8	PP-006	2.80mil	4.1		
16	Bottom Layer	Copper	1.38mil			
17	Bottom Solder	SM-001	1.00mil	4		
18	Bottom Overlay					

## PCB FABRICATION NOTES:

### MATERIAL:

FR4 (GF per MIL-P-13949) MIN UL 94V0

### Cu WEIGHT:

OUTER LAYER: 1oz

INNER LAYER: STANDARD (SEE LAYER STACK)

### SOLDER MASK:

TYPE: LPI (LIQUID PHOTO-IMAGE)

COVER: SMOBC (SOLDER MASK OVER BARE Cu)

COLOR: RED

### OVERALL PCB THICKNESS:

PCB: 63MIL (SEE LAYER STACK)

TOLERANCE: 7MIL

### PCB ELECTRICAL TEST

TESTED TO GERBER DATA

PURCHASE ORDER TO OVERRIDE

### HOLE DIAMETER TOLERANCE:

PLATED HOLE TOLERANCE: 3MIL

NON PLATED HOLE TOLERANCE: 3MIL

### SILK SCREEN

SIDES: TOP AND BOTTOM

COLOR: WHITE

### ACCEPTABILITY:

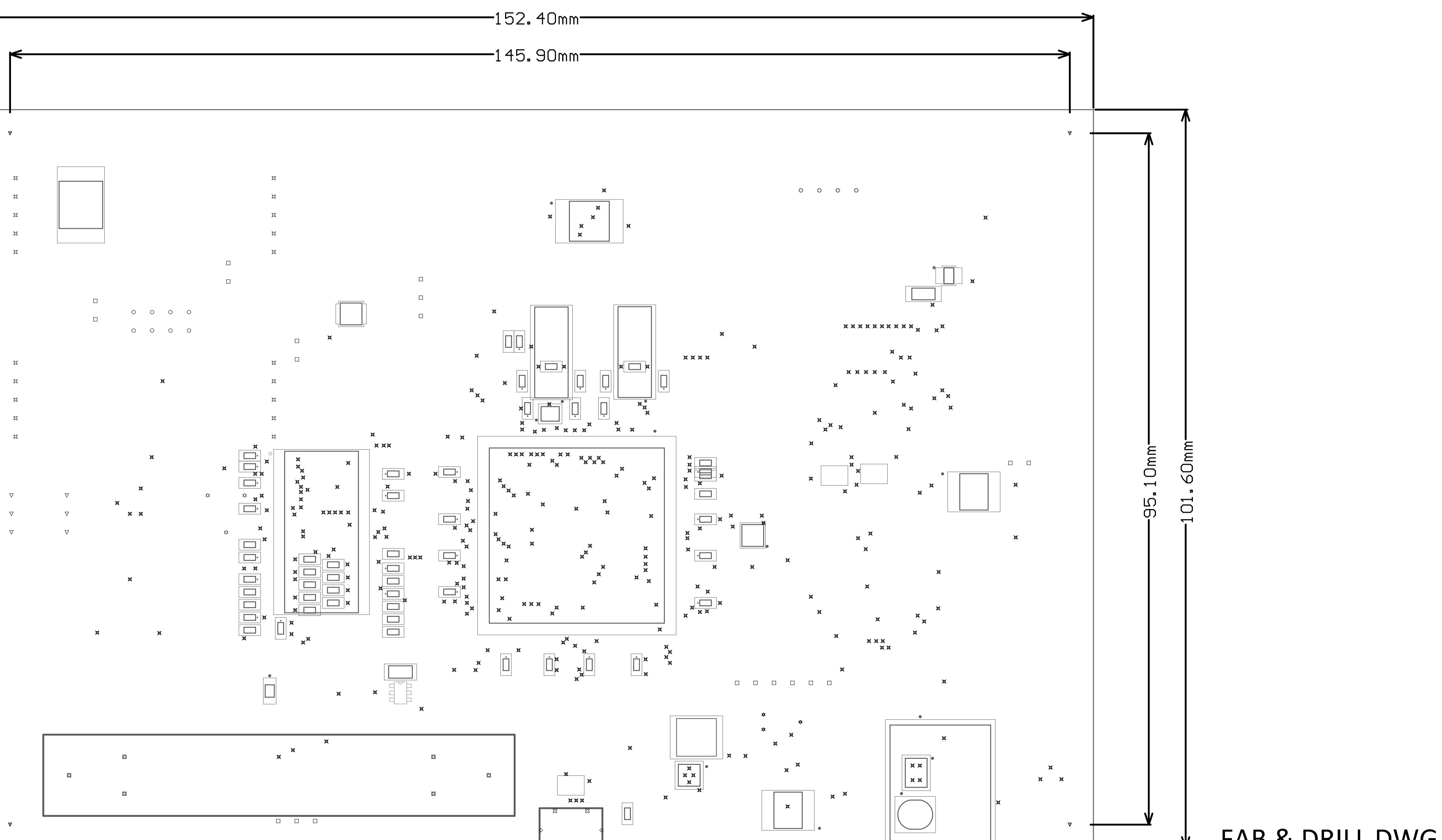
STANDARD: IPC-A-600 (LATEST REV)

MFG TO ADD: DATE CODE, UL FLAME CODE

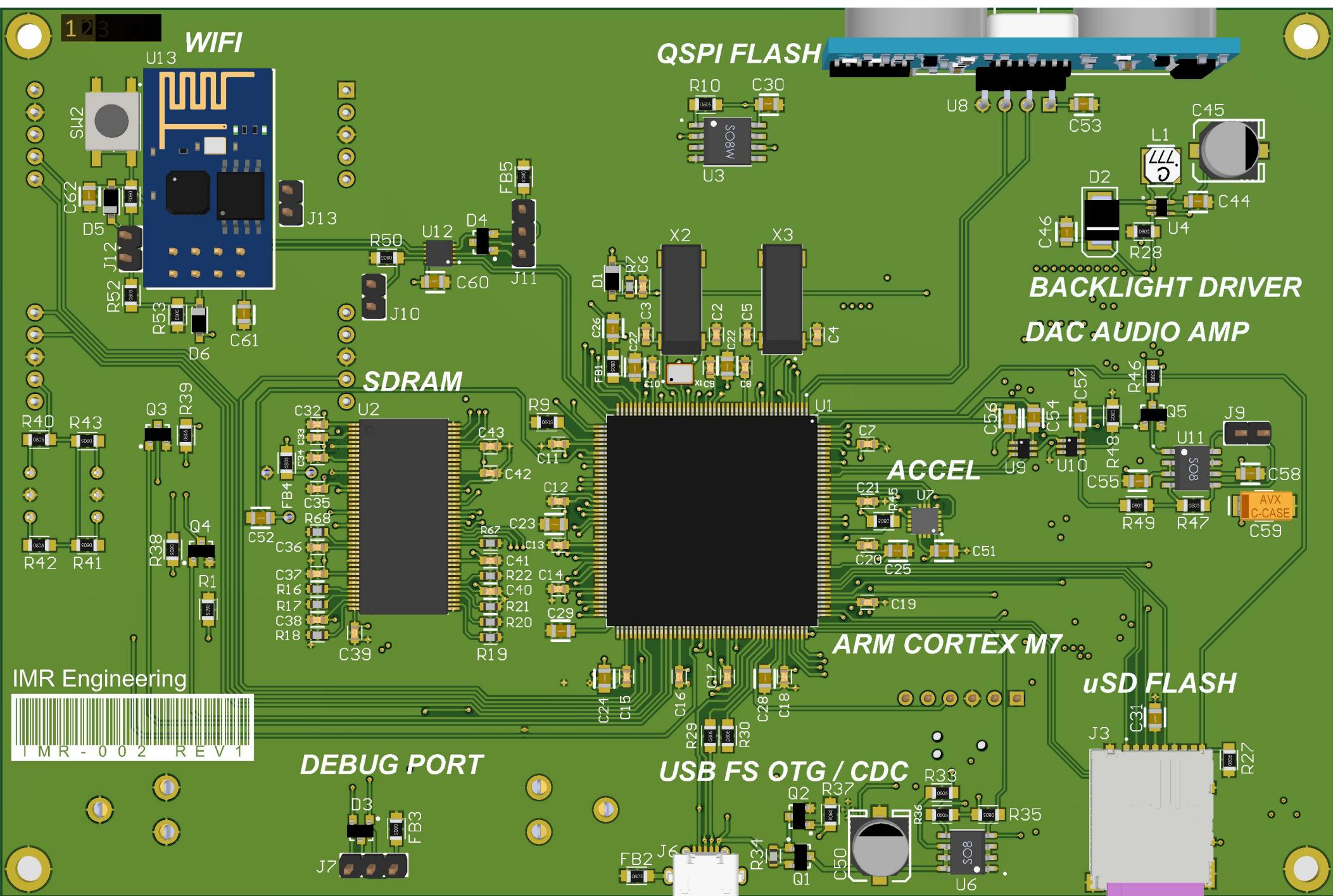
### SURFACE FINISH:

PROTOTYPE: HASL OR EING

PRODUCTION: ENIG (PER PO)



FAB & DRILL DWG



# Hab Technology Demonstrator

