

Schéma obvodového zapojení výukového kitu Minerva



evropský
sociální
fond v ČR



EVROPSKÁ UNIE

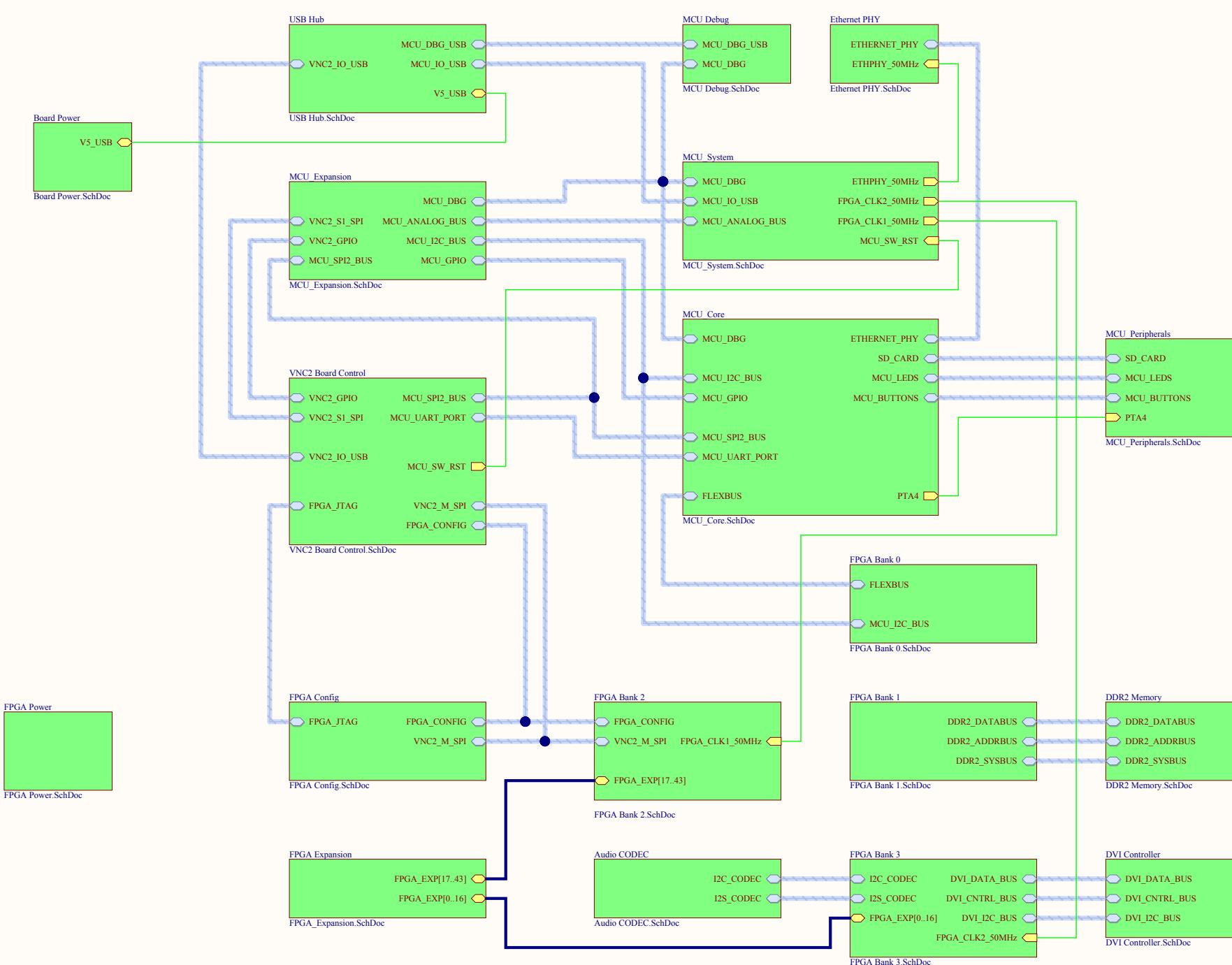


MINISTERSTVO ŠKOLSTVÍ,
MLÁDEŽE A TĚLOVÝCHOVY

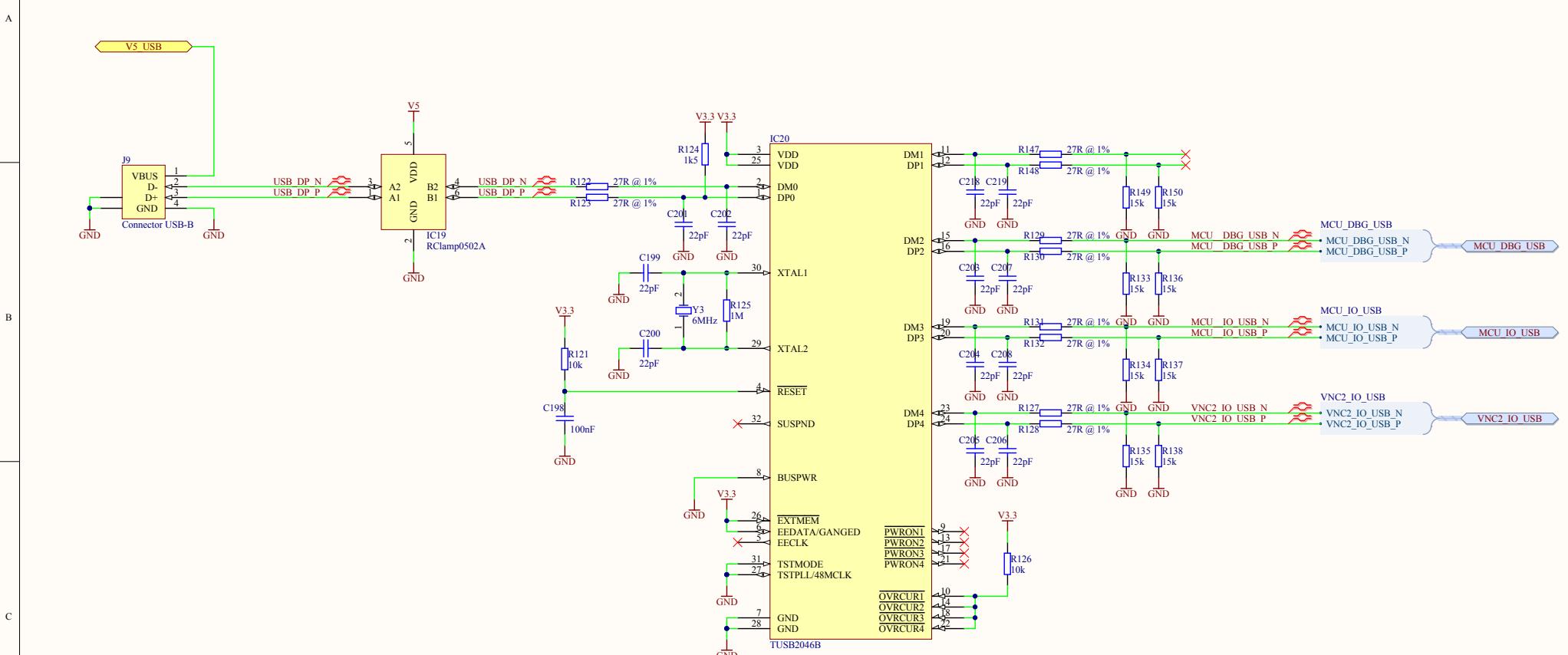


OP Vzdělávání
pro konkurenčeschopnost

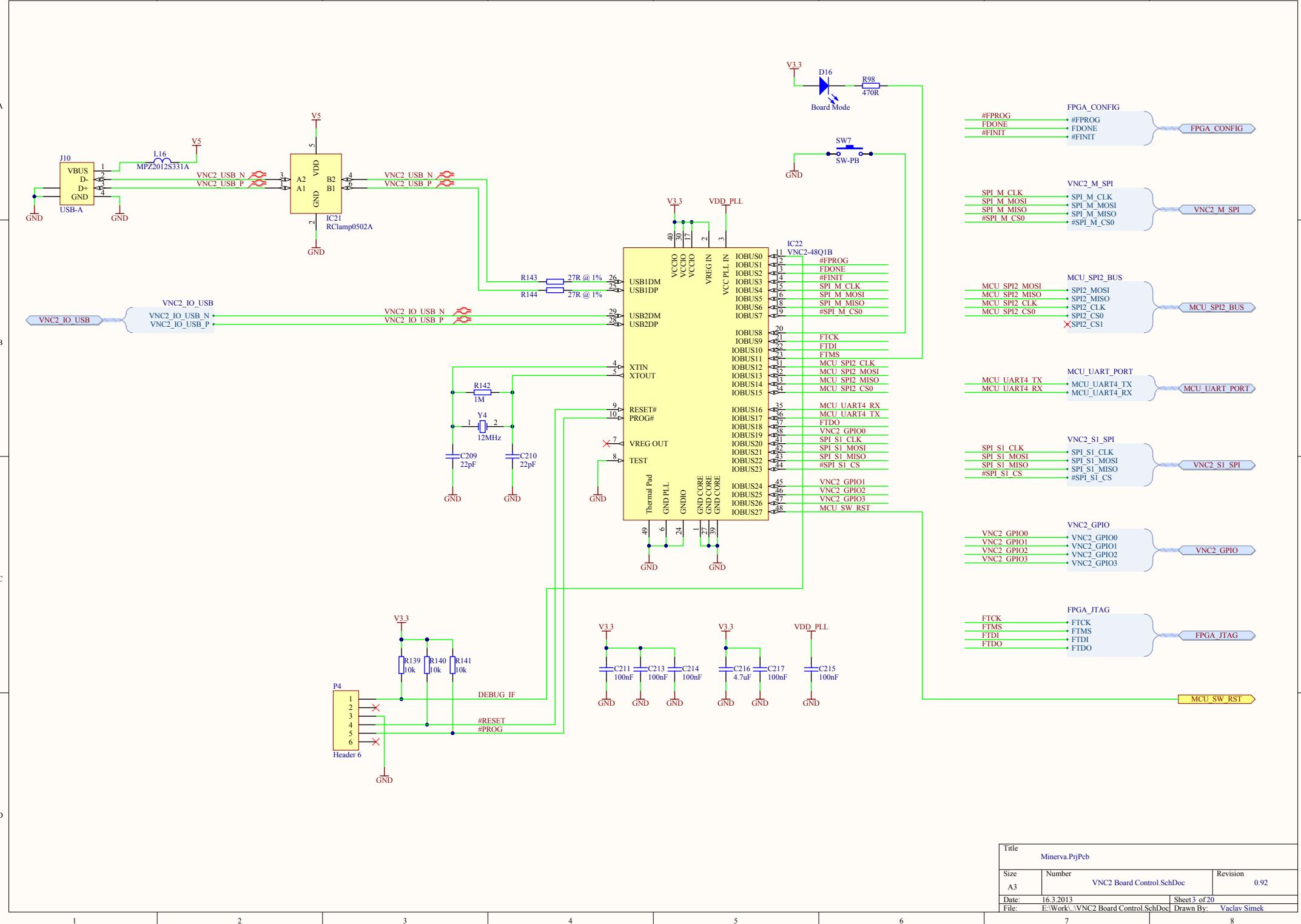
INVESTICE DO ROZVOJE VZDĚLÁVÁNÍ



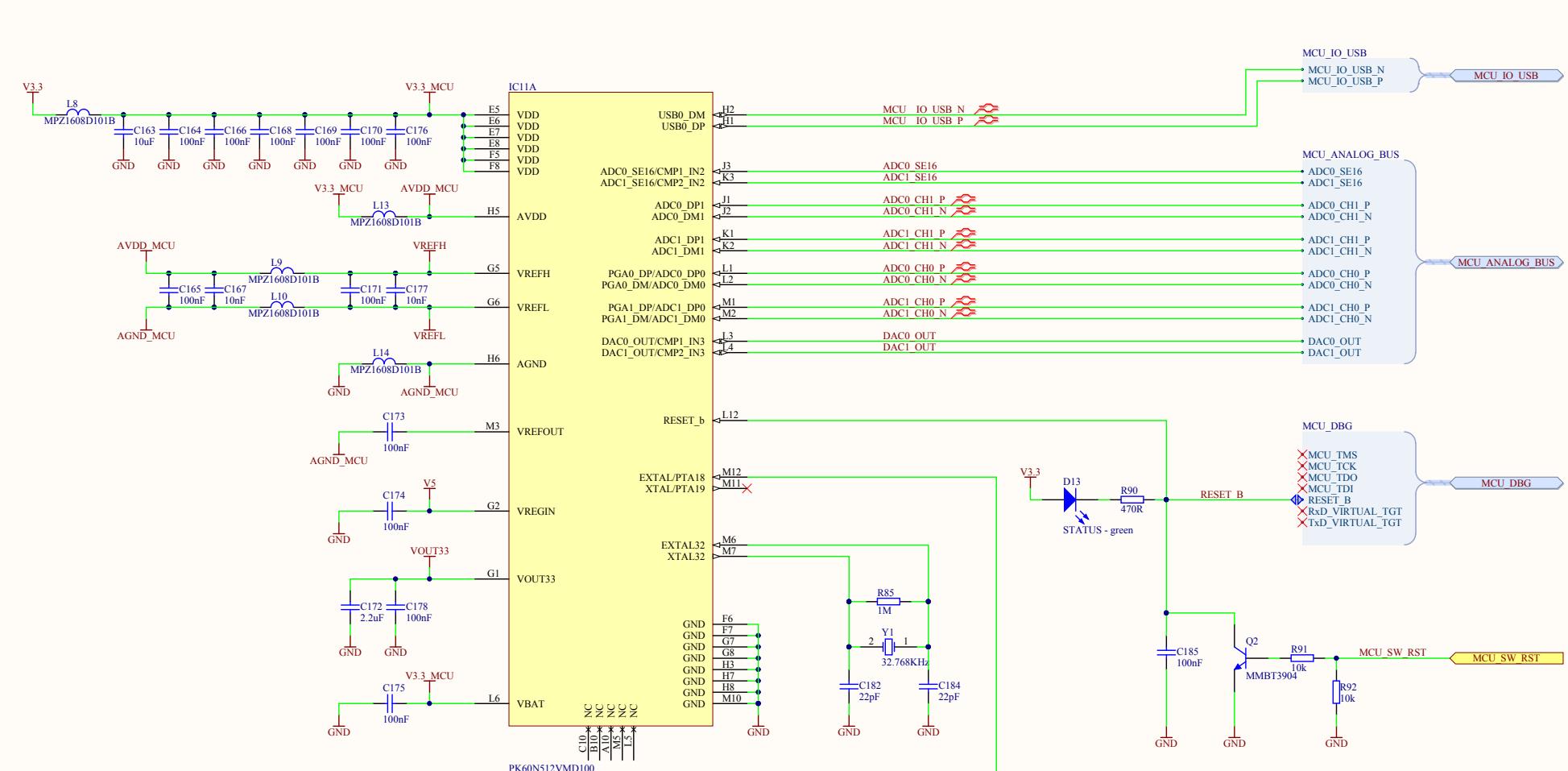
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Size A3	Number Minerva.SchDoc	Revision 092	
Date: 16.3.2013		Sheet 1 of 20	
File: E:\Work\...\Minerva.SchDoc		Drawn By: Vaclav Simek	



Title Minerva.PrjPcb		
Size A3	Number USB Hub.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet of 20	
File: E:\Work\USB Hub.SchDoc	Drawn By: Vaclav Simek	

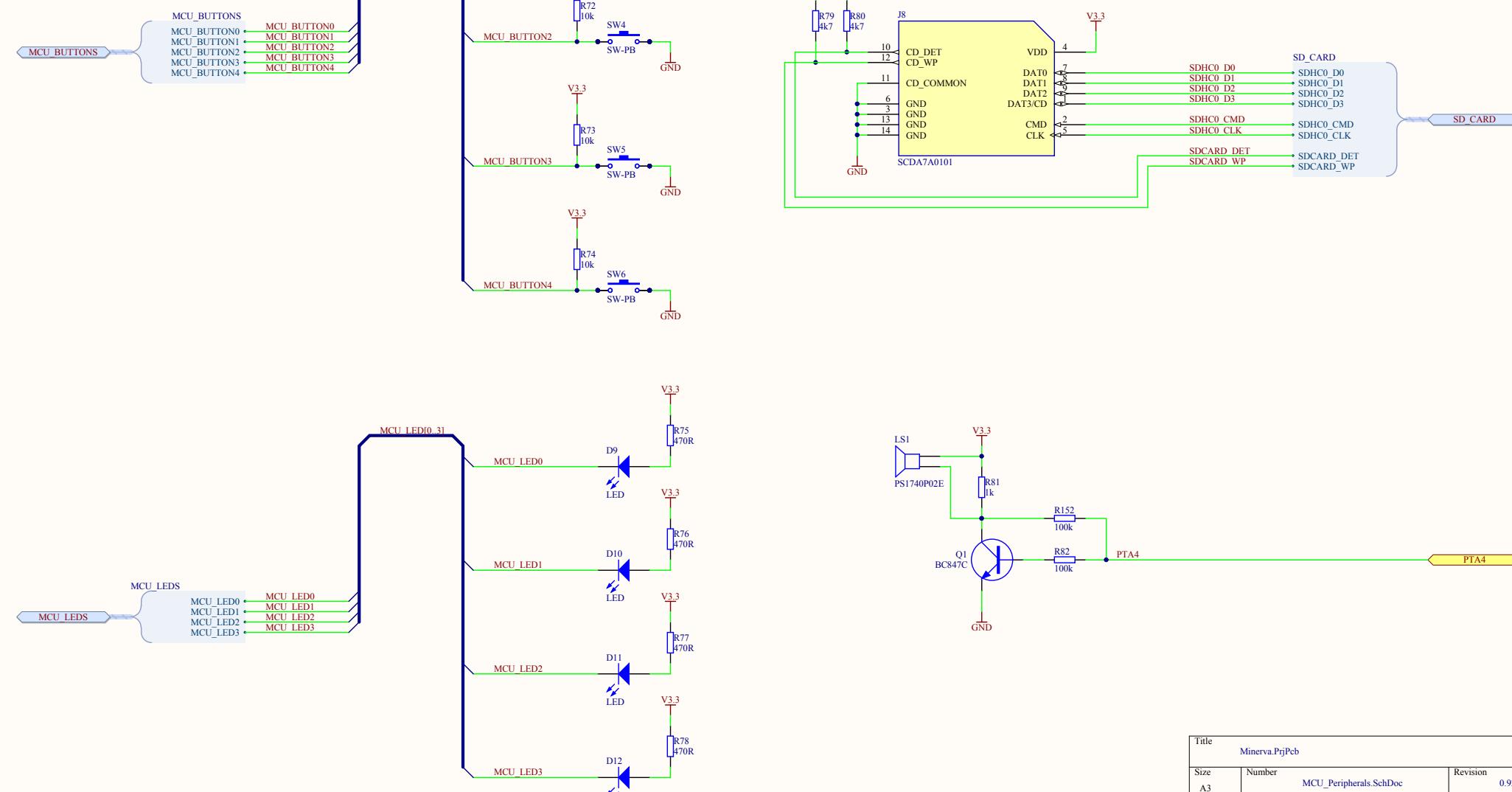


Title Minerva.PjPcb		
Size A3	Number VNC2 Board Control.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet 3 of 20	
File: E:\Work_\VNC2 Board Control.SchDoc	Drawn By: Vaclav Simek	

Title
Minerva.PjPcb

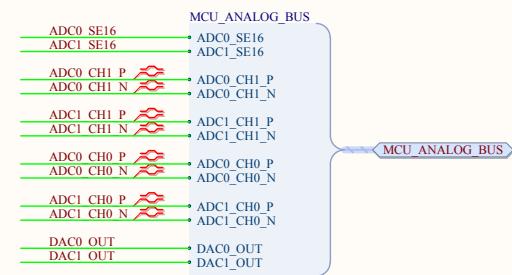
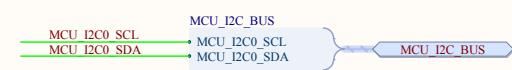
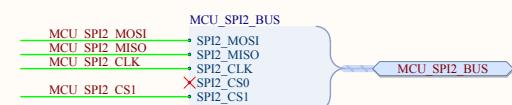
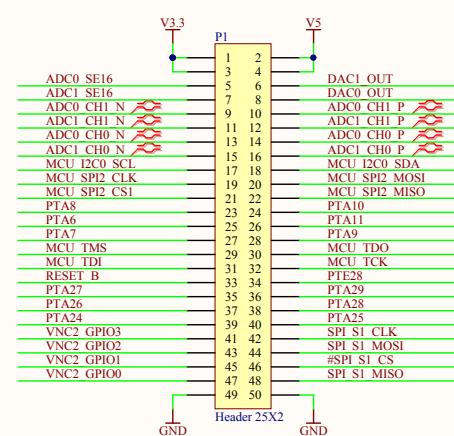
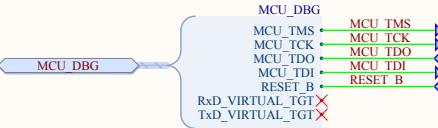
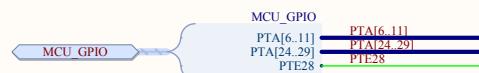
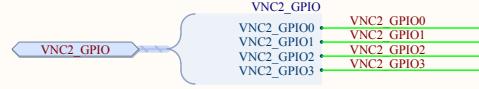
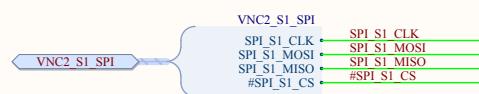
Size	Number	Revision
A3	MCU_System.SchDoc	092
Date:	16.3.2013	Sheet 4 of 20
File:	E:\Work\...\MCU System.SchDoc	Drawn By: Vaclav Simek



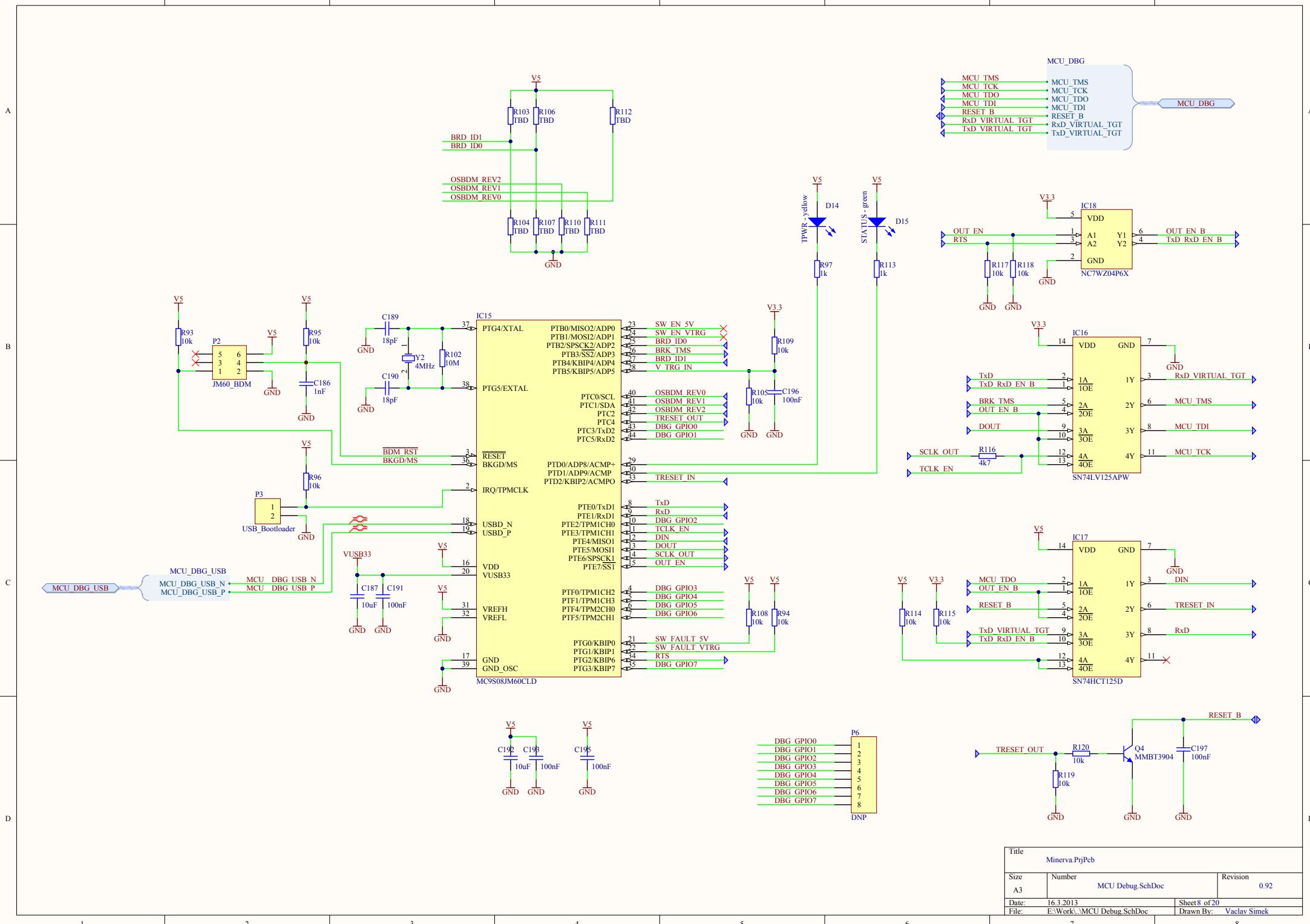


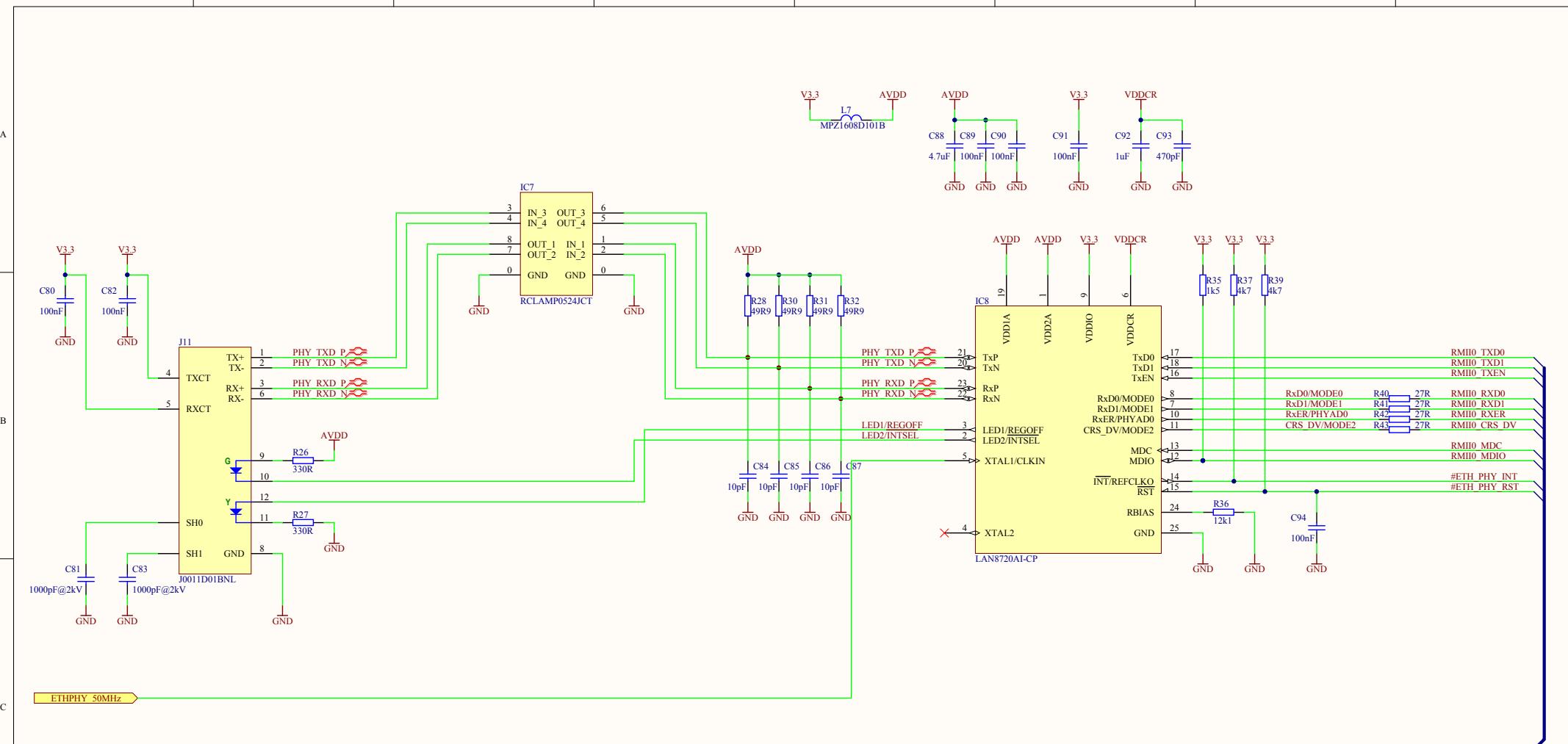
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Size A3	Number MCU_Peripherals.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet 6 of 20	
File: E:\Work_\MCU_Peripherals.SchDoc		Drawn By: Vaclav Simek

A

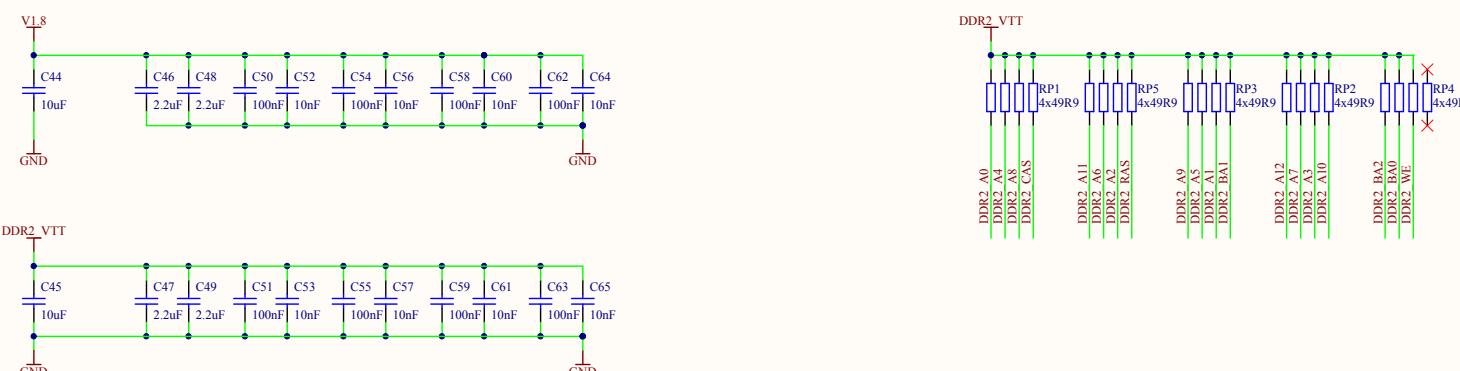
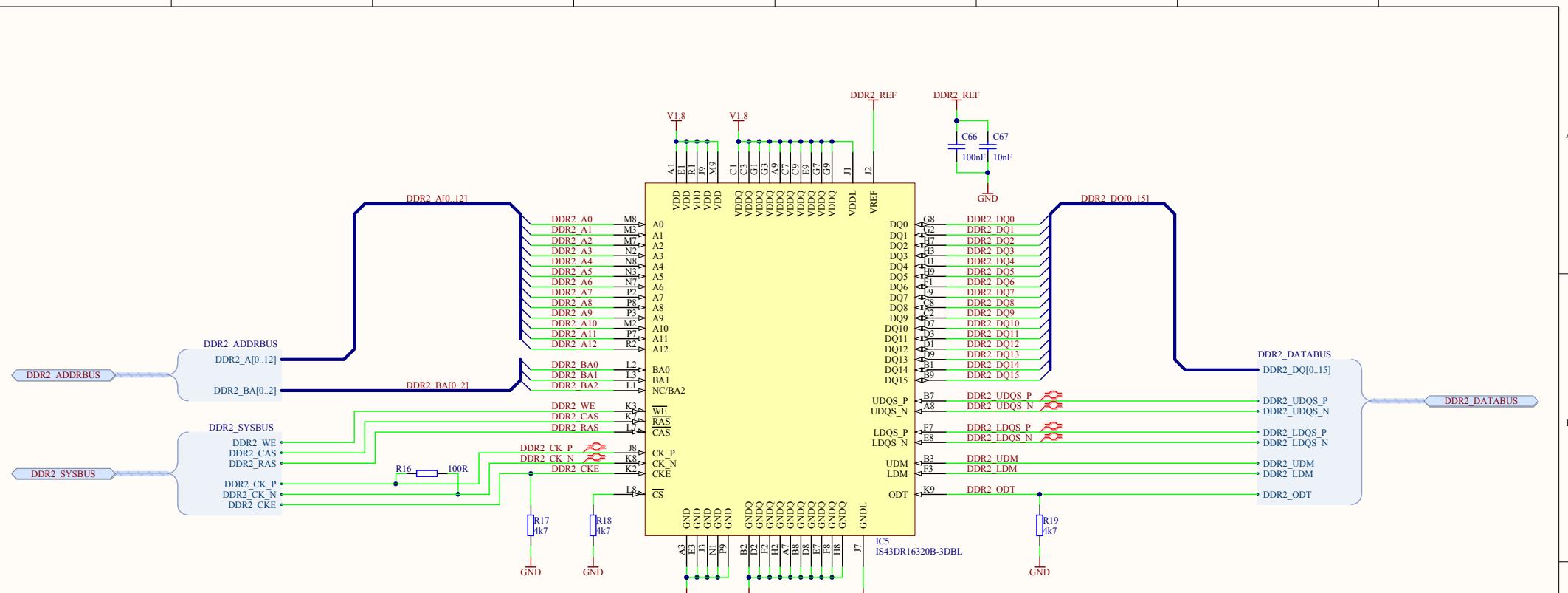


Title Minerva.PjPcb		
Size A3	Number MCU_Expansion.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet 7 of 20	
File: E:\Work\...\MCU Expansion.SchDoc	Drawn By: Vaclav Simek	

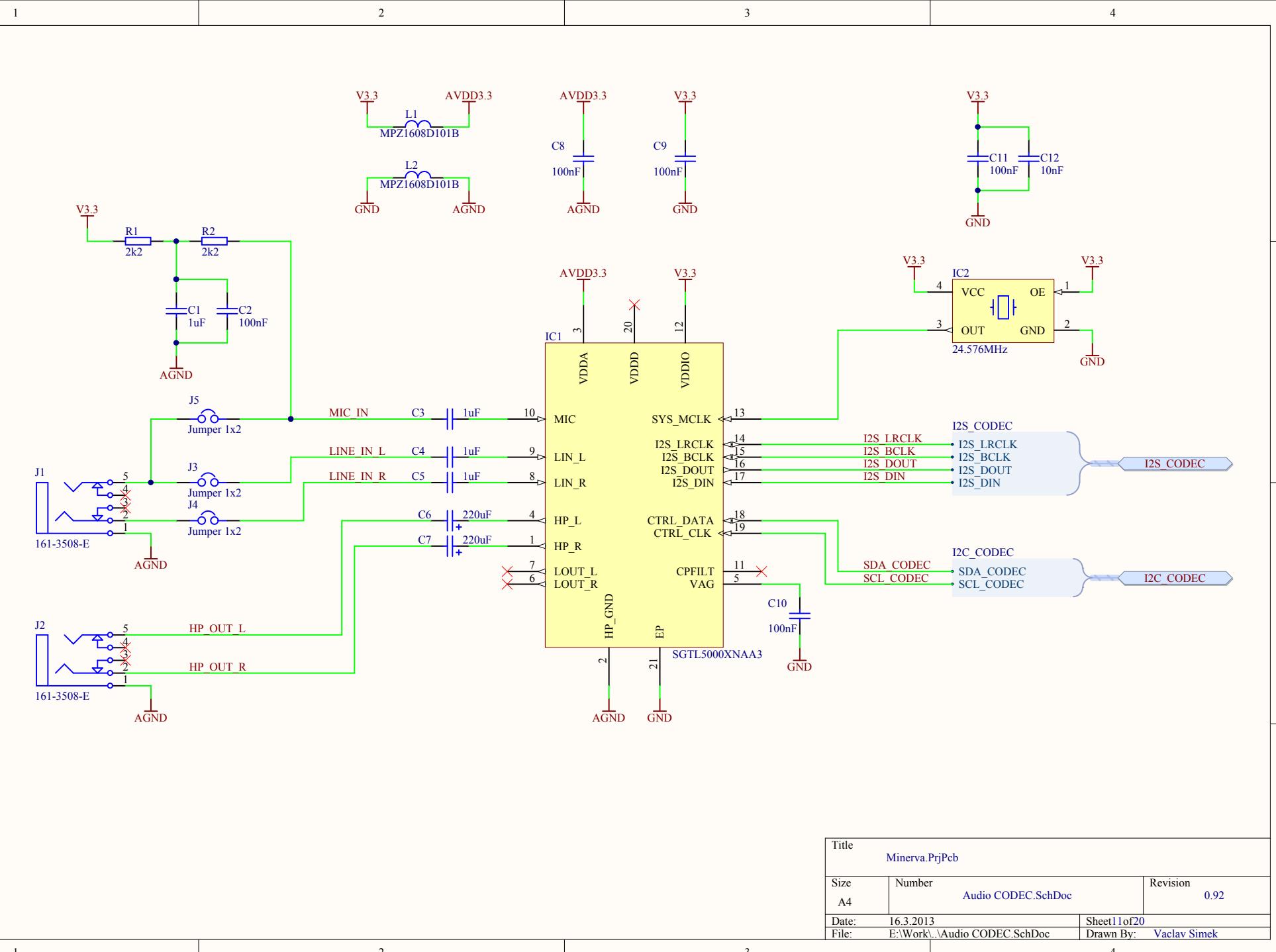


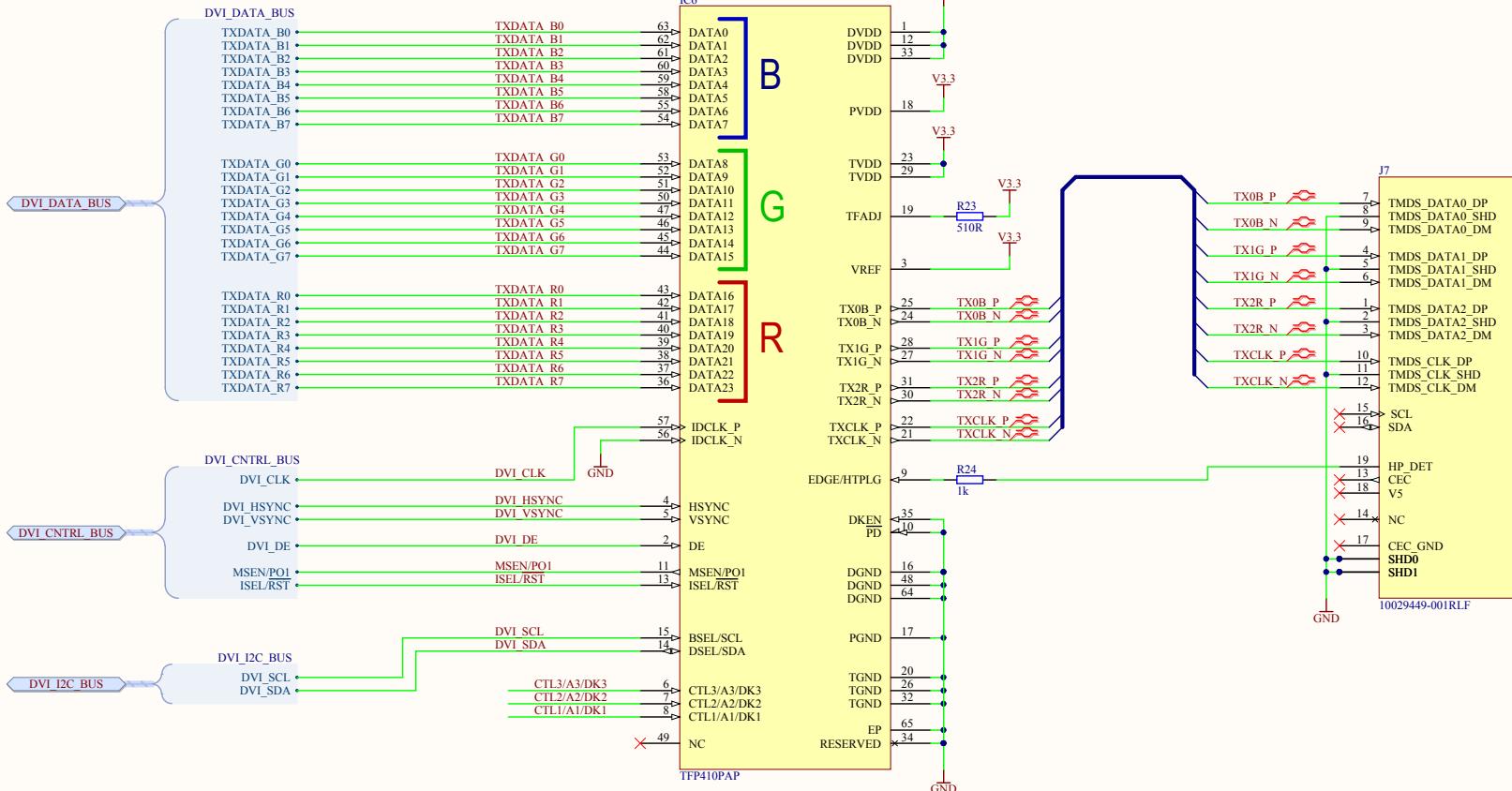
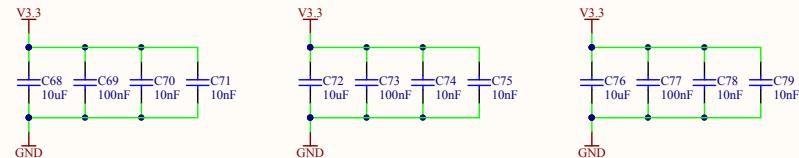


Title Minerva.PjPcb		
Size A3	Number Ethernet PHY.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet 9 of 20	
File: E:\Work\...\Ethernet PHY.SchDoc	Drawn By: Vaclav Simek	



Minerva.PrjPcb		
Size	Number	Revision
A3	DDR2 Memory.SchDoc	0.92
Date:	16.3.2013	Sheet10oof20
File:	E:\Work\DDR2 Memory SchDoc	Drawn By: Vaclav Simek

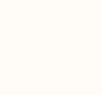




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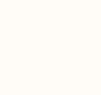
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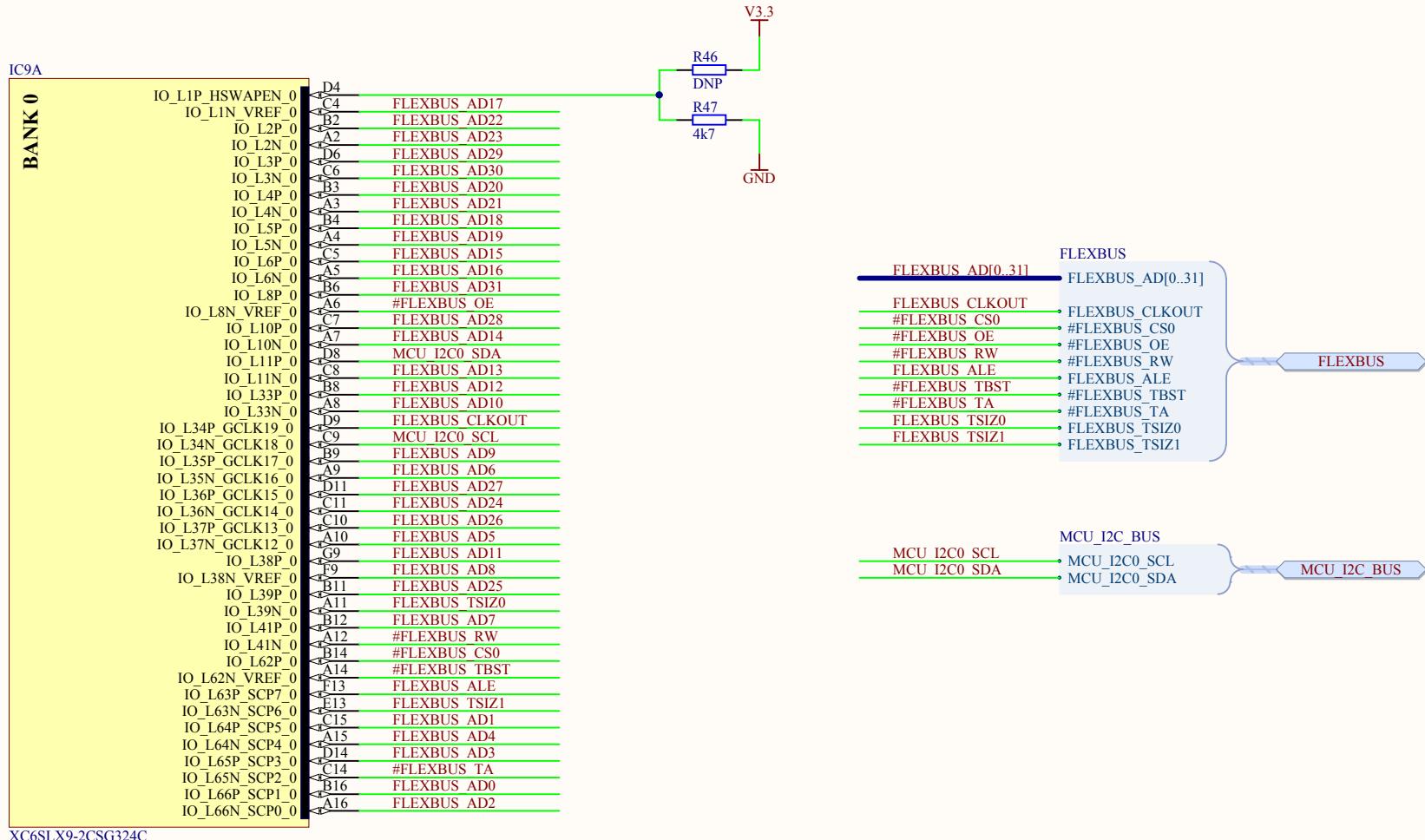
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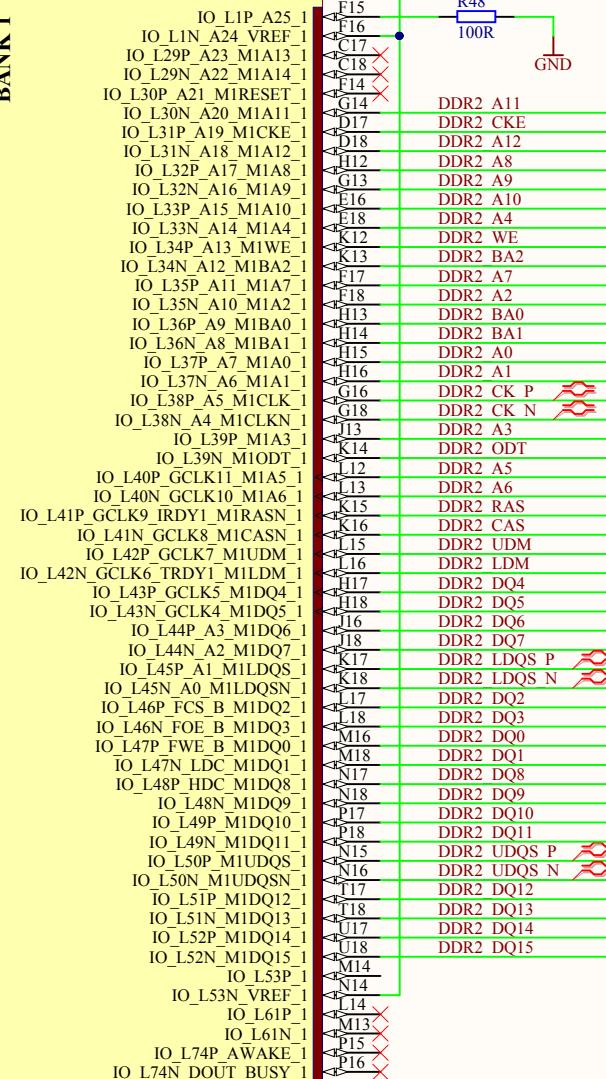
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Minerva.PjPcb		
Size	Number	Revision
A3	DVI Controller.SchDoc	0.92
Date:	16.3.2013	Sheet12of20
File:	E:\Work\...\DVI Controller.SchDoc	Drawn By: Vaclav Simek



Title
Minerva.PnjPcb

Size	Number	Revision
A4	FPGA_Bank_0.SchDoc	0.92
Date:	16.3.2013	Sheet13of20
File:	E:\Work\..\FPGA_Bank_0.SchDoc	Drawn By: Vaclav Simek

IC9B

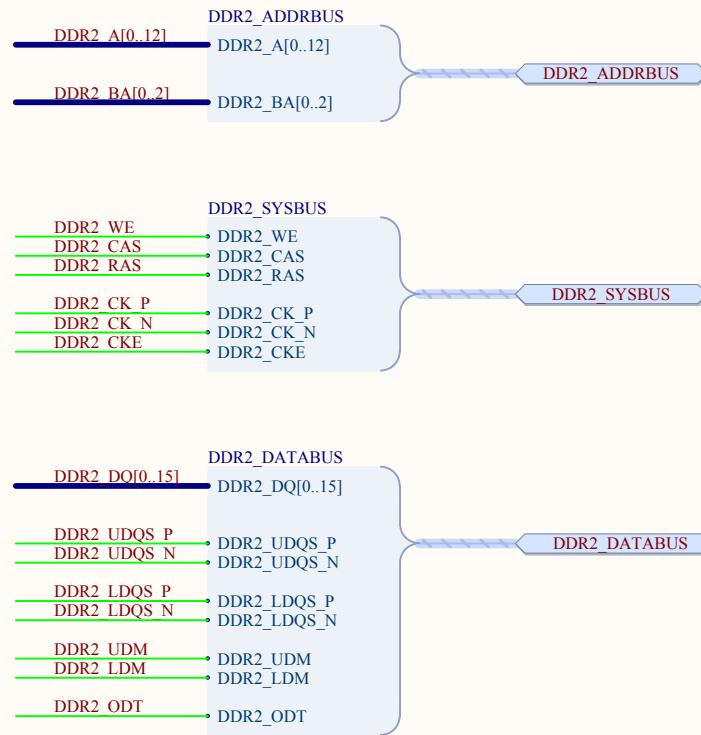
BANK 1

XC6SLX9-2CSG324C

DDR2_REF

100R

GND

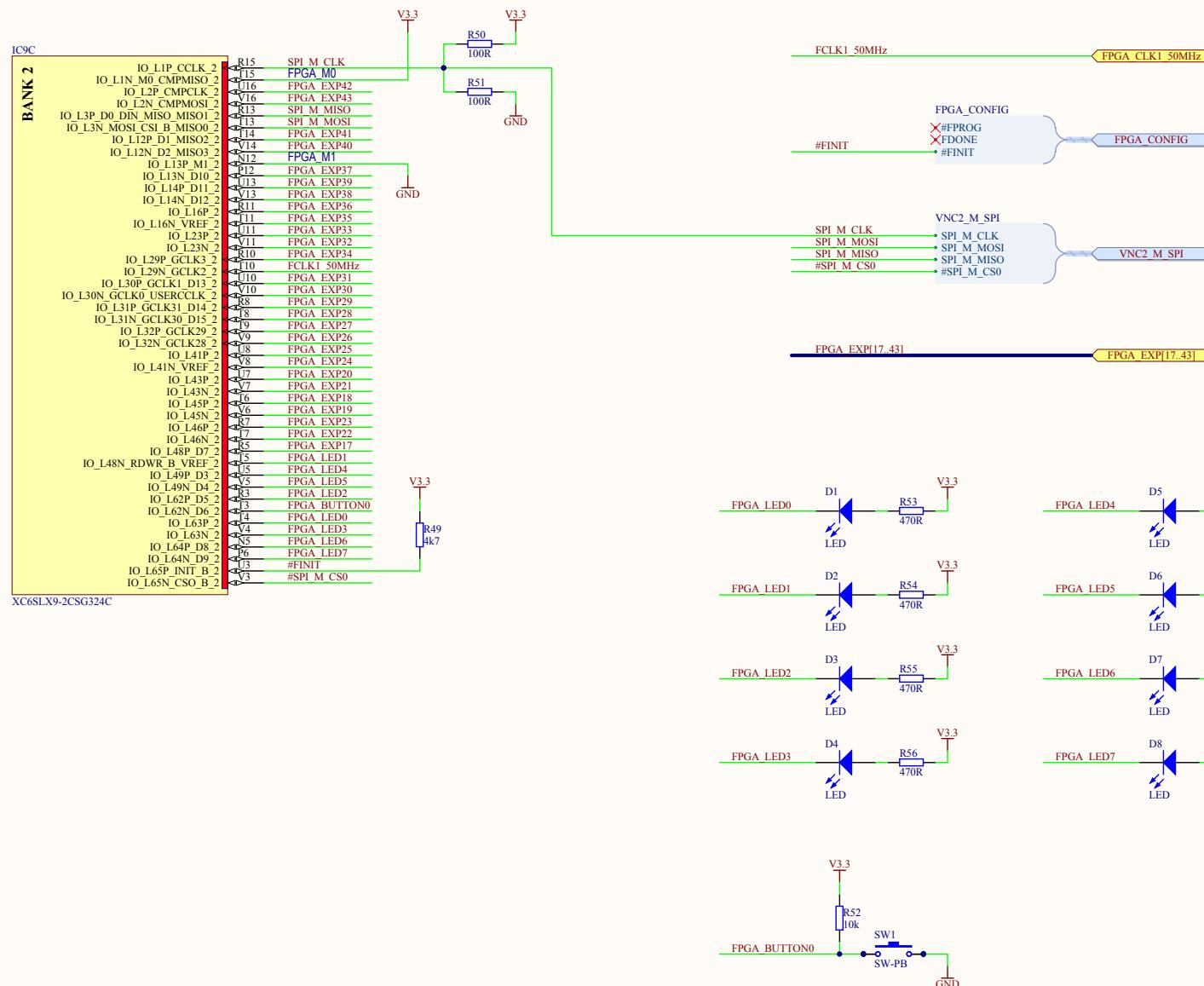


Title
Minerva.PnjPcb

Size	Number	FPGA Bank 1.SchDoc	Revision
A4			0.92
Date:	16.3.2013	Sheet14of20	
File:	E:\Work\...\FPGA Bank 1.SchDoc	Drawn By:	Vaclav Simek

A

A



B

B

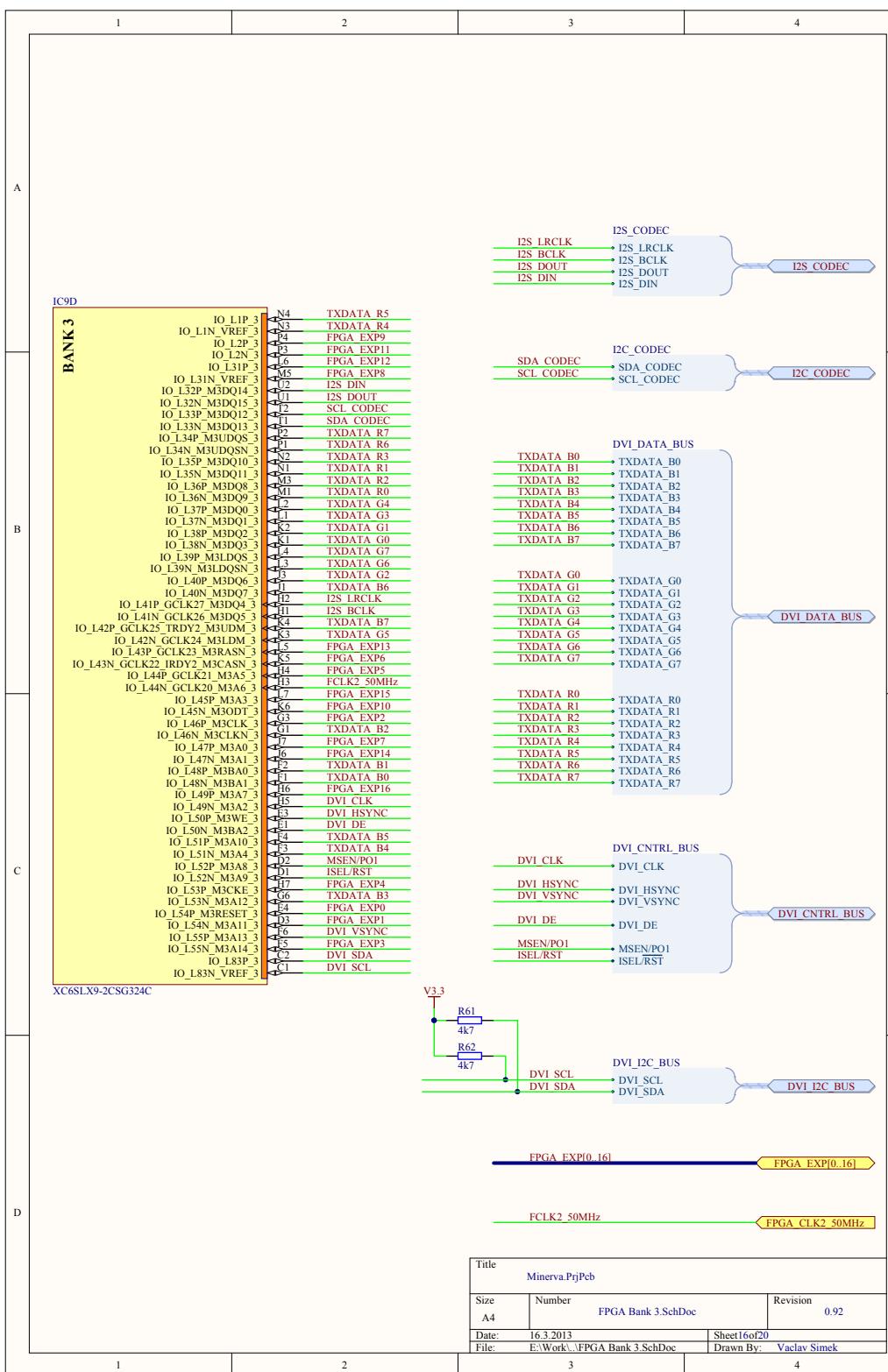
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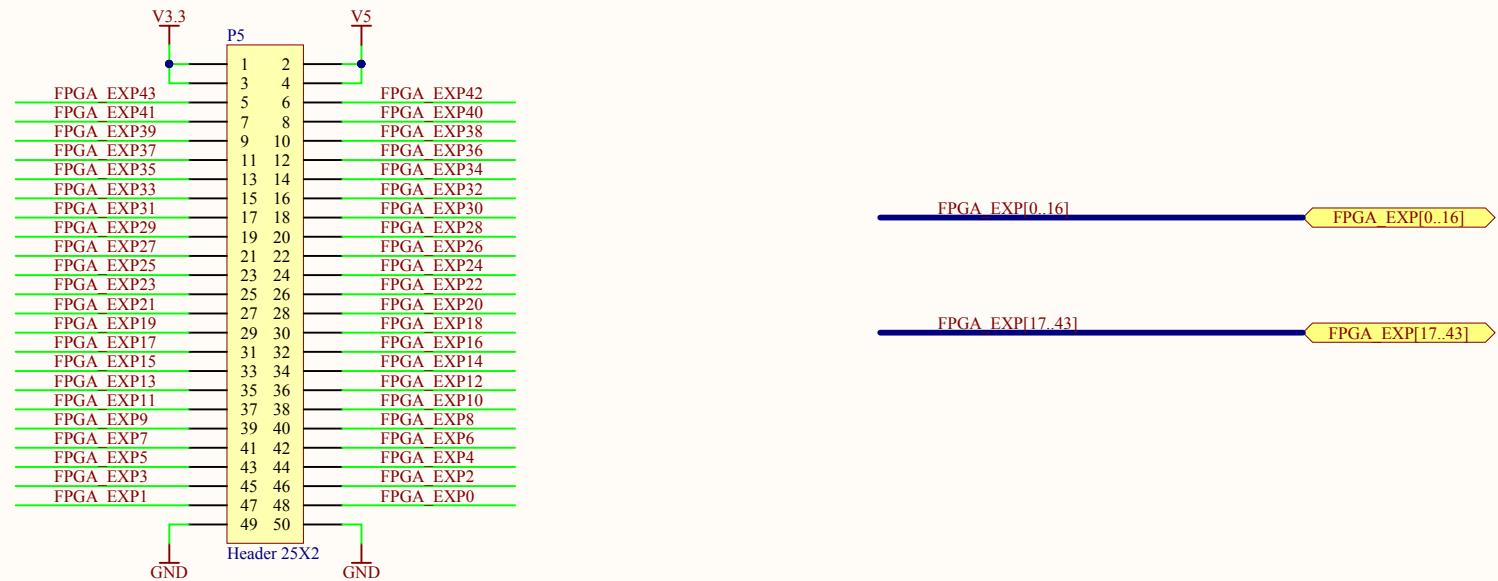
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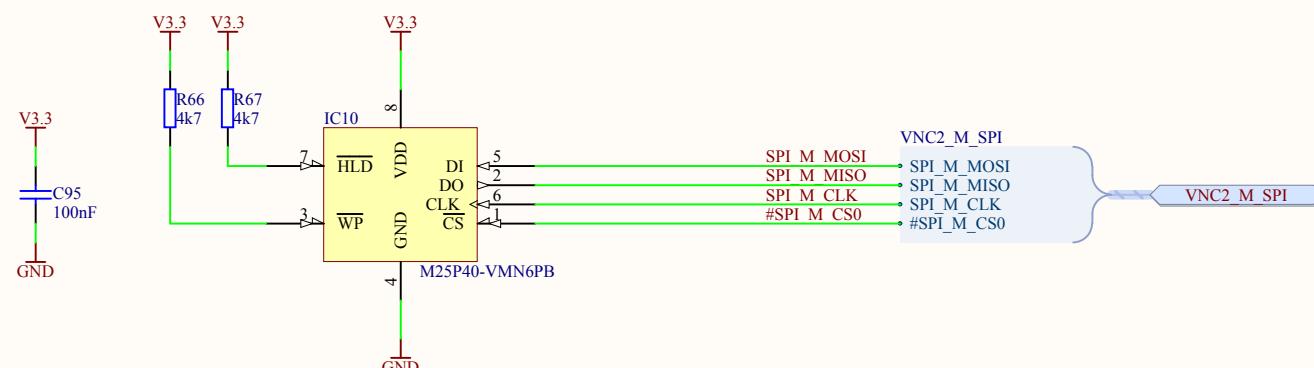
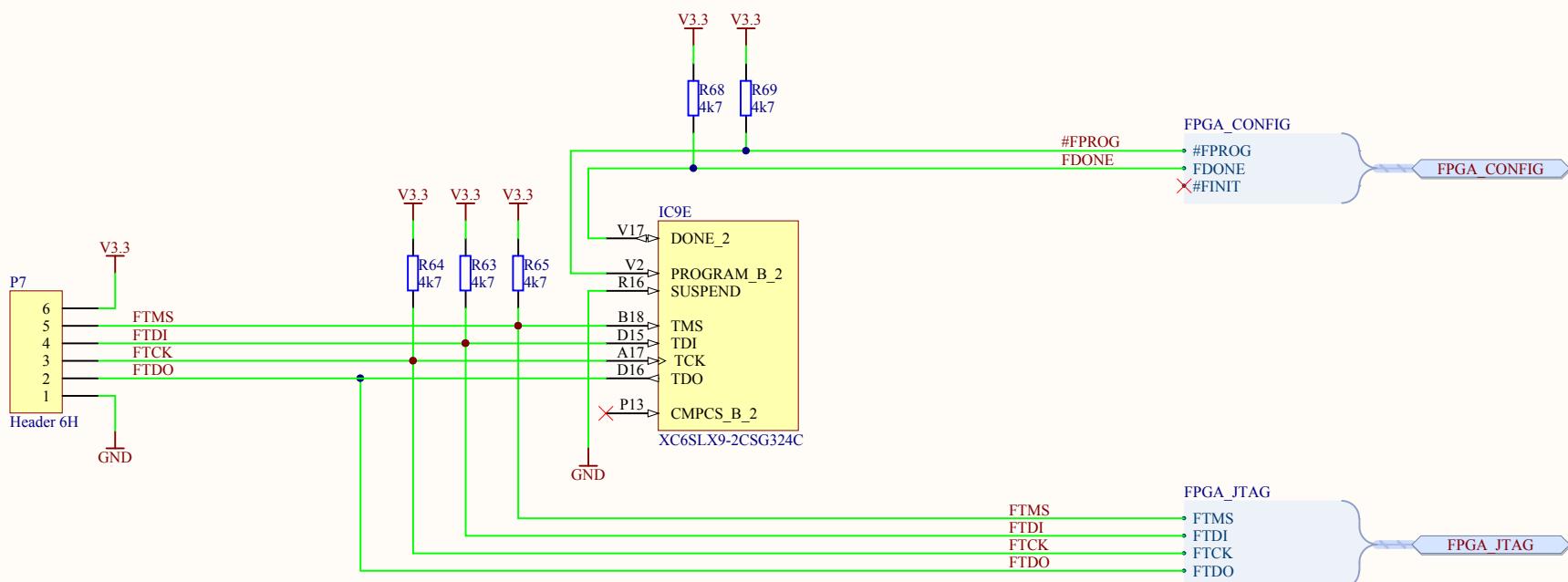
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Title Minerva.PrjPcb		
Size A3	Number FPGA Bank 2.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet15of20	
File: E:\Work_\FPGA Bank 2.SchDoc		Drawn By: Vaclav Simek



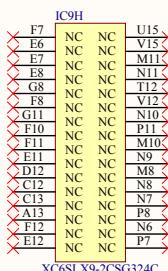
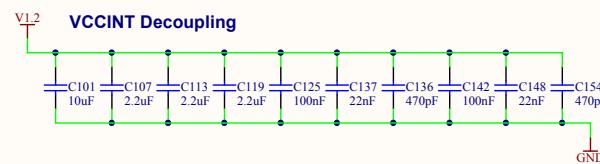
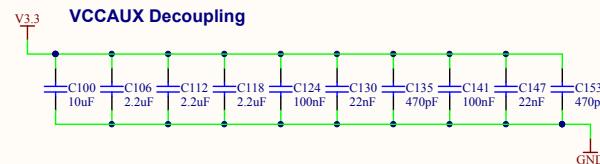
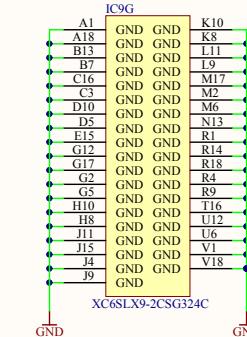
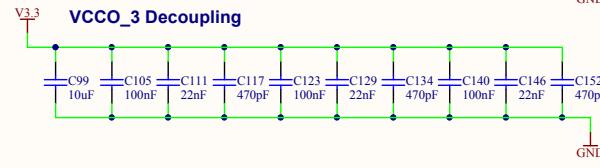
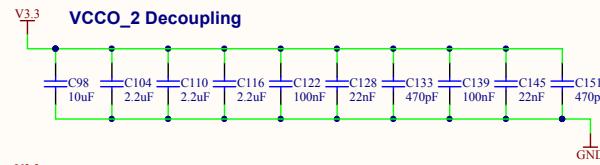
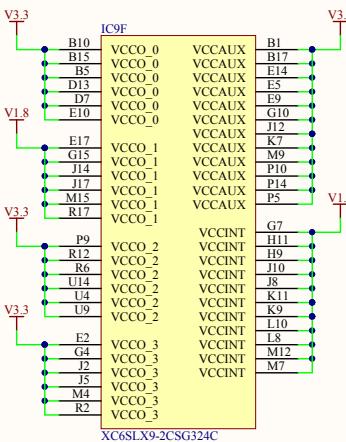
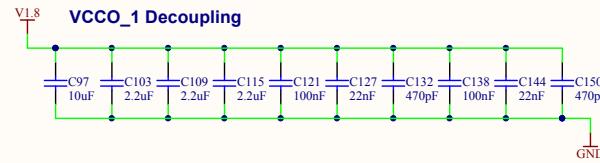
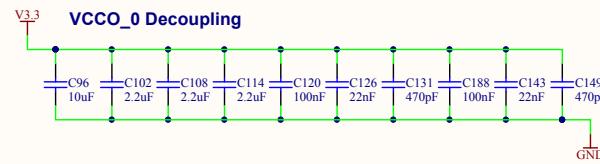


Title Minerva.PrjPcb		
Size A4	Number FPGA_Expansion.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet 17 of 20	
File: E:\Work\..\FPGA_Expansion.SchDoc	Drawn By: Vaclav Simek	



Title			
Minerva.PrjPcb			
Size	Number	Revision	
A4	FPGA Config.SchDoc	0.92	
Date:	16.3.2013	Sheet1of20	
File:	E:\Work_\FPGA Config.SchDoc	Drawn By:	Vaclav Simek

A



Title Minerva.PjPcb		
Size A3	Number FPGA Power.SchDoc	Revision 0.92
Date: 16.3.2013	Sheet19of20	
File: E:\Work_\FPGA Power.SchDoc		Drawn By: Vaclav Simek

