

## Tunnel Diodes All Around (TDAA)

Could Esaki Diodes be used for Logic & Memory Gates?

“For many purposes, a three-terminal device, such as a field-effect transistor, is more flexible than a device with only two terminals. Practical tunnel diodes operate at a few milliamperes and a few tenths of a volt, making them low-power devices.[12]”

“A [tunnel diode](#) or Esaki diode is a type of semiconductor diode that has effectively "negative resistance" due to the quantum mechanical effect called tunneling. It was invented in August 1957 by Leo Esaki when working at Tokyo Tsushin Kogyo, now known as Sony.[1][2]”

<https://forum.allaboutcircuits.com/threads/i-found-this-link-about-making-your-own-tunnel-diode-quite-interesting.107895/>

<https://electronics.stackexchange.com/questions/534205/how-can-a-tunnel-diode-be-used-as-a-memory-element>

[https://web.archive.org/web/20100107111641/https://www.eetimes.com/special/special\\_issues/millennium/milestones/holonyak.html](https://web.archive.org/web/20100107111641/https://www.eetimes.com/special/special_issues/millennium/milestones/holonyak.html)

“Superconducting digital logic circuits use single flux quanta (SFQ), also known as magnetic flux quanta, to encode, process, and transport data. SFQ circuits are made up of active Josephson junctions and passive elements such as inductors, resistors, transformers, and transmission lines. Whereas voltages and capacitors are important in semiconductor logic circuits such as CMOS, currents and inductors are most important in SFQ logic circuits. Power can be supplied by either direct current or alternating current, depending on the SFQ logic family.”

[https://semiengineering.com/knowledge\\_centers/integrated-circuit/transistors/3d/gate-all-around-fet/](https://semiengineering.com/knowledge_centers/integrated-circuit/transistors/3d/gate-all-around-fet/)

“As the fin width in a finFET approaches 5nm, channel width variations could cause undesirable variability and mobility loss. One promising transistor candidate — gate-all-around FET — could circumvent the problem. Considered the ultimate CMOS device in terms of electrostatics, gate-all-around is a device in which a gate is placed on all four sides of the channel. It’s basically a silicon nanowire with a gate going around it.”

### Outsider's Analysis

While CMOS and GAA continue to see application at shrinking nodes, the energy efficiency of superconducting semiconductors has seen limited research. Previous research has shown that [static](#) power can consume more than 10 times dynamic power in Rapid Single Flux Quantum (RSFQ), while [newer research](#) has shown improvements up to [65x](#) in superconducting diodes to 80x efficiency compared to CMOS using Adiabatic Quantum Flux Parametron (AQFP), even after accounting for cooling.

While the MANA (Monolithic Adiabatic iNtegration Architecture) uses between 10,000 AQFPs (20,000 Josephson junctions), applying that to SRAM will require up to 8x the number of gates. Whether [cryogenic](#) cooling will be a practical technology for mobile and edge devices remains to be seen, although [room](#)-temperature superconductors could also lead to that.

### Citations:

<sup>12</sup>. Turner, L.W., ed. (1976). *Electronics Engineer's Reference Book* (4th ed.). London, UK: Newnes-Butterworth. pp. 8–18. [ISBN 0-408-00168-2](#).