T-HEAD

XuanTie CPU Series

C-SKY Introduction

what's the meaning of a new arch for linux

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<https://github.com/c-sky/buildroot>

C-SKY Upstream

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https://git.kernel.org/pub/scm/linux/kernel/git/torvalds/linux.git/commit/?h=master&id=ac435075892e3e651c667b4a9f2267cf3ef1d5a2

```
Arnd acks, and adds the following notes:
 "I did a thorough review of the ABI, which as usual mainly consists of
  spotting any files that don't use the asm-generic ABI itself, and
  having it changed to it matches exactly what we do on other new
  architectures.

  I also looked at every other patch and commented on maybe half of them
  where I saw something that did not quite seem right. Others have
  reviewed specific patches in greater depth. I'm sure that one could
  fine more of the minor details, but as long as they are not ABI
  relevant, they can be fixed later.

  The only patch that is part of the ABI and that nobody reviewed is the
  signal handling. This is one of the areas I never worked on in much
  detail. I did not see anything wrong with it, but I also don't know
  what the problems with the other architectures are here, and we seem
  to be hitting issues occasionally, and we never managed to generalize
  this enough for new architectures to have a trivial implementation.

  I was originally hoping that we could have the 64-bit time_t
  interfaces ready in time to completely drop the 32-bit ones, but that
  did not happen. We might still remove them in the next merge window
  depending on whether the libc upstream people prefer to keep them or
  not.

  One more general comment: I think this may well be the last new CPU
  architecture we ever add to the kernel. Both nds32 and c-sky are made
  by companies that also work on risc-v, and generally speaking risc-v
  seems to be killing off any of the minor licensable instruction set
  projects, just like ARM has mostly killed off the custom
  vendor-specific instruction sets already.

  If we add another architecture in the future, it may instead be
  something like the LLVM bitcode or WebAssembly, who knows?"

To which Geert Uytterhoeven pipes in about another architecture still in
the pipeline: Kalray MPPA.
```

A little regret (missing comment)

2018-10-30 00:22:45 +0800

https://lore.kernel.org/lkml/20181029162243.GA988@guoren-Inspiron-7460/

> ISA is like a language, we will learn foreign languages, but we will not give up our mother tongue. RISC-V is a great ISA, and it will promote other ISAs to be more open.
>
> From ecology, diversity will make Linux more robust.
>
> We will continue to improve csky subsystem, and now is only the beginning.
>
> Best Regards
> Guo Ren

Our jobs:

CPU	ISA	Linux Directory
610 (no sale)	MCORE 32 (Modified)	linux/arch/csky/abiv1
807/810/860	**C-SKY 32**	linux/arch/csky/**abiv2**
910	RISC-V 64	linux/arch/riscv

- Now we need take care of 3 ISAs with 5 cores
- Kernel, glibc, uclibc-ng, buildroot, elfutils, strace, greenlet, perf, systemtap ...
- https://**gitlab**.com/c-sky/**buildroot**/pipelines

Kernel Version

- Linux-next
- Linux-4.19
- Linux-4.9

Quick Start:

https://github.com/c-sky/buildroot

Boot

code:

- https://c-sky.gitlab.io/-/buildroot/-/jobs/346100688/artifacts/output/images/hw/gdbinit.c860mp.txt
- https://git.kernel.org/pub/scm/linux/kernel/git/torvalds/linux.git/tree/arch/csky/kernel/head.S
- https://git.kernel.org/pub/scm/linux/kernel/git/torvalds/linux.git/tree/arch/csky/kernel/setup.c

Our Principle:

- Easy to use
- Easy to understand

Use KSEG for 32bit CPU

- KSEG is an ancient technology from mips.
  https://johnloomis.org/microchip/pic32/memory/memory.html
- We also have KSEG0, KSEG1, but they are used mapping 0-1GB cached memory (No IO map) to reduce unnecessary TLB miss
- We also provide base regs to support any start physical address (512MB align)
- Why we use KSEG ?
  - It’s cheaper than middle level page mapping for hardware
  - It’s more efficient than MMU for hardware
  - Hugetlbfs and THP are useless in 32b system with small memory (personal opinion)

Current State:

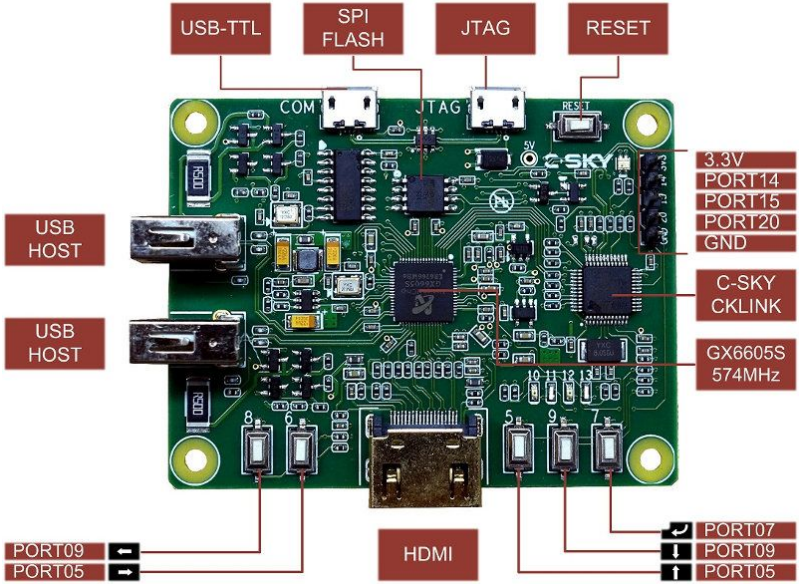
- Highmem
- SMP
  - cpu hotplug
  - 1024 sources root interrupt controller
  - support both percpu-irq and comm-irq in one driver
- Ftrace, Dynamic Ftrace
- Strace
- Perf (Hardware PMU supported with perf record)

Recent Plan:

- SystemTap (kprobe/uprobe)
- VDSO Optimization
- BPF JIT
- Trace with “perf record -e thead_pt/*”
- IOMMU

$6 Linux Development Board with C-SKY ISA

https://c-sky.github.io/docs/gx6605s.html



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Thank you

Actually, I don’t know what’s the meaning of a new arch for linux :P

But we’ll continue improving the arch - day by day, patch by patch
Just continue working & keep changing